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# Impact of PECVD μc-Si:H deposition on tunnel oxide for passivating contacts

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Abstract. Passivating contacts are becoming a mainstream option in current photovoltaic industry due to their ability to provide an outstanding surface passivation along with a good conductivity for carrier collection. However, their integration usually requires long annealing steps which are not desirable in industry. In this work we study PECVD as a way to carry out all deposition steps: silicon oxide  $(SiO_x)$ , doped polycrystalline silicon (poly-Si) and silicon nitride  $(SiN_x:H)$ , followed by a single firing step. Blistering of the poly-Si layer has been avoided by depositing  $(p^+)$  microcrystalline silicon ( $\mu$ c-Si:H). We report on the impact of this deposition step on the SiO<sub>x</sub> layer deposited by PECVD, and on the passivation properties by comparing PECVD and wet-chemical oxide in this hole-selective passivating contact stack. We have reached iVoc > 690 mV on p-type FZ wafers for wet-chemical SiO<sub>x</sub>\( $p^+$ )  $\mu$ c-Si\SiN<sub>x</sub>:H with no annealing step.

Keywords: Silicon solar cell / passivating contact / silicon oxide /  $\mu$ c-Si:H / PECVD / XPS / passivation / cast-mono

### 1 Introduction

Crystalline silicon solar cell is the dominant technology in today's photovoltaic (PV) market. In order to foster PV development and make it economically more competitive, it is necessary to further reduce production costs as well as to increase cell efficiencies. In order to achieve the latter, reducing recombination losses at the metal/semiconductor interface is of paramount importance. To do so, the integration of so-called passivating contacts is a mainstream option [1–3]: they consist of a silicon oxide (SiO<sub>x</sub>) doped polycrystalline silicon (poly-Si) stack that allows an outstanding surface passivation while providing a low series resistance and higher conductivity than doped a-Si:H.

As for cost reduction, the main option is to reduce the number of processing steps. For example, Ingenito et al. use a single firing step to both contact and anneal the cell, while limiting the overall thermal budget applied to the silicon wafer [4]. Additionally,  $SiO_x$  and doped poly-Si layers can be deposited sequentially by PECVD [5].

high quality silicon wafers. This is the case of the castmono silicon technology, which has reached industrial maturity and is currently being commercialized by companies such as Photowatt through their technology Crystal Advanced [6]. The aim of this work is to study the feasibility of a low

The aim of this work is to study the feasibility of a low thermal budget-route for hole-selective passivating contacts fabrication using a full PECVD process, and to investigate the relevance of using mono-cast silicon wafers.

Another way to further reduce costs is to use low-cost,

#### 2 Methods

#### 2.1 Sample fabrication

#### 2.1.1 Substrate

Firstly the SiO<sub>x</sub> and  $(p^+)$  poly-Si layers were developed on one side of double side polished (DSP) *n*-type Cz silicon wafers (280 µm thick, and wafer resistivity of 1–5  $\Omega$ .cm), that were cleaned with a HF dip (5% for 30 s). Secondly, the "lifetime samples" were symmetrical structures, deposited on three kinds of *p*-type silicon substrates described in Table 1.

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**Table 1.** Characteristics of *p*-type wafers used for lifetime samples. SDR stands for saw damage removal, and the texturation bath is composed of KOH and additives.

Float-zone	Cz	Mono-cast
DSP	SDR + textured	SDR + textured
$280\mu{ m m}$	$170\mu{ m m}$	$190\mu{ m m}$
$35~\Omega.\mathrm{cm}$	$24~\Omega.\mathrm{cm}$	1–3 $\Omega.\mathrm{cm}$

These wafers were RCA cleaned and the remaining oxide was removed by an HF dip (HF 5% diluted in deionized water DIW, for 20 s).

#### 2.1.2 Tools

The SiO<sub>x</sub> layer was either deposited in an RF-PECVD reactor Octopus II (INDEOtec) at 175 °C with a gas mixture of SiH<sub>4</sub>, H<sub>2</sub> and CO<sub>2</sub>, or wet-chemically grown using a second round of RCA2 process (DIW, H<sub>2</sub>O<sub>2</sub>, HCl mixture for 10 min at 75 °C). The  $(p^+)$  Si layer was deposited by PECVD in Octopus II at 175 °C with a gas mixture of SiH<sub>4</sub>, H<sub>2</sub> and trimethylborane (B(CH<sub>3</sub>)<sub>3</sub>, noted TMB). The silicon nitride layer (SiN<sub>x</sub>:H) was deposited in a capacitively coupled RF-PECVD reactor (MVSystems) at 340 °C with a gas mixture of SiH<sub>4</sub> and NH<sub>3</sub>. On a few symmetric samples we deposited a stack of (i) a-Si:H\ $(n^+)$  a-Si:H in Octopus II at 175 °C. The annealing and firing steps were done in a Jetfirst rapid thermal annealing furnace (Jipelec).

#### 2.1.3 Different batches

In Batch 1, as-deposited 1–2 nm thick PECVD SiO<sub>x</sub>, as well as the 30 nm thick PECVD (p<sup>+</sup>)  $\mu$ c-Si:H on SiO<sub>x</sub> before and after firing step (1 s at 850 °C) were optically optimized and studied. In Batch 2, the effective lifetime of "lifetime samples" with 1–2 nm PECVD SiO<sub>x</sub>\30 nm PECVD (p<sup>+</sup>)  $\mu$ c-Si:H\70 nm PECVD SiN<sub>x</sub>:H was measured. In Batch 3, the passivation of "lifetime samples" with 1–2 nm wetchemical SiO<sub>x</sub>\30 nm PECVD (p<sup>+</sup>)  $\mu$ c-Si:H\70 nm PECVD SiN<sub>x</sub>:H was studied as well. Batch 4 was a reference passivation batch, in order to evaluate the highest passivation that can currently be reached on our wafers, by depositing a stack of 10 nm (i) a-Si:H\60 nm (n<sup>+</sup>) a-Si:H followed by a 220 °C annealing step for 10 min.

#### 2.2 Characterization

The optical properties of the deposited layers were measured by spectroscopic ellipsometry (SE) with a Horiba Jobin Yvon Uvisel 2 ellipsometer. The data were processed with the DeltaPsi2© software.

The X-ray Photoelectron Spectroscopy (XPS) analyses were carried out with a Thermo Fischer K-Alpha<sup>+</sup> spectrometer using a monochromatic Al-k $\alpha$  source at 1486.6 eV. The in-depth composition and chemical environments were obtained by sequential Ar<sup>+</sup> sputtering (1000 eV, 30 s). The XPS spot size was 400  $\mu$ m for a depth probed in the range of 10 nm. High resolution spectra were acquired using a 20 eV pass energy. Data were processed using the Thermo Avantage© software.

Images of the surface of the samples were acquired with an OLS5000 confocal microscope (Olympus). Lifetimes of the symmetric samples were measured by Quasi Steady-State Photoconductance using a WCT-120 (Sinton Instruments). Photoluminescence (PL) images calibrated in lifetime were acquired with an LIS-R2 (BT Imaging).

#### 3 Results and discussion

#### 3.1 PECVD process

We developed a process for depositing  $\text{SiO}_x$  by PECVD at 175 °C (Batch 1). In order to supply the required oxygen amount, we increased the  $r = \text{CO}_2/\text{SiH}_4$  gas flow rates ratio. The optical properties of these films were measured by SE, and fitted with Tauc-Lorentz model [7]. For r = 10 we got a material with n(633 nm) = 1.6 and k(400 nm) = 0.007.

In standard passivating contact fabrication, a hydrogenated amorphous silicon (a-Si:H) layer is deposited, and then annealed for a long time at high temperature (usually  $850 \,^{\circ}$ C for 30 min or more [5,8–10]). This can lead to the formation of blisters. The aim of this work being to spend a low thermal budget, this annealing step was skipped. A single firing step, however, leads to even higher stress, resulting in an easier formation of blisters. One way to tackle this issue was to dilute  $SiH_4$  into  $H_2$  [10,11]. We deposited 1–2 nm of PECVD  $SiO_x$  (30 s deposition), and subsequently deposited the boron doped silicon layer on top of it. Doing so, we varied the  $SiH_4$  flow rate, and consequently its dilution into hydrogen. The samples were then subject to a firing step (850 °C for a few seconds). The confocal images of the surface are shown in Figure 1. It can be seen that at lower  $R = H_2/SiH_4$  flow rate ratio (R = 50), a lot of blisters form, whereas at R = 125, none can be seen. The thicknesses of the layers are respectively, for R = 50/63/83/125: 38/33/26/24 nm, measured by ellipsometry in the layers that are shown in Figure 1. Experiments were carried out with adapted layer thicknesses (35/37/35/37 nm) and the same trend is obtained, with blisters appearing for the first 3 samples, and no blister for R = 125.

The optical properties of these four samples were measured by SE before annealing, and models have been made in order to fit them as a stack of a SiO<sub>x</sub> layer with fixed optical properties – known by SE measurements from the SiO<sub>x</sub> optimization step – and an effective medium layer composed of a mixture of a-Si:H, voids and  $\mu$ c-Si:H on top of it (Bruggeman model [12]). Figure 2 shows the crystalline fraction of the silicon layer (fraction of the material being fitted as small-grain c-Si material), and the fitted thickness of the underlying oxide layer. The crystalline fraction increased when decreasing the silane flow rate. Surprisingly, the thickness of the oxide layer also seemed to decrease. In order to investigate this phenomenon, an XPS analysis was carried out on the samples deposited with R = 50 and R = 125 flow rate ratios.



# 6 sccm

## 4 sccm

Fig. 1. Confocal images of the surface of  $SiO_x (p) \ \mu c-Si:H$ samples *after firing step* (Batch 1) for different  $R = H_2/SiH_4$ ratios.



Fig. 2. Evolution of crystalline fraction in the PECVD silicon layer, and fitted silicon oxide thickness with the  $SiH_4/H_2$  flow rate ratio on Batch 1 samples *before firing step*. Nominal  $SiO_x$  thickness is 2.2 nm.

## 3.2 Morphology of PECVD SiO<sub>x</sub> layer

To get insight on the possible evolution of the buried  $\text{SiO}_x$  layer thickness, XPS depth profile analyses were realized on Batch 2 samples with a 30 nm thick silicon layer deposited with  $R = \text{SiH}_4/\text{H}_2 = 50$  or R = 125 on top of the same oxide. The XPS Si and O concentration profiles



**Fig. 3.** Concentration profile of an as-deposited stack of c-Si\PECVD SiO<sub>x</sub>\PECVD ( $p^+$ ) µc-Si:H (deposited with R = 125) from Batch 1.

obtained on the R = 125 sample are presented in Figure 3. Despite the high surface sensitivity of XPS, the detection of this ultra-thin SiO<sub>x</sub> layer is challenging since its 1-2 nm thickness is inferior to the escape depth of the emitted photoelectrons, requiring the optimization of the abrasion sequence not to cross over the layer.

This profile evidences three regions in agreement with the corresponding  $\mu$ c-Si:H, SiO<sub>x</sub> and c-Si stack structure.

Contrarily to what was estimated by SE, for sample with  $\mathrm{SiH}_4/\mathrm{H}_2 = 125$ , this profile shows that the oxide layer is still present in-between the c-Si and the  $\mu$ c-Si:H layer. An oxygen concentration bump is clearly visible, with a maximum of the oxygen content corresponding to the moment when the surface of the silicon oxide layer is reached. Indeed, since depth resolution is limited by the approximate 10 nm escape depth of the photoelectrons, the oxygen starts being detected before the interface is physically reached by sputtering and then starts decreasing afterward, while the Si content conversely rises.

Figure 4a shows the Si2p core levels measured at the surface of the buried oxide layer samples with a-Si:H (R = 50) and  $\mu$ c-Si (R = 125) as silicon layer. The reference spectrum obtained on a 1-2 nm of  $\text{SiO}_x$  deposited by PECVD on a silicon wafer previously cleaned by HF is presented as a comparison. The intensity of the peak situated at 98.8 eV corresponding to the Si–Si bonds is the same for all the spectra. Since it is related to the collection of the photoelectrons emitted by the c-Si wafer underneath the oxide, and that the intensity decreases with the thickness of oxide on top of it, we can assess that there is no apparent etching of the  $SiO_x$  layers. However, it can be seen that the Si-O contributions at higher binding energy are notably modified. The well-defined and roughly symmetric characteristic feature around 103.0 eV obtained for the reference PECVD  $SiO_x$ , is modified indicating changes in the oxide network and the presence of a set of suboxides in relation with the tail like shape of the left part of the Si2p peak. This is an important piece of information since it



**Fig. 4.** (a) Si2p and (b) O1s spectra at the surface of the oxide layer (Batch 1).

means that in both studied conditions the deposition of the silicon layer changes significantly the oxide layer chemistry. Figure 4b shows the corresponding O1s photopeaks. It can be seen that the overall oxygen content of the encapsulated layers has significantly decreased, in agreement with the presence of suboxides. A possible explanation for the oxygen loss after silicon deposition may be an etching phenomenon by the hydrogen plasma operated during the (p)  $\mu$ c-Si:H deposition step. To sum up, the deposition of the silicon layer on top of our  $SiO_r$  layer grown by PECVD does not remove it nor reduce its thickness, but it modifies its chemistry, leading to oxygen removal, and changes in the oxidation degree. However, no major difference could be observed between the two samples studied (a-Si:H with R = 50 and  $\mu$ c-Si with R = 125), thus questioning the accuracy of the SE model for such thin buried layers.

#### 3.3 Passivation of FZ DSP wafers

In Tables 2 and 3, we compare the minority carrier lifetime and implied Voc of symmetric samples for

**Table 2.** Lifetime of symmetric samples from Batches 2 and 3 on FZ wafers with wet  $\operatorname{SiO}_x \setminus (p^+) \mu c$ -Si before and after deposition of  $\operatorname{SiN}_x$ :H (no annealing step).

$SiO_x$ layer	Before SiN	After SiN
RF-PECVD	$5\mu{ m s}$	$6\mu s$
Wet-chemical	$67\mu s$	$909\mu s$

**Table 3.** Implied Voc of symmetric samples from Batches 2 and 3 on FZ wafers with wet  $\text{SiO}_x \setminus (p^+) \mu c$ -Si before and after deposition of  $\text{SiN}_x$ :H (no annealing step).

$SiO_x$ layer	Before SiN	After SiN
RF-PECVD	549  mV	$558 \mathrm{mV}$
Wet-chemical	$619 \mathrm{~mV}$	$693 \mathrm{~mV}$



**Fig. 5.** Photoluminescence image calibrated in lifetime of a *p*-type FZ DSP 1/4 wafer passivated by a wet  $\text{SiO}_x \setminus (p^+) \mu \text{c-Si} \setminus \text{SiN}_x$ : H stack (Batch 3) with no annealing step.

RF-PECVD and standard wet-chemical oxides (RCA2) as deposition methods for the oxide in the stack  $\operatorname{SiO}_x(p^+)$  µc-Si $\operatorname{SiN}_x$ :H. The  $(p^+)$  µc-Si:H layer is deposited with a  $H_2/SiH_4$  gas ratio of 125. The samples are as-deposited (no annealing step). It can be noticed that the passivation provided by the stack with the PECVD oxide is very low, contrarily to the one with wetchemical oxide. This means that the process conditions used are not yet suited for passivating contacts. Although the lifetime of this sample was limited to  $6 \,\mu s$ , the one with the wet oxide with  $SiN_r$ : H capping reached  $909 \,\mu s$  and  $693 \,\mathrm{mV}$  of implied Voc. The very large increase of the passivation with  $SiN_{r}$ : H may be explained by the hydrogen in-diffusion from the  $SiN_x$ :H layer to the c-Si $SiO_x$  interface. A photoluminescence image calibrated in lifetime of this sample is shown in Figure 5. Locally, the passivation achieved is significantly higher than the average  $909 \,\mu s$ , reaching values up to 1.3 ms.

**Table 4.** Implied Voc of symmetric samples from Batches 3 and 4 for different passivation stacks on Cz and mono-cast wafers.

Passivation stack	Cz	Mono-cast
$\mathrm{SiO}_x \setminus (\mathrm{p}) \ \mu \mathrm{c-Si} \setminus \mathrm{SiN}_x \mathrm{H}$	$647 \mathrm{~mV}$	$648 \mathrm{~mV}$
(i,n) a-Si:H	$673 \mathrm{~mV}$	$670 \mathrm{~mV}$

The samples have been submitted to a firing step. The passivation was severely damaged (5  $\mu$ s, 570 mV). This was an expected behavior in the case of no further hydrogenation step. Indeed, Lehmann et al. have recently shown that in the case of fired passivated contacts, a subsequent hydrogenation step is necessary in order to achieve high passivation quality [13]. Further investigations need to be carried out on the capping layer in order to hinder the hydrogen effusion during this step.

#### 3.4 Cz vs. mono-cast textured wafers

For industrial integration, it is of major importance to deposit the passivating contacts on industrially relevant substrates, such as textured Cz or mono-cast silicon wafers. The passivation provided by passivated contacts with wet  $SiO_r$  is also compared with the one provided by amorphous silicon ((i) a-Si:H $(n^+)$  a-Si:H stack) as reported in Table 4. No difference is observed between mono-cast and Cz wafers as far as iVoc is concerned, meaning that the integration of passivating contacts on mono-cast wafers is definitely worth being investigated. It is broadly known that textured wafers are harder to passivate than chemically polished wafers, mostly because of increased surface area and a greater number of crystallographic imperfections [14]. As a consequence, the process still needs to be optimized to reduce the difference between passivating contacts and a-Si:H passivation, and the firing step needs to be carried out in order to allow the hydrogen contained in the  $SiN_x$ :H layer to diffuse and passivate the interface.

#### 4 Conclusion

In this study we have shown that it is possible to achieve a blister-free passivating contact structure after a single firing step by depositing doped  $\mu$ c-Si:H by PECVD without annealing on top of the oxide layer. It has been demonstrated that this deposition step leads to changes in the buried oxide stoichiometry, with evident oxygen loss, causing conversion into suboxide phases and probable oxide network modification. 693 mV of iVoc and 930  $\mu$ s of lifetime were reached on a p-type FZ wafer with a simple stack of wet-SiO<sub>x</sub>\(p<sup>+</sup>)  $\mu$ c-Si:H\SiN<sub>x</sub>:H in the as-deposited state, with no annealing step. The comparable passivation between Cz and Monocast wafers showed that it is of interest to keep studying the integration of passivating contacts on this kind of wafers.

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#### Author contribution statement

Anatole Desthieux: main author and contributor to this work. Made all the experiments apart from the XPS measurements. Wrote the article. Jorge Posada: made all the chemistry related to the cleaning of the samples, and chemical oxides. Davina Messou: XPS measurements and analyses. Barbara Bazer-Bachi, Cédric Broussillou and Gilles Goaer: industrial expertise, scientific feedbacks on the impact of TOPCon integration in industry. Processing and preparation of Monocast substrates. Muriel Bouttemy: XPS expertise for data analysis. Pierre-Philipe Grand: expertise on silicon solar cell processes. Etienne Drahi: expertise on silicon solar cell processes. Project leader and a lot of feedbacks on characterization techniques, and other investigations. Pere Roca i Cabarrocas: expertise on plasma and vacuum processes. Helped analyse all the data, and mostly the spectroscopic ellipsometry measurements which lead to the XPS investigation.

#### References

- F. Feldmann, M. Bivour, C. Reichel, M. Hermle, S.W. Glunz, Sol. Energy Mater. Sol. Cells **120**, 270 (2014)
- R. Peibst, U. Romer, K.R. Hofmann, B. Lim, T.F. Wietler, J. Krugener, N.-P. Harder, R. Brendel, IEEE J. Photovolt. 4, 841 (2014)
- M.K. Stodolny, J. Anker, B.L.J. Geerligs, G.J.M. Janssen, B.W.H. van de Loo, J. Melskens, R. Santbergen, O. Isabella, J. Schmitz, M. Lenes, J.-M. Luchies, W.M.M. Kessels, I. Romijn, Energy Proc. **124**, 635 (2017)
- A. Ingenito, G. Nogay, Q. Jeangros, E. Rucavado, C. Allebé, S. Eswara, N. Valle, T. Wirtz, J. Horzel, T. Koida, M. Morales-Masis, M. Despeisse, F.-J. Haug, P. Löper, C. Ballif, Nat. Energy 3, 800 (2018)
- N. Nandakumar, J. Rodriguez, T. Kluge, T. Grosse, D. Landgraf, N. Balaji, M. Esber, P. Padhamnath, S. Duttagupta, in *IEEE 7th WCPEC, Waikoloa Village, HI, USA, 2018*, p. 4
- Photowatt, http://www.photowatt.com/produits/modules/ pw2450f-crystal-advanced
- 7. G.E. Jellison, F.A. Modine, Appl. Phys. Lett. 69, 371 (1996)
- A.S. Kale, W. Nemeth, S.P. Harvey, M. Page, D.L. Young, S. Agarwal, P. Stradins, Sol. Energy Mater. Solar Cells 185, 270 (2018)
- F. Feldmann, M. Simon, M. Bivour, C. Reichel, M. Hermle, S.W. Glunz, Sol. Energy Mater. Sol. Cells 131, 100 (2014)
- A. Morisset, R. Cabal, B. Grange, C. Marchat, J. Alvarez, M.-E. Gueunier-Farret, S. Dubois, J.-P. Kleider, Sol. Energy Mater. Solar Cells **200**, 109912 (2019)

- H. Kim, S. Bae, K.-S. Ji, S.M. Kim, J.W. Yang, C.H. Lee, K.D. Lee, S. Kim, Y. Kang, H.-S. Lee, D. Kim, Appl. Surf. Sci. 409, 140 (2017)
- 12. D.A.G. Bruggeman, Ann. Phys. 416, 636 (1935)
- M. Lehmann, N. Valle, J. Horzel, A. Pshenova, P. Wyss, M. Döbeli, M. Despeisse, S. Eswara, T. Wirtz, Q. Jeangros,

A. Hessler-Wyser, F.-J. Haug, A. Ingenito, C. Ballif, Sol. Energy Mater. Sol. Cells **200**, 110018 (2019)

 H. Angermann, J. Rappich, in *Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells*, edited by W.G.J.H. M. van Sark, L. Korte, F. Roca (Springer, Berlin, 2012), pp. 45–94

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