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Gate-Tunable Negative Differential Resistance in Next-Generation Ge Nanodevices and their Performance Metrics

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In the quest to push the contemporary scientific boundaries in nanoelectronics, Ge is considered a key building block extending device performances, delivering enhanced functionalities. In this work, we embed a quasi-1D monocrystalline and monolithic Al-Ge-Al nanowire heterostructure into a novel field-effect transistor architecture capable of combining Ge based electronics with an electrostatically tunable negative differential resistance (NDR) distinctly observable at room temperature. In this regard, we present a detailed study of the key metrics of negative differential resistance in Ge. Most notably, we demonstrate a highly efficient and low-footprint platform paving the way for potential applications such as fast switching multi-valued logic devices, static memory cells or high-frequency oscillators all implemented in one fully Complementary metal–oxide–semiconductor (CMOS) compatible Al-Ge based device platform.

1. Introduction

The continuous down-scaling of the Si-based planar metal oxide field effect transistor (MOSFET) integrated circuit technology has been the main driving force to reduce size, power consumption and cost of modern microelectronic devices.^[1] However, despite the continuous advancement in nanofabrication and electronic device geometries, fundamental scaling limits will restrict further performance enhancement.^[2] At the same time, emerging distributed computing paradigms such as the Internet of Things^[3] are placing extraordinarily stringent constraints on hardware performance, forcing a shift of research efforts towards the integration of new materials, processes and device architectures.^{[4],[5],[6]} In this context, low-dimensional Ge structures such as nanomembranes^{[7],[8]} and vapor-liquid-solid^[9] (VLS) grown nanowires^{[10],[11]} (NWs), exhibiting unique electrical^{[4],[12],[13]} and optical^{[14],[15],[16]} properties departing from their bulk counterparts, are considered key building blocks in a “More than Moore” approach extending device performances beyond the limits imposed by miniaturization.^{[17],[18]} In this respect, a highly interesting transport mechanism is the transferred electron effect, enabling negative differential resistance (NDR) following the Ridley-Watkins-Hilsum theory.^[19] Also known as the Gunn-effect in GaAs^[20] and GaN nanocrystals,^[21] this effect is based on applying sufficiently high electric fields, resulting in electrons from the energetically favorable conduction band valley, characterized by a low effective mass, being transferred to a heavy mass valley nearby.^[20] The unique NDR characteristic can be exploited for novel logic gates providing significant advantage over conventional logic devices in one or more performance metrics such as area, speed, or power.^[22] In this respect, the monostable-

bistable transition logic element (MOBILE) is a functional logic gate employing two NDR devices connected in series and was shown to perform both NAND and NOR operations.^{[22],[23]} However, the monolithic integration of large foot-print group III-V based NDR devices on a Si platform is challenging.^[23] Despite pioneering work demonstrating NDR in Ge, until now, the observation was either limited to low temperatures,^{[24],[25]} impracticable for typical applications, the exploitation of the transient behavior of surface traps,^[26] plasmon-induced hot electron injection^[27] or required careful preconditioning of the Ge surface.^[28]

In this work, we systematically analyze NDR at room temperature based on the transferred electron effect in Al-Ge-Al NW heterostructures. The reproducible and reliable device fabrication combined with a low foot-print and stable device operation enabled the extraction of the key parameters of NDR in Ge providing a significant step towards potential applications such as fast switching logic circuits, static memory cells, or high-frequency oscillators.^[22]

2. Results and Discussion

To investigate the electrical properties, nominally intrinsic VLS-grown Ge NWs with diameters between 25 nm and 50 nm were integrated into field-effect transistors (FETs) (see **Figure 1a**). For device fabrication, a thermally induced exchange reaction between the NWs and Al contact pads was used to achieve Ge segments contacted by self-aligned, single crystalline Al NW leads^[29] with atomically sharp and flat heterojunctions (see **Figure 1b**).^[30] Due to the large surface to volume ratio, adsorbates and surface states have a significant impact on the electrical characteristics of NW-based devices.^{[31],[32]} Consequently, to ensure reliable and reproducible electrical measurements, the NWs were enwrapped in a protective 20 nm thick atomic layer deposition (ALD) grown Al₂O₃-insulator shell.^[26] Without contact annealing, the device characteristic appeared to be a statistic process resulting in either p-type, n-type or ambipolar

operation (see Figure S1). This variability can be attributed to a residual (and patchy) parasitic oxide-layer on the contact area between the Ge NW and the Al pads that is indeed known to have a significant influence on the transport properties of nanoscale devices.^[33] Figure 1c shows the unique atomically sharp interface of the fabricated Al-Ge-Al longitudinal NW heterostructure based on high angle annular dark field (HAADF) scanning transmission electron microscopy (STEM). The image confirms that our NW axis is oriented along the $\langle 111 \rangle$ crystallographic direction. Further, details regarding the fabrication process of our Al-Ge-Al NW heterostructures used for other electronic applications, as well as physical analysis, i.e. high-resolution transmission electron microscopy (HR-TEM) and energy dispersive X-ray spectroscopy investigations can be found in the work of Kral *et al.*^[30] and El Hajraoui *et al.*^[34] Using the Si substrate as global back-gate, nominally intrinsic Ge NWs enwrapped in a protective Al₂O₃-shell exhibit a slight ambipolar behavior, with predominant hole transport for negative gate voltages (see dashed curves in Figure 1d).^[11] It has been noted that surface doping,^[35] due to acceptor-like traps, results in a shift of the energy band structure throughout the entire NW cross-section, causing predominant p-type behavior in nominally intrinsic Ge NWs.^{[36],[31]} Exemplary for the evaluation of more than 25 similar heterostructure devices (see Figure S2), the transfer characteristic shown in Figure 1a reveals that even applying ultra-low drain voltages down to $V_D = 1 \text{ mV}$, an I_{ON}/I_{OFF} ratio increasing from 10^4 to 10^5 can be achieved with our devices while only showing a slight ambipolar behavior. Assuming thermionic emission, the Schottky barrier height (SBH) for electrons of the Al-Ge junction can be obtained from the slope of the activation energy plot of $\ln(J/T^2)$ versus $1000/T$ at various bias voltages (see supporting information). The thereof calculated SBH in the sub-threshold region of the electron-dominated transport was estimated to be $220 \pm 25 \text{ meV}$, which is in perfect agreement with the theoretical value of 200 meV for bulk Al-Ge Schottky junctions.^[37] To improve the electrostatic control of the Ge channel and to decrease the absolute value of the applied gate voltage, an omega-shaped top-gate was fabricated atop the Al₂O₃ coated Ge channel. In this

configuration, the I_{ON}/I_{OFF} ratio could be improved by one order of magnitude to $10^5 - 10^6$ (solid lines shown in Figure 1d). Additional transfer curves of heterostructure devices with channel lengths of $L_{Ge} = 150 \text{ nm}$ to 759 nm are shown in Figure S6. For our top-gated devices an enhanced sub-threshold swing of $SS = d[\log(I_D)] / dV_{TG} = 300 \pm 50 \text{ mV/decade}$ was extracted.

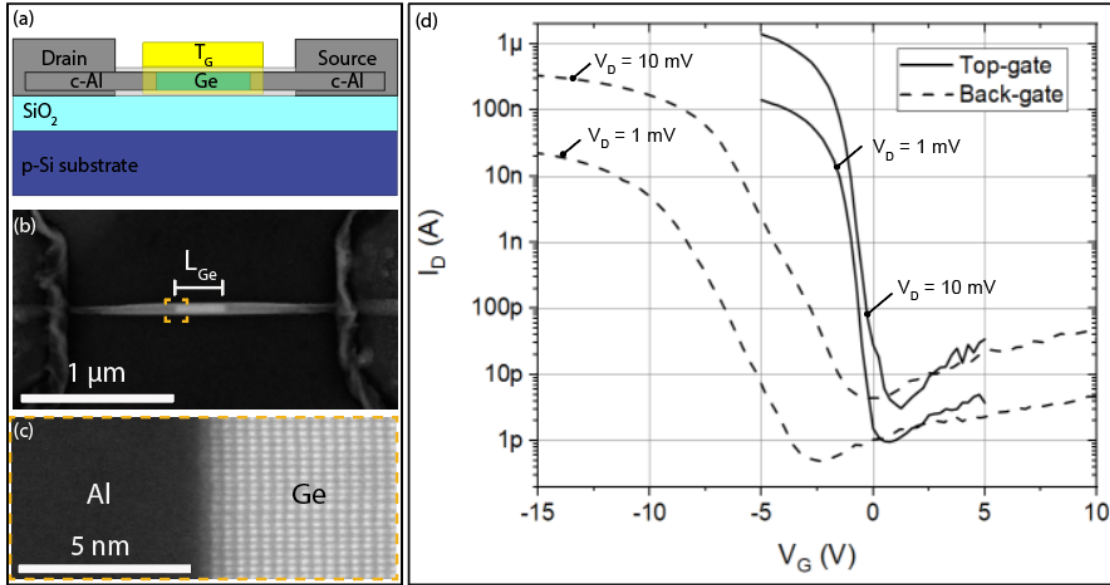


Figure 1. (a) Schematic of a top-gated Al-Ge-Al NW heterostructure device. (b) SEM image before top-gate fabrication. The length and diameter of the actual Ge channel is $L_{Ge} = 256 \text{ nm}$ and $d_{NW} = 30 \text{ nm}$, respectively. (c) HAADFSTEM image showing a zoom-in at the Al-Ge interface region. (d) Transfer characteristic of a back-gated (dashed lines) and top-gated (solid lines) Ge NW FET device for a bias of $V_D = 1 \text{ mV}$ and 10 mV .

To gain access to the electron-dominated transport regime positive back-gate voltages of $V_{BG} = 5 \text{ V}$, 15 V and 30 V were applied. The corresponding I/V measurements were recorded by linearly increasing V_D while monitoring I_D (**Figure 2a**). For a positive V_{BG} an unambiguous observation NDR is given with progressive enhancement for higher V_{BG} . The respective band diagram is shown in the left inset of Figure 2a. For V_{BG} ranging between 5 V and 30 V , the increasing downward band bending results in a thinning of the barrier width for electron

injection at the source electrode and thus in an enhancement of electron injection through Fowler-Nordheim tunneling. In this configuration, we interpret the observations as follows. Hot electrons are scattered from the energetically favorable conduction band valley, characterized by a low effective mass to a heavy mass valley nearby.^[20] Although the Γ -point minimum in Ge is energetically closer to the L-point minimum, the coupling constant between $\langle 111 \rangle$ and $\langle 000 \rangle$ minima is significantly lower than between $\langle 111 \rangle$ and $\langle 100 \rangle$ minima.^[38] Consequently, as schematically illustrated in the right inset of Figure 2a, the transferred electron effect in Ge is most likely to apply for the L-point and Δ -point minima of the $\langle 111 \rangle$ and $\langle 100 \rangle$ subbands of the conduction band with the respective effective masses of $m_{L,t}^* = 0.082 m_0$ and $m_{\Delta,t}^* = 0.288 m_0$.^[38] Figure S7 shows a series of consecutive I/V measurements to demonstrate the stability of the NDR operation of our devices. Figure S8 shows the current density at V_{Peak} (J_{Peak}) of 24 similar Al-Ge-Al heterostructures in dependence of the Ge channel length and the NW diameter. With an average J_{Peak} of 2 kA/cm^2 at room-temperature, our devices reveal a three orders of magnitude higher value compared to larger footprint Ni/n+ Ge diodes^[24] even when operating at $T = 230 \text{ K}$. According to the nature of the transferred electron effect, measuring the I/V characteristic for $V_{BG} = 30 \text{ V}$, sweeping V_D first from -4 V to 4 V and back from 4 V to -4 V , results in the NDR being observed in the negative branch of the I/V characteristic (see Figure S9).^[39] Further, Figure 2b shows the dependence of the electric field ($E_{Transfer}$) required to carry out the proposed electron transfer from the $\langle 111 \rangle$ to the $\langle 100 \rangle$ minima. The evaluation of Al-Ge-Al devices with L_{Ge} between 150 nm and $2 \mu\text{m}$ revealed that a relatively constant electric field of $E_{Transfer} = 1 \times 10^4 \text{ V/cm}$ appeared to be sufficient for devices with $L_{Ge} > 1 \mu\text{m}$ to initiate the electron transfer. However, with ever shorter Ge channel lengths, an exponential increase of the electric field close to the break-down field for bulk Ge with $E_C = 100 \text{ kV/cm}$ ^[40] was found. As schematically illustrated in the inset of Figure 2b, this finding is consistent with hot electrons releasing their energy gained from the electric field by creating electron-hole pairs, which are subsequently split by the increasing electric field. The continuation of this process results in highly energetic

electrons and thus an increased rate of electrons being transferred to the $\langle 100 \rangle$ valley. However, with ever decreasing channel lengths, the acceleration path is decreasing, resulting in less energetic electrons. Thus, a significantly higher $E_{Transfer}$ is required to initiate NDR in short channel devices.

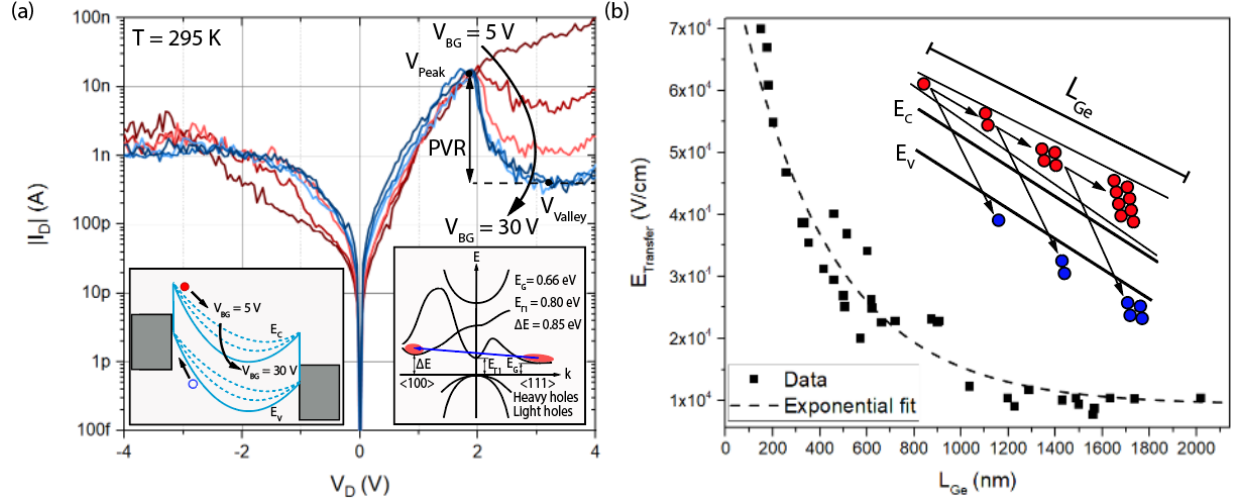


Figure 2. (a) Semi-logarithmic I/V characteristic recorded for different back-gate voltages between $V_{BG} = 5 V$ and $30 V$ of an Al-Ge-Al NW heterostructure device with $L_{Ge} = 450 nm$. Shifting the device characteristic to n-type operation, clear signatures of NDR are visible. The left inset shows the respective schematic band diagram for applying a positive V_D to the heterostructure device, resulting electrons being injected by a combination of Fowler-Nordheim tunneling and thermionic emission. The large bias voltage and the downward bent bands enable the electron transfer from the L- to the Δ -valley. The right inset shows the band diagram of Ge with the electric field induced electron transfer from the $\langle 111 \rangle$ valley into the $\langle 100 \rangle$ valley enabling NDR.^[41] (b) $E_{Transfer}$ as a function of the Ge channel length L_{Ge} . The inset is showing a schematic illustration of charge carrier scattering in the Ge channel.

Next, we focus on the NDR figure-of-merit (FOM) parameters of our Al-Ge-Al NW heterostructures. **Figure 3** shows a semi-logarithmic I/V characteristic showing the NDR recorded for a fixed back-gate voltage of $V_{BG} = 30 V$. The most important parameter of NDR

devices is their peak-to-valley ratio (PVR), which is defined by $PVR = I(V_{Peak}) / I(V_{Valley})$. We found that with respect to the back-gate voltage, the PVR in our devices can be tuned. In conjunction with an increased accumulation of electrons, tuning the back-gate voltage from $V_{BG} = 10 V$ to $30 V$ dramatically increases the PVR from 2.5 to 27.5. Figure 3a shows the temperature dependence of the NDR of a heterostructure device with $L_{Ge} = 450 nm$, recorded at a constant back-gate voltage of $V_{BG} = 30 V$ for $T = 200 K$, $295 K$ and $350 K$. Associated with an increase of the scattering mean free path at low temperatures, the respective PVR values are 220, 25 and 5, accordingly. An evaluation of the average PVR of 10 heterostructure devices for temperatures between $T = 200 K$ and $350 K$ is supplied in the inset. Linearly fitting the data, the PVR decreases with a rate of $0.46 / K$ within the given temperature range. We want to note that the relatively high back-gate voltage of $V_{BG} = 30 V$ can be reduced to $5 V$ if a top-gate architecture is used (see Figure S10). As a substantially larger PVR is desirable for oscillators and diverse digital applications,^{[22],[23]} we have systematically evaluated the PVR as a function of the Ge channel length (Figure 3b) and the NW diameter (Figure 3c) of 21 heterostructure devices. In comparison with Ge quantum dot tunneling diodes^[42], Si and Si/SiGe resonant interband tunneling diodes,^{[43],[44]} the room-temperature PVR of our best performing devices is approximately a factor 20 larger.

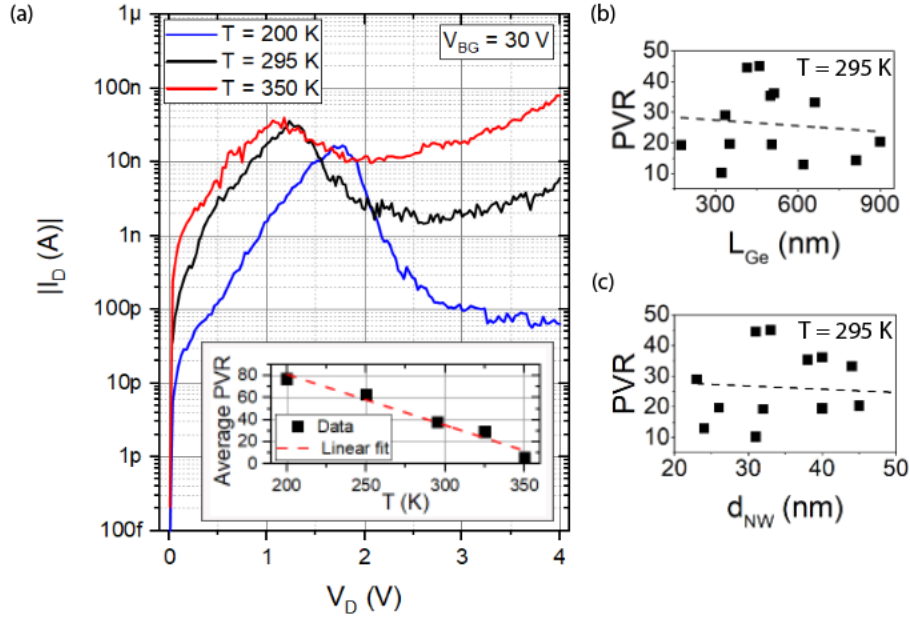


Figure 3. (a) Semi-logarithmic I/V characteristic recorded for $V_{BG} = 30 V$ an Al-Ge-Al NW heterostructure device with $L_{Ge} = 450 nm$, recorded at $T = 200 K$, $295 K$ and $350 K$. The respective PVR values are 220, 25 and 5. The inset shows the average PVR based on the measurement of 10 devices measured at temperatures between $T = 200 K$ and $350 K$. Dependence of the PVR on (b) the Ge channel length NW and (c) the NW diameter.

With respect to scalability of the NDR in Ge, we found that heterostructure devices with Ge channel lengths $L_{Ge} < 100 nm$ showed no signs of NDR, which we attribute to the quasi-ballistic^[45] nature of such short channel Ge heterostructure devices. Consequently, the best performing devices were found to have $d_{NW} = 20 nm$ and $L_{Ge} = 150 nm$ just over three times longer than the scattering mean free path in our Ge NWs.^[45] Compared to the state of the art NDR devices our optimal device structure exhibit an ultra-small footprint, As shown in **Figure 4a**, embedded in the proposed top-gate architecture, these devices can be operated with $V_{Peak} = 0.9 V$ and $V_{Valley} = 1.2 V$, still providing a PVR of 4.5 at $T = 295 K$. As shown in Figure 4b and 4c respectively, a longer Ge channel increases the device resistance, shifting V_{Peak} and V_{Valley} to higher voltages. With respect to oscillator devices, NDR metrics such as $V_{Span} = (V_{Peak} - V_{Valley})$, the conductance slope ($|G_{Slope}|$), characterizing the abruptness of the NDR region and the extent

of the voltage plateau ($V_{Plateau}$), defined as the width of the valley, are of utmost importance.^[22]

V_{Span} is used to characterize the voltage window of the NDR region, with a larger voltage being preferred for oscillator applications, as the maximum oscillation power is proportional to V_{Span} .^[23] We found a maximum of $V_{Span} = 2.2 V$ for devices with $L_{Ge} = 900 nm$. In conjunction with both, $|G_{Slope}|$ and $V_{Plateau}$ being significantly larger for long Ge channels, heterostructure devices with $L_{Ge} > 700 nm$, seem to be better suited for oscillator applications.

The performed systematic benchmark of the NDR metrics in Al-Ge-Al NW heterostructures embedded in FET architectures, revealed their high potential as a low-footprint platform enabling both, logic and oscillator applications. Highly relevant for a cost-efficient practical implementation our approach presented here can be transferred into a fully CMOS compatible Al-Ge based device platform paving the way for an unprecedented realization of circuits based on monolithically integrated gate controlled NDR transistors with conventional MOSFETs.

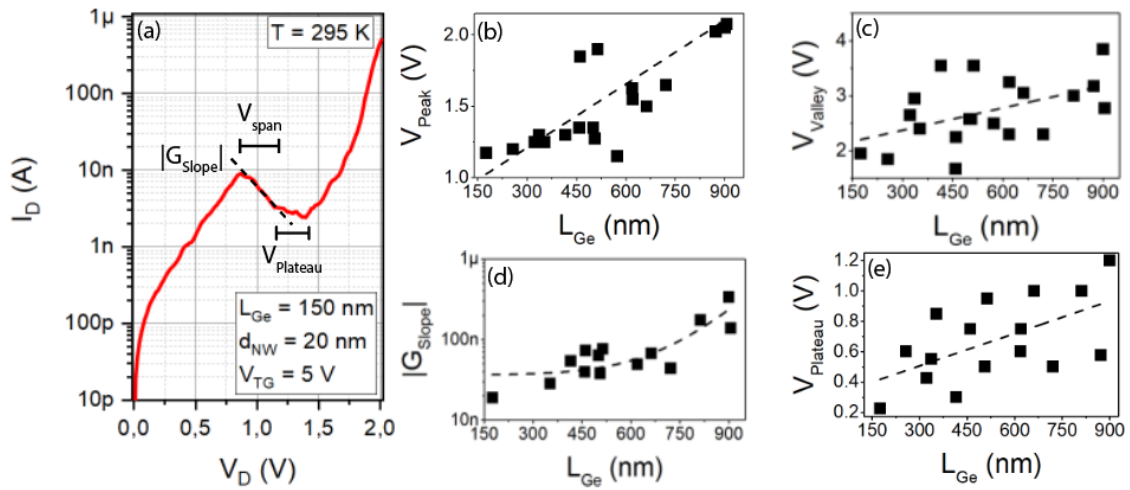


Figure 4. (a) Semi-logarithmic I/V characteristic of an ultra-scaled top-gated Al-Ge-Al heterostructure NDR device with $L_{Ge} = 150 nm$ and $d_{NW} = 20 nm$ recorded for a top-gate voltage of $V_{TG} = 5 V$. The important NDR FOM metrics $|G_{Slope}|$, V_{Span} and $V_{Plateau}$ are indicated. (b-e) Dependence of V_{Peak} , V_{Valley} , $|G_{Slope}|$ and V_{Span} on L_{Ge} . The data were measured at ambient conditions at a temperature of $T = 295 K$.

3. Conclusion

In conclusion, we have thoroughly analyzed the NDR effect in Al-Ge-Al NW heterostructures embedded in back- and top-gated FET architectures. Based on the evaluation, the NDR FOM metrics could be extracted. Most notably, the versatility of our Al-Ge-Al NW heterostructures provides a platform extending Ge based electronics with NDR applications such as fast switching logic circuits, static memory cells, or high-frequency oscillators. In this respect, we believe that our investigations provide a significant step towards a beyond CMOS approach enabling functional diversification and alternative computing for the post-Si era.

4. Methods

Synthesis of Ge NWs:

The used Ge NWs were grown on Si (111) substrates using the VLS growth mechanism with mono-germane (GeH_4 , 2% diluted in He) as precursor and a 2 nm thick sputtered Au layer as the 1D growth promoting catalyst and seed. The actual growth was performed using a low-pressure hot wall CVD chamber at a total pressure of 50 mbar and a gas flow of 100 sccm for both, the precursor gas and H_2 as carrier gas. After stabilizing the pressure and precursor gas flow, the temperature was ramped up at a rate of 110 K/min to the target temperature of 614 K. The rather high growth temperature ensures uniform catalyst diameter and good NW epitaxy. After a 10 min nucleation phase, the temperature was lowered to 573 K. Typical growth duration of 60 min results in 8 μm long NWs and uniform diameters of about 30 nm. Subsequently to

the growth, the NWs were uniformly coated with a 20 nm thick Al₂O₃-shell^[27] by ALD at a temperature of 473 K.

Device fabrication:

The starting materials were VLS grown Ge NWs with diameters of approximately 30 nm coated with 20 nm high-k Al₂O₃ using ALD. The passivated Ge NWs were drop-casted onto a 100 nm thick thermally grown SiO₂ layer atop of a 500 μm thick highly p-doped Si substrate acting as a common back-gate. The Ge NWs were contacted via Al pads fabricated by electron beam lithography, 100 nm Al sputter deposition and lift-off techniques. A successive thermally induced exchange reaction by rapid thermal annealing at a temperature of $T = 624$ K in forming-gas atmosphere initiates the substitution of Ge by Al.^{[30],[34],[45]} Facilitating this heterostructure formation scheme allows the integration of single-crystalline monolithic Al-Ge-Al NW heterostructures with tunable channel lengths in a back-gated FET architecture. Further, omega-shaped Ti/Au top-gates were fabricated using a combination of electron beam lithography, Ti/Au electron beam evaporation (8 nm Ti, 125 nm Au, deposition rate 0.05 nm/s, base pressure 2×10^{-7} mbar), and lift-off techniques.

High-resolution HAADF STEM:

HAADF STEM was performed on Al-Ge-Al NW heterostructures fabricated on 40 nm thick Si₃N₄ membranes^{[46],[47]} using a probe-corrected FEI Titan Themis, working at 200 kV. The Al-Ge interface in the shown images lies along the [112] direction of observation of the Ge crystal.

Electrical characterization:

The electrical measurements were carried out at room temperature and ambient conditions using a combination of a semiconductor analyzer (HP 4156B) and a probe station. To minimize the influence of ambient light as well as electromagnetic fields, the probe station is placed in a dark

box. Temperature dependent measurements (200 - 350 K) were performed in vacuum at a background pressure of approximately 5×10^{-6} mbar using a cryogenic probe station (LakeShore PS-100) and a semiconductor analyzer (Keysight B1500A).

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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R.B. and M.S. contributed equally to this work. M.S. and M.G.B. performed the device fabrication. R.B., M.S. and K.E. conducted the measurements. M.S. wrote the manuscript. M.A.L. and M.I.H. carried out the TEM characterization and analysis. A.L. provided helpful feedback and commented on the manuscript. W.M.W conceived the project and contributed essentially to the experimental design. All authors analyzed the results and helped shape the research and manuscript. The authors gratefully acknowledge financial support by the Austrian Science Fund (FWF): project No.: P29729-N27. The authors further thank the Center for Micro- and Nanostructures for providing the cleanroom facilities.

Conflict of Interest

The authors declare no conflict of interest.

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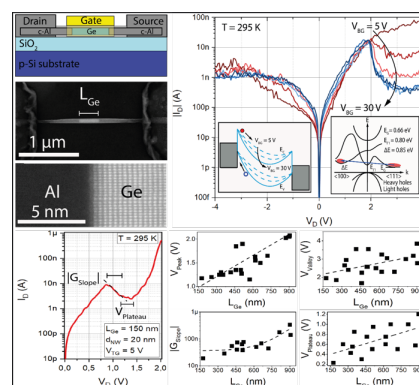
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Nanoscale Ge is considered a key building block extending device performances, delivering enhanced functionalities. Here, a highly efficient and low-footprint architecture comprising doping-free Ge and monocrystalline Al nanowire contacts revealing a strong and reproducible electrostatically tunable negative differential resistance (NDR) at room temperature is demonstrated. Most notably, a systematic study of the key performance metrics of NDR is presented.

*Raphael Böckle, Masiar Sistani, Kilian Eysin, Maximilian G. Bartmann, Minh Anh Luong, Martien I. den Hertog, Alois Lugstein and, Walter M. Weber**

Gate-Tunable Negative Differential Resistance in Next-Generation Ge Nanodevices and their Performance Metrics



Supporting Information

Gate-Tunable Negative Differential Resistance in Next-Generation Ge Nanodevices and their Performance Metrics

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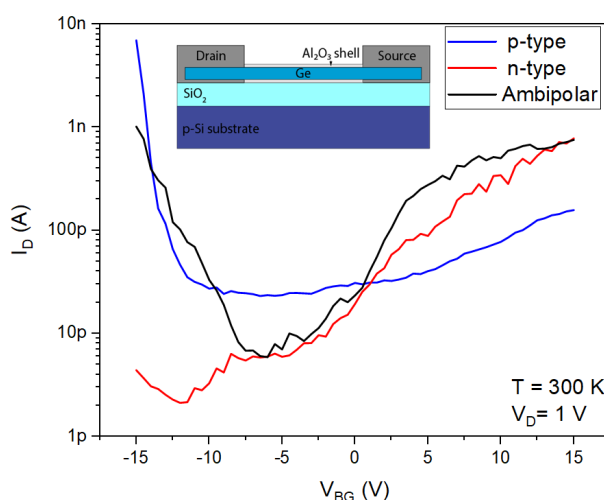


Figure S1: Transfer characteristics of Al-Ge-Al NW heterostructures prior to the thermally induced Al-Ge exchange. Presumably, different contact properties after fabrication resulted in a statistic distribution of p-type, n-type and ambipolar behavior. Based on the evaluation of 45 devices, the statistical distribution for p-type, n-type, and ambipolar behavior was 70%, 23% and 7% respectively. The inset shows a schematic of the device architecture.

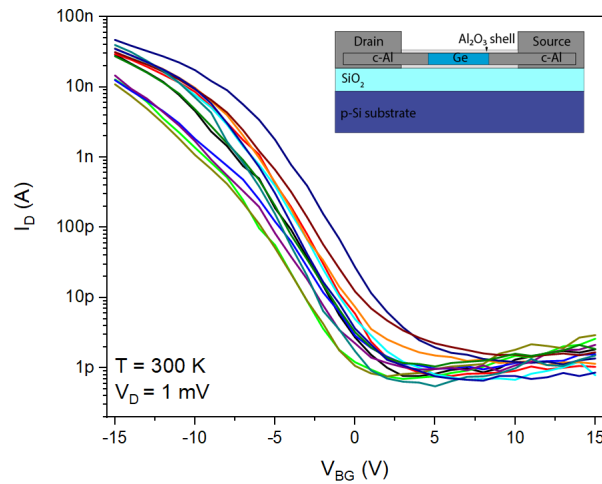


Figure S2: Transfer characteristics of back-gated Al-Ge-Al NW heterostructures with channel lengths between $L_{Ge} = 1.1 \mu m$ and $1.8 \mu m$ and diameters of $d_{NW} = 30 nm$ after the thermally induced Al-Ge exchange. Due to the contact modifications by annealing, all devices revealed a p-type behavior. The inset shows a schematic of the device architecture.

Determination of the Schottky barrier height for electrons:

To determine the Schottky barrier height for electrons, temperature dependent I/V measurements for $V_{BG} = 10 V$ (sub-threshold region of the electron-dominated current) were performed on an Al-Ge-Al heterostructure device enwrapped in a $20 nm$ thick Al_2O_3 -shell with a diameter of $d_{NW} = 30 nm$ and a channel length of $L_{Ge} = 500 nm$ (see Figure S3).

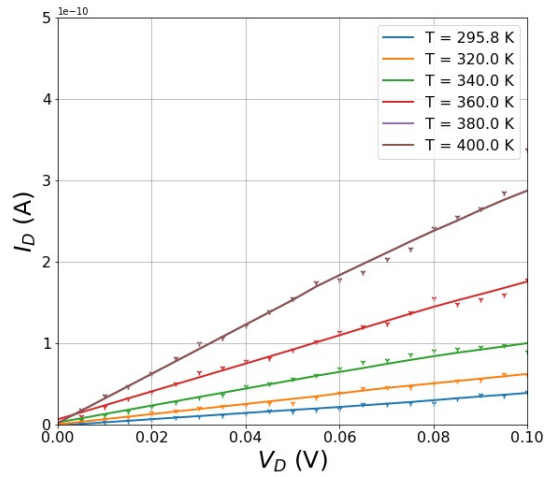


Figure S3. I/V measurements for $V_{BG} = 10$ V recorded in the temperature range between $T = 295.8$ K and 400 K of an Al-Ge-Al heterostructure device with a diameter of $d_{NW} = 30$ nm and a channel length of $L_{Ge} = 500$ nm. The data were interpolated using a first order Savitzky-Golay filter (solid lines).

As the Al-Ge-Al heterostructure can be electronically modeled as two back-to-back Schottky diodes, the Schottky barrier height can be extracted using the thermionic emission theory, which is valid for barrier heights much larger than $k_B T$, and small bias voltages to avoid barrier lowering and thus significant tunneling currents. The thermionic emission current over the barrier is described by $J_{TE} = A^* T^2 \exp\left(\frac{-q\phi_{SB}}{k_B T}\right)$, with A^* being the effective Richardson constant. Without knowing the exact value of the Richardson constant the barrier height can be extracted by measuring the I/V characteristics at different temperatures and reformulating the previous equation to: $\ln\left(\frac{J_{TE}}{T^2}\right) = \frac{-q\phi_{SB}}{k_B T} + \ln(A^*)$. Thus, by plotting $\ln\left(\frac{J_{TE}}{T^2}\right)$ as a function of $1000/T$ (i.e. Richardson plot) for a specific bias voltage V_D the barrier height can be extracted from the slope of a linear fit, as shown in Figure S4.

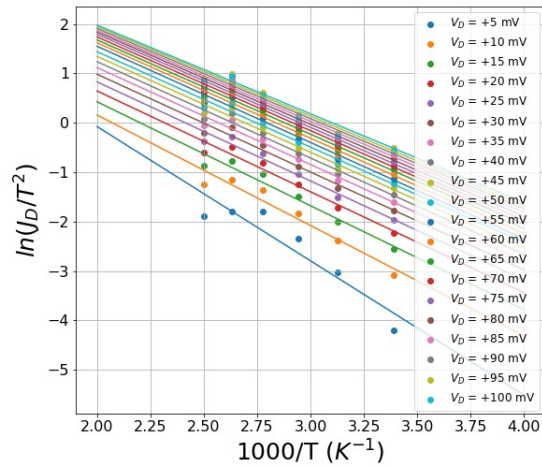


Figure S4. Richardson plots at bias voltages ranging from 0 V to 100 mV . The barrier height was extracted from the slope of the linear fits.

The barrier heights $q\phi_{SB}$ are calculated from the Richardson plots and are plotted as a function of the respective bias voltages as shown in Figure S5. Extrapolation of the data points to 0 V of several Al-Ge-Al heterostructures with similar structural sizes result in an effective barrier height of $220 \pm 25 \text{ meV}$, which is in good agreement with the theoretical value of 200 meV for bulk Al-Ge Schottky junctions.

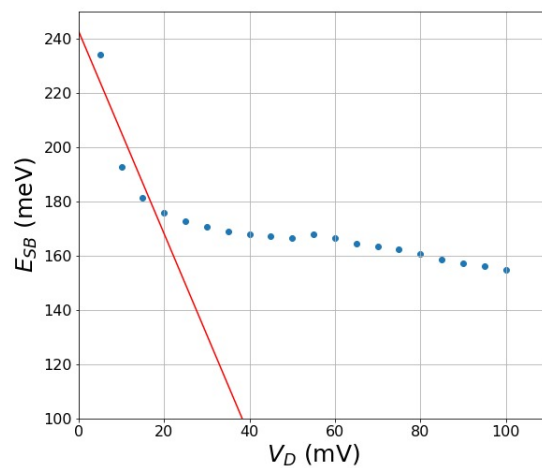


Figure S5. Estimated Schottky barrier height as function of the applied bias. The effective Schottky barrier at 0 V bias can be extracted by extrapolation of the data points at higher bias voltages.

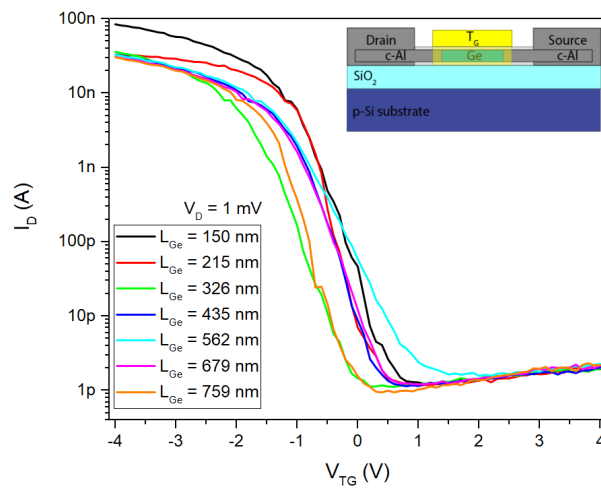


Figure S6: Transfer characteristics of top-gated Al-Ge-Al NW heterostructures with channel lengths between $L_{Ge} = 150 \text{ nm}$ and 759 nm and diameters of $d_{NW} = 30 \text{ nm}$ after the thermally induced Al-Ge exchange.

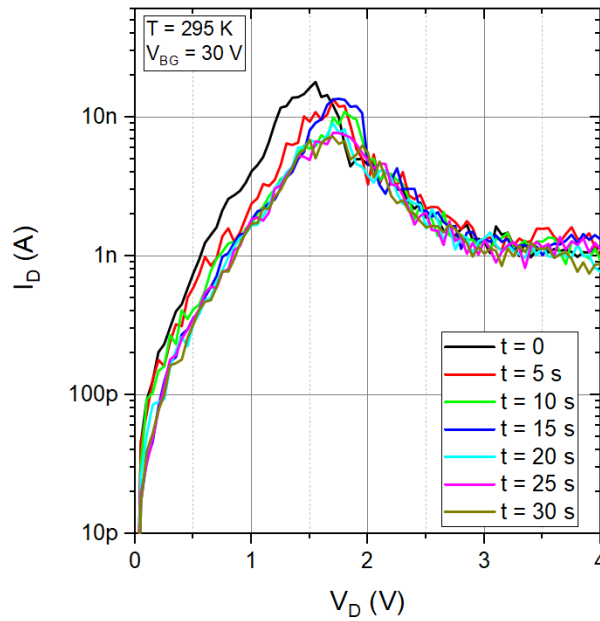


Figure S7: Progression of consecutive I/V recordings of an Al-Ge-Al NW heterostructure with $L_{Ge} = 662 \text{ nm}$ recorded for $V_{BG} = 30 \text{ V}$ to show the device stability. The sweep rate was set to 0.25 V/s and the delay time between the measurements was set to 5 s .

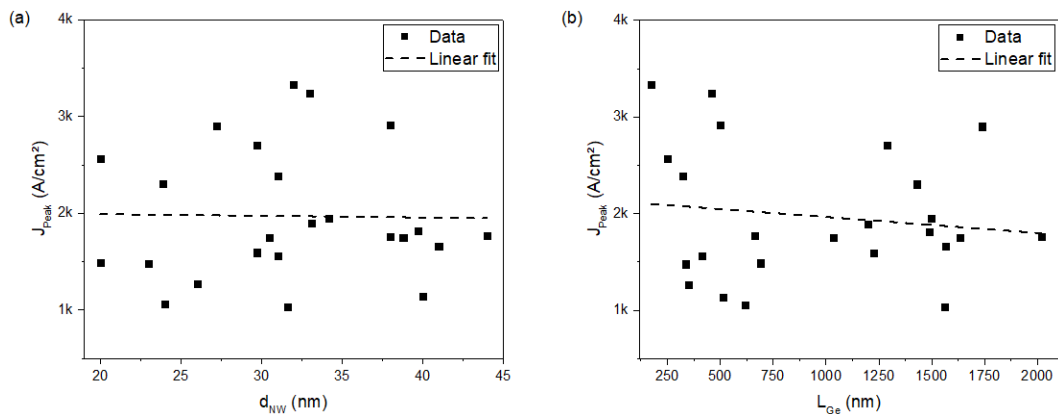


Figure S8: Current density J_{Peak} at V_{Peak} of 24 Al-Ge-Al NW heterostructure devices evaluated depending on (a) the diameter and (b) the Ge segment length.

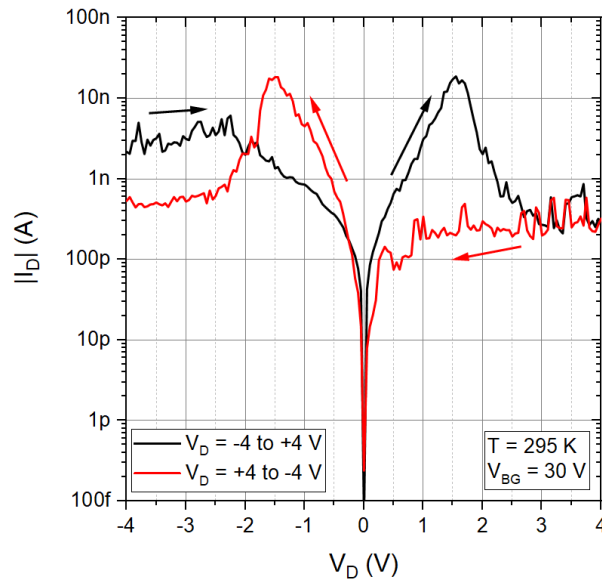


Figure S9: Semi-logarithmic I/V characteristic recorded for $V_{BG} = 30$ V of an Al-Ge-Al NW heterostructure device with $L_{Ge} = 460$ nm, sweeping V_D first from -4 V to 4 V (black) and back from 4 V to -4 V (red).

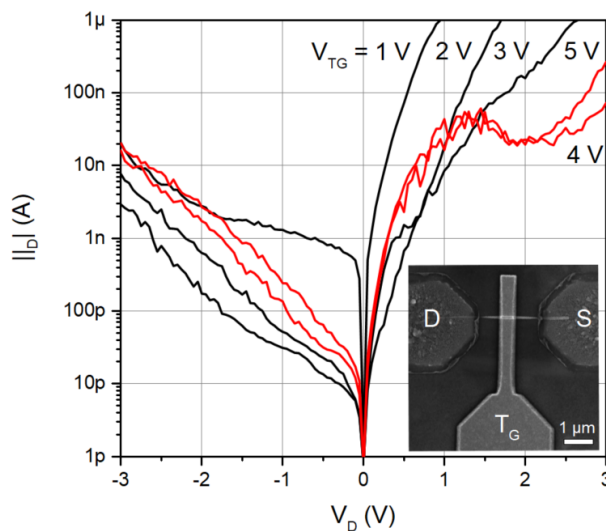


Figure S10. Semi-logarithmic I/V characteristic recorded for different top-gate voltages between $V_{TG} = 1$ V and 5 V in 1 V steps of an Al-Ge-Al NW heterostructure device with $L_{Ge} = 450$ nm. The voltage sweep was executed from -3 V to 3 V. Shifting the device characteristic to n-type operation, clear signatures of NDR are visible for a top-gate voltage of $V_{TG} = 4$ V and 5 V. A SEM image of the device is shown in the inset.