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# Optimized Buffer Stack with Carbon-Doping for Performance Improvement of GaN HEMTs

Ajay Shanbhag<sup>1</sup>, Sruthi M P<sup>1</sup>, Farid Medjdoub<sup>2</sup>, Anjan Chakravorty<sup>1</sup>, Nandita DasGupta<sup>1</sup>, and Amitava DasGupta<sup>1</sup>

<sup>1</sup>Department of Electrical Engineering, Indian Institute of Technology Madras, India

<sup>2</sup>IEMN-CNRS, Institute of Electronics, Microelectronics and Nanotechnology, France

**Abstract**—This paper focuses on determining an optimized value of carbon-doping level in the buffer and corresponding channel thickness to improve the performance of GaN HEMTs in terms of subthreshold slope ( $SS$ ), breakdown voltage ( $V_{BD}$ ) and transit frequency ( $f_t$ ). With the increase in carbon-doping, we observe improvements in  $SS$  and  $V_{BD}$  while the  $f_t$  is reduced. However, as the channel thickness increases above a certain thickness, no significant impact of carbon-doping is observed on the characteristics. TCAD simulation is calibrated using experimental data for a device with carbon-doping level of  $3 \times 10^{18} \text{ cm}^{-3}$  in the buffer with channel thickness of 500 nm. Using the calibrated device in TCAD, the carbon-doping level and channel thickness are varied to see the effects on different parameters. We observed that an optimized channel thickness of 200 nm with carbon-doping level of  $1 \times 10^{19} \text{ cm}^{-3}$  in the buffer yields the best results in terms of  $V_{BD}$  and  $f_t$ .

**Index Terms**—AlGaIn-GaN HEMTs, AlInN-GaN HEMTs, breakdown voltage, buffer traps, C-doping, subthreshold slope, transit frequency.

## I. INTRODUCTION

WITH the increased demand for high power and RF applications, Gallium Nitride (GaN) high electron mobility transistors (HEMTs) have proven to be an ideal choice due to its material properties such as large band gap, high electron mobility, saturation velocity, and electric field strength, along with superior thermal conductivity [1]–[4]. As the unintentional dopants incorporated during the epitaxial growth of GaN, the buffer leakage increases, causing a deterioration of the device breakdown voltage ( $V_{BD}$ ), subthreshold slope ( $SS$ ), and on-off current ratio ( $I_{ON}/I_{OFF}$ ). Various techniques have been reported to reduce the buffer leakage, such as intentional doping with acceptor traps such as Iron ( $Fe$ ) or Carbon ( $C$ ) [5], and growing a high bandgap material such as AlGaIn below the channel layer to ensure a back-barrier [6]. We initially focus on reducing the buffer leakage and increase buffer resistivity by intentionally doping carbon in the buffer layer. Although this helps in increasing ( $V_{BD}$ ), the introduction of such traps degrades the dynamic performance of the device due to the slow emission process of the traps, thereby reducing the transit frequency ( $f_t$ ). Hence, an

optimized buffer stack is necessary to get the best performance from the device.

Few works have reported the use of C-doping in GaN as a deep acceptor [7], [8]. In contrast, a few others have reported it to be self-compensating in nature since C acts as a deep acceptor and a shallow donor as it can replace Ga or N and acts as either donor or acceptor, respectively [9], [10]. However, if we consider an equal concentration of acceptor and donor, no current collapse should be observed unlike experimental data. Additionally, the energy required for C to replace Ga in GaN is high, resulting in a higher probability of it behaving like an acceptor trap [8]. Hence in the TCAD simulations, we have considered 80% self-compensating behavior.

As carbon acts as deep acceptor trap centers in GaN, it can potentially trap the electrons from 2-dimensional electron gas (2DEG) in the buffer, degrading the DC characteristics significantly. A sudden change in the drain and/or gate voltage in pulsed applications generates a sudden change in the electric field at the gate edge on the drain side, resulting in enough energy for the electrons from the channel to go deeper into the buffer and get trapped in the trap sites. As these are deep traps, the emission process is slow, resulting in trapping-related dispersion effects such as drain-lag, gate-lag, and current collapse [11], [12]. Hence, it is a common practice to dope carbon away from the channel region to prevent the trapping of electrons from the 2DEG. However, if the C-doped layer is far away from the channel region, the buffer leakage increases. Hence, the channel region must not be very thick. Also, the carbon concentration in the C-doped layer is an important parameter to control the leakage current. If the carbon concentration is very high, the dynamic performance of the device will degrade due to its slow detrapping process. Hence, an optimum carbon concentration and channel thickness are required to obtain the best results.

Although studies on the impact of  $V_{BD}$  with C-doping are available in the literature [13], a detailed and systematic research on the interplay of the channel thickness and C-doping on the device performance is missing. In this paper, we focus on the variation of channel thickness and C-doping level and compare its impact on  $SS$ ,  $I_{ON}/I_{OFF}$ ,  $V_{BD}$ , and  $f_t$ . Section II discusses the TCAD simulation framework including the detailed analysis of channel thickness and C-doping level on the device performance. Obtained results are analyzed in detail with appropriate physical insights. Finally, we conclude in Section III.

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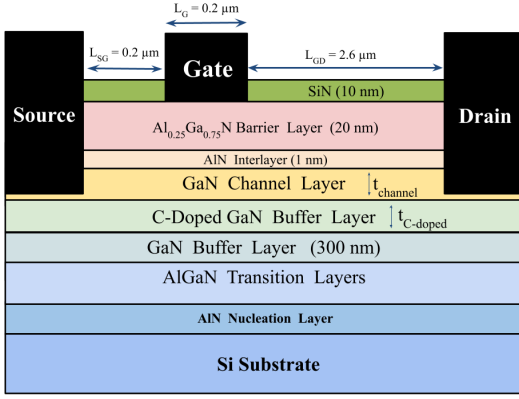


Fig. 1: Cross-sectional view of the device under investigation.

## II. TCAD SIMULATION FRAMEWORK AND RESULTS

### A. Device structure and models

The GaN HEMT structure as shown in Fig. 1 is calibrated in TCAD using Synopsys Sentaurus [14]. The device consists of  $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$  heterostructure on a silicon (Si) substrate. The epilayer structure includes 20 nm  $\text{AlGaN}$  barrier layer, 1 nm  $\text{AlN}$  spacer, 500 nm thick GaN channel ( $t_{\text{channel}}$ ), 200 nm C-doped layer ( $t_{\text{C-doped}}$ ) with concentration of  $3 \times 10^{18} \text{ cm}^{-3}$ , and 300 nm GaN buffer layer followed by  $\text{AlGaN}$  transition layer and Si substrate. The HEMT is fabricated with gate length ( $L_G$ ) of  $0.2 \mu\text{m}$ , source-gate spacing ( $L_{SG}$ ) of  $0.2 \mu\text{m}$ , gate-drain spacing ( $L_{GD}$ ) of  $2.6 \mu\text{m}$ , and  $50 \mu\text{m}$  gate width. To account for the surface states, surface donor traps are considered at an energy level of  $E_C - 0.5 \text{ eV}$  with a density of  $3 \times 10^{13} \text{ cm}^{-2}$  as reported in [15]. Using deep level transient spectroscopy (DLTS) and low-frequency  $Y_{22}$  parameters, it has been shown that the C-traps have an activation energy of around 0.9 eV from the valence band [16] and the same has been used in simulation with a concentration of  $3 \times 10^{18} \text{ cm}^{-3}$ , and electron and hole capture cross-section as  $10^{-18} \text{ cm}^2$  and  $10^{-14} \text{ cm}^2$  respectively in the C-doped layer. To account for the self compensating nature, shallow donors with a concentration of  $2.4 \times 10^{18} \text{ cm}^{-3}$  with activation energy of 0.2 eV from conduction band with similar electron and hole capture cross-section have been considered. In other regions of the device, acceptor traps with a concentration of  $5 \times 10^{16} \text{ cm}^{-3}$  and activation energy of 0.47 eV from the conduction band are considered. The unintentional n-doping in GaN is considered to be in the order of  $10^{15} \text{ cm}^{-3}$ . The work function of the gate Schottky contact is set to 4.4 eV. To make the source and drain contacts ohmic, non-local electron tunneling at the contacts is activated by setting a work function of 4 eV. The polarization model is used to consider the polarization charges at the interfaces. The drift-diffusion equations are solved along with various physical models, e.g., doping and field-dependent mobility, mobility degradation due to traps, thermionic emission, Shockley-Read-Hall (SRH) recombination, and Fermi statistics. According to Chynoweth law, the impact ionization model has been considered in GaN to account for the carrier generation. The breakdown voltage

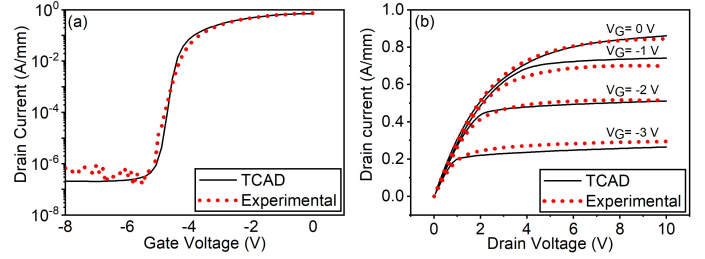


Fig. 2: Comparison of results obtained from experimental data and TCAD simulations: (a) transfer and (b) output characteristics of GaN HEMT.

TABLE I: Reference Device Metric Values

Device Metric	Value
Maximum drain current ( $I_{Dmax}$ )	45.38 mA
On-off current ratio ( $I_{ON}/I_{OFF}$ )	$4.6 \times 10^6$
Subthreshold slope ( $SS$ )	128 mV/dec
Breakdown voltage ( $V_{BD}$ )	119 V
Transit frequency ( $f_t$ )	43.8 GHz

is measured as the OFF-state drain current of 1mA/mm with gate-source voltage ( $V_{GS}$ ) being set at -8V.

Using the models and parameter values mentioned so far, detailed TCAD simulation is carried out. Corresponding simulation results along with the experimental data for the transfer and output characteristics are shown in Fig. 2. We observe that the on-state current and leakage current have been well-calibrated. For this reference device, the observed values of  $SS$ ,  $I_{ON}/I_{OFF}$ ,  $V_{BD}$ , and  $f_t$  are shown in Table I. In the following subsections, we attempt to optimize C-doping level in the GaN buffer layer and  $t_{\text{channel}}$  by comparing the resulting metrics with those of the reference device.

### B. Channel thickness variation with fixed C-doping level

From the reference parameter values of the device, we varied  $t_{\text{channel}}$  keeping C-doping level fixed at  $3 \times 10^{18} \text{ cm}^{-3}$ . Corresponding variations of device metric are presented in Fig. 3 and Table II. On reducing the channel thickness from 500 nm to 35 nm, the ratio  $I_{ON}/I_{OFF}$  increases by six orders,  $SS$  reduces by 45 mV/dec, and  $V_{BD}$  increases more than four times, while the  $f_t$  is reduced by half as compared to those of the reference device. As the channel region thickness is reduced, the C-GaN layer comes closer

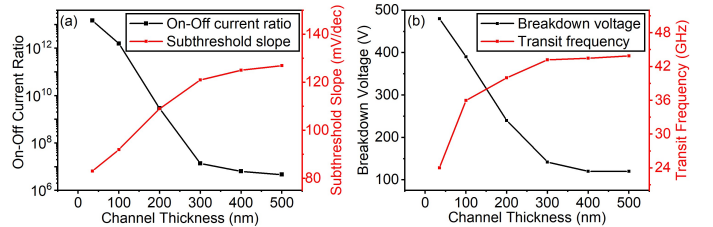


Fig. 3: TCAD results showing variation of channel thickness on: (a) On-off current ratio and subthreshold slope, (b) breakdown voltage and transit frequency, by keeping C-doping at  $3 \times 10^{18} \text{ cm}^{-3}$  in C-doped GaN buffer.

TABLE II: Device Metric Values with C-doping in C-GaN as  $3 \times 10^{18} \text{ cm}^{-3}$

$t_{channel}$ (nm)	$I_{Dmax}$ (mA)	$I_{ON}/I_{OFF}$	$SS$ (mV/dec)	$V_{BD}$ (V)	$f_t$ (GHz)
35	36	$1.45 \times 10^{13}$	83	480	24.5
100	42.5	$1.57 \times 10^{12}$	92	389	36
200	44.9	$2.9 \times 10^9$	109	239	40
300	45.2	$1.38 \times 10^7$	121	142	43.2
400	45.3	$6.35 \times 10^6$	125.57	119	43.5
500	45.4	$4.65 \times 10^6$	127	119	43.8

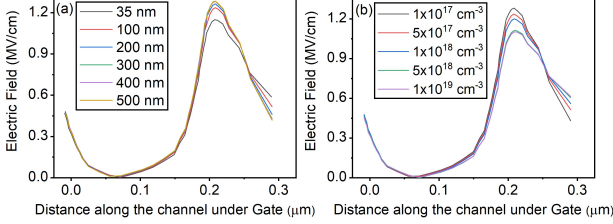


Fig. 4: TCAD results showing the effect on electric field profile below the gate from drain to source by varying (a) channel thickness with C-Doping level of  $3 \times 10^{18} \text{ cm}^{-3}$  in C-GaN and (b) C-doping level with channel thickness of 35 nm.

to the channel, causing a significant reduction of the off-state leakage. This results in higher  $I_{ON}/I_{OFF}$  and better  $SS$ . Additionally, we observe electric field relaxation at the drain side of the gate edge as shown in Fig. 4a due to which  $V_{BD}$  increases. However, the trapping increases significantly, reducing the overall  $f_t$ . From the simulated data, we see that as the channel thickness increases above 300 nm, there is no significant change in device metrics compared to those of the reference device. This is due to a reduced interaction of C-dopants with  $2DEG$  leading to an insignificant effect on the electric field as observed in Fig. 4a. However, with a reduction in channel thickness, we see a few metrics are significantly improved while a few others are deteriorated. Hence, we attempt to optimize the C-doping level in the C-doped GaN buffer layer in order to obtain an optimum performance concerning all the metrics.

### C. C-doping level variation for different channel thickness

To find an optimum buffer design with C-doped GaN, we varied the C-doping level in the C-doped GaN buffer for various channel thicknesses. Fig. 5 shows the effects of C-doping levels for various channel thicknesses on different metrics.

Table III shows the results of different metrics for  $t_{channel}$  of 35 nm. It is observed that if the C-doping level is below

TABLE III: Device Metric Values with  $t_{channel}$  as 35 nm

C-Doping in C-GaN ( $\text{cm}^{-3}$ )	$I_{Dmax}$ (mA)	$I_{ON}/I_{OFF}$	$SS$ (mV/dec)	$V_{BD}$ (V)	$f_t$ (GHz)
$1 \times 10^{17}$	45.4	$3.8 \times 10^4$	279	55	44.3
$5 \times 10^{17}$	42.5	$1.1 \times 10^{12}$	105	205	38
$1 \times 10^{18}$	39	$1.1 \times 10^{12}$	84.6	317	33.7
$5 \times 10^{18}$	34	$1.1 \times 10^{12}$	80.4	550	12.9
$1 \times 10^{19}$	30	$1.1 \times 10^{12}$	79	670	12

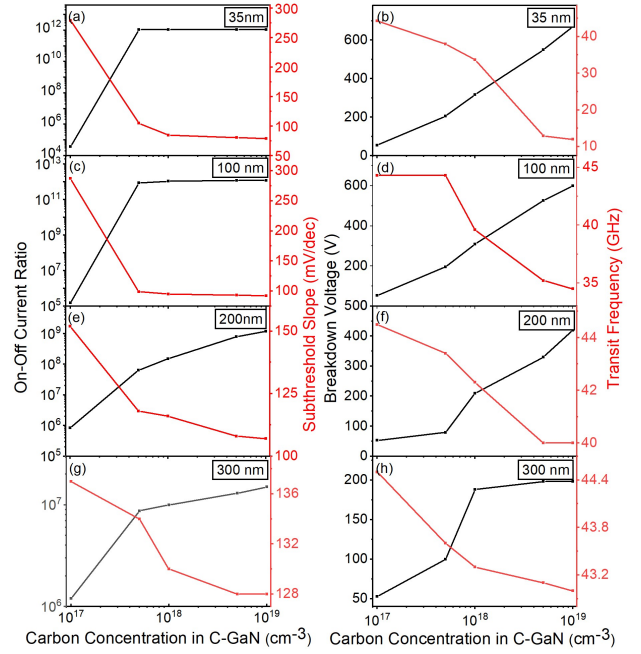


Fig. 5: TCAD results showing the effects of variation of C-doping in C-GaN buffer for different channel thickness on different device metrics such as on-off current ratio, subthreshold slope, breakdown voltage, and transit frequency.

$5 \times 10^{17} \text{ cm}^{-3}$ ,  $SS$ ,  $I_{ON}/I_{OFF}$ , and  $V_{BD}$  deteriorate significantly, due to the self-compensating nature of carbon in GaN. As a result, we see an overall reduced concentration of acceptor traps causing an increase in the leakage current. However, as the C-concentration is increased above  $5 \times 10^{17} \text{ cm}^{-3}$ , we see improvements in  $SS$  and  $V_{BD}$ , but with a significant fall in  $f_t$ . Due to a reduction in the leakage current as the C-doping level increases and effective confinement of  $2DEG$  in the channel region, we find improvements in  $SS$  and  $I_{ON}/I_{OFF}$ . Additionally due to the electric field relaxation at the drain side of gate edge as shown in Fig. 4b,  $V_{BD}$  improves significantly. But as C-GaN layer is very close to the channel, trapping effect is higher, causing the  $f_t$  to fall. Hence, considering  $t_{channel}$  as 35 nm, it is suggested that C-doping level should be around  $5 \times 10^{17} \text{ cm}^{-3}$  in order to ensure the best performance. However, the value of  $f_t$  is fairly low and the improvement in  $V_{BD}$  is only by a factor of 2 with this configuration. Hence, it is decided to increase  $t_{channel}$  to 100 nm. Table IV shows the resulting metric values.

We observe a similar trend at a lower C-doping level. However, as the doping level increases, the % reduction in  $f_t$  is less compared to the previous case, as the electrons from

TABLE IV: Device Metric Values with  $t_{channel}$  as 100 nm

C-Doping in C-GaN ( $\text{cm}^{-3}$ )	$I_{Dmax}$ (mA)	$I_{ON}/I_{OFF}$	$SS$ (mV/dec)	$V_{BD}$ (V)	$f_t$ (GHz)
$1 \times 10^{17}$	45.5	$1.5 \times 10^5$	287	53	44.3
$5 \times 10^{17}$	44	$8.8 \times 10^{11}$	98.9	196	44.3
$1 \times 10^{18}$	43.4	$1.2 \times 10^{12}$	95.5	309	39.7
$5 \times 10^{18}$	42.2	$1.2 \times 10^{12}$	93.2	527	35.2
$1 \times 10^{19}$	42	$1.2 \times 10^{12}$	92	600	34.4



TABLE V: Device Metric Values with  $t_{channel}$  as 200 nm

C-Doping in C-GaN ( $\text{cm}^{-3}$ )	$I_{Dmax}$ (mA)	$I_{ON}/I_{OFF}$	$SS$ (mV/dec)	$V_{BD}$ (V)	$f_t$ (GHz)
$1 \times 10^{17}$	45.5	$8.54 \times 10^5$	152	53	44.5
$5 \times 10^{17}$	45	$6.4 \times 10^7$	118	78.9	43.34
$1 \times 10^{18}$	44.9	$1.5 \times 10^8$	116	209	42.3
$5 \times 10^{18}$	44.78	$8.1 \times 10^8$	116	330	40
$1 \times 10^{19}$	44.8	$1.2 \times 10^9$	107	440	40

TABLE VI: Device Metric Values with  $t_{channel}$  as 300 nm

C-Doping in C-GaN ( $\text{cm}^{-3}$ )	$I_{Dmax}$ (mA)	$I_{ON}/I_{OFF}$	$SS$ (mV/dec)	$V_{BD}$ (V)	$f_t$ (GHz)
$1 \times 10^{17}$	45.5	$1.2 \times 10^6$	137	53	44.5
$5 \times 10^{17}$	45.3	$8.7 \times 10^6$	134	100	43.6
$1 \times 10^{18}$	45.3	$1 \times 10^7$	130	188	43.3
$5 \times 10^{18}$	45.3	$1.3 \times 10^7$	128	198	43.1
$1 \times 10^{19}$	45.3	$1.5 \times 10^7$	128	198	43

the 2DEG are no longer very close to the C-GaN layer. From the simulation results, we suggest an optimum buffer design considering  $t_{channel}$  as 100 nm and C-doping level of the order of  $1 \times 10^{18} \text{ cm}^{-3}$  in C-GaN layer to achieve the best results in terms of all the metrics. Though  $V_{BD}$  increases with higher C-doping, it is not preferred for pulsed applications, as it would lead to high current collapse. For this optimized device,  $V_{BD}$  is around 2.5 times higher than the reference device, while  $f_t$  is only marginally reduced. Next we simulated devices with  $t_{channel}$  of 200 nm to achieve a higher  $V_{BD}$  value without compensating for  $f_t$ . The corresponding results for the various metrics are shown in Table V.

In this case, as C-doping level is increased, an even lesser impact on  $f_t$  is observed. On the other hand, there is a four-fold increase in  $V_{BD}$  over that of the reference device. Also, the leakage current has decreased by 3 orders of magnitude. Considering  $t_{channel}$  as 200 nm and C-doping of around  $1 \times 10^{19} \text{ cm}^{-3}$  in C-GaN buffer, we obtain the best performance in all the metrics. Simulation was also carried out by considering  $t_{channel}$  fixed at 300 nm and varying the C-doping level to improve the metrics. Table VI shows the corresponding results where we find hardly any change in  $f_t$  with increase in C-doping. However,  $V_{BD}$  has increased to only around 1.6 times that of the reference device for a C-doping concentration of  $5 \times 10^{18} \text{ cm}^{-3}$  or higher. The simulation results for  $t_{channel}$  of 400 nm and 500 nm with varied C-doping levels in C-GaN do not show any significant improvement over the reference device metrics. Hence they are not shown here.

### III. CONCLUSION

We have studied the interplay between GaN channel thickness and carbon-doping in the GaN buffer layer using calibrated TCAD simulations. It is observed that as the channel thickness decreases keeping the C-doping unaltered,  $SS$ ,  $I_{ON}/I_{OFF}$ , and  $V_{BD}$  improve while  $f_t$  reduces significantly. We observe a similar trend as the C-doping level is increased for a given channel thickness. Additionally, as the channel layer thickness increases beyond 300 nm, no significant impact on the above parameters is observed. Analyzing the results obtained from simulations, we obtain an optimized structure with 200 nm GaN channel thickness followed by a C-GaN

layer with a C-doping of  $1 \times 10^{19} \text{ cm}^{-3}$ . The resulting device yields the best values for  $SS$ ,  $I_{ON}/I_{OFF}$ ,  $V_{BD}$ , and  $f_t$ . Our study and corresponding findings can help the industries and academia to obtain an optimum set of buffer layer parameters during its epitaxial growth to extract the best results for both high power and RF applications.

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