GaN-based power devices: Physics, reliability, and perspectives

Matteo Meneghini, Carlo de Santi, Idriss Abid, Matteo Buffolo, Marcello Cioni, Riyaz Abdul Khadar, Luca Nela, Nicolò Zagni, Alessandro Chini, F Medjdoub, et al.

GaN-based power devices: physics, reliability and perspectives

Matteo Meneghini[1], Carlo De Santi[1], Idriss Abid[2], Matteo Buffolo[1] Marcello Cioni[5], Riyaz Abdul Khadar[3], Luca Nela[3], Nicolò Zagni[5], Alessandro Chini[5], Farid Medjdoub[2], Gaudenzio Meneghesso[1], Giovanni Verzellesi[4], Enrico Zanoni[1], Elison Matioli[3]

[1]*University of Padova, Department of Information Engineering, via Gradenigo 6/B, 35131 Padova, Italy*

[2]*IEMN (Institute of Electronics, Microelectronics and Nanotechnology), Avenue Poincaré, 59650 Villeneuve d'Ascq, France*

[3]*École Polytechnique Fédérale de Lausanne, ELD 012 (Bâtiment ELD), CH-1015 Lausanne*

[4]*University of Modena and Reggio Emilia, Dipartimento di Scienze e Metodi dell'Ingegneria, via Amendola 2 - Pad. Morselli, 42122 Reggio Emilia, Italy*

[5]*University of Modena and Reggio Emilia, Dipartimento di Ingegneria "Enzo Ferrari", Via P. Vivarelli, 10, 41125 Modena, Italy*

Abstract:

Over the last decade, gallium nitride has emerged as an excellent material for the fabrication of power devices. Among the semiconductors for which power devices are already available on the market, GaN has the widest energy gap, the largest critical field, the highest saturation velocity, thus representing an excellent material for the fabrication of high speed/high voltage components.

The presence of spontaneous and piezoelectric polarization allows to create a 2-dimensional electron gas, with high mobility and large channel density, in absence of any doping, thanks to the use of AlGaN/GaN heterostructures. This contributes to minimize resistive losses; at the same time, for GaN transistors switching losses are very low, thanks to the small parasitic capacitances

and switching charges. Device scaling and monolithic integration enable high frequency operation, with consequent advantages in terms of miniaturization.

For high power/high voltage operation, vertical device architectures are being proposed and investigated, and 3-dimensional structures – fin-shaped, trench-structured, nanowire-based – are demonstrating a great potential. Contrary to silicon, GaN is a relatively young material: trapping and degradation processes must be understood and described in detail, with the aim of optimizing device stability and reliability.

This tutorial paper describes the physics, technology and reliability of GaN-based power devices: in the first part of the article, starting from a discussion of the main properties of the material, the characteristics of lateral and vertical GaN transistors are discussed in detail, to provide guidance in this complex and interesting field. The second part of the paper focuses on trapping and reliability aspects: the physical origin of traps in GaN, and the main degradation mechanisms are discussed in detail. The wide set of referenced papers and the insight on the most relevant aspects gives the reader a comprehensive overview on present and next-generation GaN electronics.

1 Table of Contents

2 Introduction

Over the past decade, gallium nitride has emerged as an excellent material for the fabrication of power semiconductor devices. Thanks to the unique properties of GaN, diodes and transistors based on this material have excellent performance, compared to their silicon counterparts, and are expected to find wide application in the next-generation power converters. Owing to the flexibility and the energy efficiency of GaN-based power converters, the interest towards this technology is rapidly growing: the aim of this tutorial is to review the most relevant physical properties, the operating principles, the fabrication parameters, and the stability/reliability issues of GaN-based power transistors. For introductory purposes, we start summarizing the physical reasons why GaN transistors achieve a much better performance than the corresponding silicon devices, to help the reader understanding the unique advantages of this technology.

The properties of GaN devices allow the fabrication of high-efficiency (near or above 99 %) [1]–[5], kW-range power converters. Such converters can have switching frequencies above 1 MHz [6], [7], and – through proper design, integration and/or hybrid GaN/CMOS manufacturing – frequencies as high as 40-75 MHz can be reached [8], [9]. High frequency operation permits to substantially reduce the size and weight of inductors and capacitors, thus resulting in a compact converter design. Further innovation will come from the design of monolithically integrated all-GaN integrated circuits: specific platforms, such as GaN on silicon-on-insulator (SOI) can be used for the fabrication of fully integrated power converters, containing smart control, pulse width modulation (PWM) circuitry, dead time control and half bridge [10], [11]. Such solutions, that can be tailored for switching in the 1-10 MHz range, can reach very short turn on/off times, which are considerably smaller than in discrete gate drivers [11]. The availability of fast, small, efficient and light-weight power converters can be particularly beneficial in the fields of portable/consumer electronics, automotive, and avionics.

GaN is a wide-bandgap semiconductor, and has an energy-gap of 3.4 eV [12]. This allows GaN devices to be operated at extremely high temperatures, thus substantially increasing the maximum power density that can be dissipated on a device, or permitting the use of light and small heat sinks. Over the last decades, several report on high temperature and stable operation of GaN HEMTs have been published. Temperatures above 400-500 °C [13]–[15] have been reached and, for

selected InAlN/GaN devices, up to 900 °C [15]. Operation at high temperature is a first, substantial, advantage of GaN devices, compared to silicon-based Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), that are typically rated for maximum operating temperature of 125-150 °C.

A second advantage of GaN arises from its high breakdown field (3.3 MV/cm [12]), which is 11 times higher than that of silicon (0.3 MV/cm). The direct consequence of such high critical field is that for withstanding a given voltage, a layer of GaN can be 11 times thinner than its silicon counterpart, with consequent beneficial impact on resistivity. As a consequence, the use of GaN switches can substantially reduce the resistive losses in switching mode power supplies (SMPSs).

A third aspect to be considered is the high mobility of the channel: as will be discussed in the following sections, GaN transistors are typically heterostructure devices. A high mobility (up to 2000 cm/Vs [12]) channel can be obtained through the formation of a 2-dimensional electron gas (2DEG) at the heterointerface between the AlGaN barrier and the GaN channel layer. Such high mobility, along with the large saturation velocity (2.5×10^7 cm/s), further contributes to reduce the resistivity of the devices. FETs based on AlGaN/GaN heterostructures are usually referred to as high electron mobility transistors (HEMTs), or heterojunction field effect transistors (HFETs).

At present, GaN devices are commercially available, and several products have been proposed, in three main voltage ranges: a) low/mid-voltage ($V_{DS,max}$<200 V) devices find application in dc-dc power converters, motor drives, wireless power transfer, LiDAR and pulsed power applications, solar micro-inverters, class-D audio amplifiers, robotics, and synchronous rectification. Such devices can have on-resistances below 2 mΩ (for drain currents up to 90 A) [16], or up to 100-200 mΩ (for operating currents in the range 0.5-5 A), depending on the final application [17], [18]. b) high voltage ($V_{DS,max}$ up to 650 V), that find application in telecommunication servers, industrial converters, photovoltaic inverters, servo motor control [19], lighting applications, power adapters, converters for consumer electronics [20], class D amplifiers [21], datacenter SMPS [22], [23]. c) devices with ultra-high voltage ($V_{DS,max}$ above 1 kV). At present, no kV-range transistor based on GaN is commercially available. The commercial transistors with highest voltage rating have a maximum voltage of 900 V, and are expected to find application in data communication systems, industrial application, motor control, and photovoltaic inverters. As will be discussed in the article, several research papers demonstrated the feasibility of GaN transistors with breakdown voltages

above 1 kV [24]–[26], and proposed possible fabrication processes to target this voltage range. kV-range GaN transistors will compete with SiC-based devices, in the industrial, automotive and photovoltaic application environments.

As will be described in detail in the paper, current GaN devices have typically a lateral layout. Several key aspects related to device design, fabrication and performance must be discussed in detail, to understand how the performance of the transistors can be optimized through careful device design: this will be done extensively in the following sections of this paper. For introductory purposes, we remind here that in a HEMT current flows between drain and source through a 2-dimensional electron gas (2DEG), which is formed at the heterojunction between an AlGaN barrier and a GaN layer. Figure 1 (a) reports the schematic structure of a GaN-based HEMT, showing the main layers that constitute the structure. Power GaN devices are typically grown on a silicon substrate, to minimize cost and maximize yield. Growing GaN on a silicon substrate is particularly complicated, due to: a) the large mismatch of the in-plane thermal expansion coefficient (2.6×10^{-6} K^{-1} for Si and 5.59×10^{-6} K^{-1} for GaN [27]), that may lead to cracking of the GaN layer during the cooling-phase after the epitaxial growth; b) the large lattice mismatch (around 16 % for Si(111)) [28], [29], that may result in the propagation of dislocations through the gallium nitride epitaxial layers, with consequent defect generation. A careful optimization of the buffer is needed in order to limit the propagation of such defects towards the 2DEG region; Figure 1 (b) reports a cross sectional SEM image of the epitaxial layers of a GaN-based transistor. As can be noticed, the use of a step-graded buffer in combination with an AlN nucleation layer is used to release the strain and prevent the formation/propagation of dislocations.

The lateral structure described in Figure 1 may have some limitations, when extremely high breakdown voltages and/or power densities are targeted. First, in a lateral transistor the breakdown voltage scales with the gate-drain spacing. Thus, devices with a high breakdown voltage can be fabricated, but will be more resistive and will use a wider semiconductor area, thus resulting in a higher device cost. Second, the density of electrons in the 2DEG can be strongly influenced by surface charges: for this reason, the performance of the final devices is strongly dependent on the process and backend. To solve the limitation of GaN lateral devices, vertical device structures are currently being explored and investigated, in line with what has been done with silicon and silicon carbide components. In a vertical device (see a schematic structure in Figure 1 (c)), current flows

through the bulk of the material, thus allowing high current and power densities. The density of electrons in the channel is modulated through a metal-oxide-semiconductor (MOS) stack, and a p-type body is usually employed to shift the threshold voltage towards more positive values. The breakdown voltage of a vertical GaN transistor depends on the thickness of the lightly-doped drift region, and not on the size and area of the device as in a lateral transistor. Vertical GaN devices represent the latest development in GaN technology, and the reader will find interest in the related concepts and applications, described in this paper.

As for every technology, there are some physical processes that may limit the performance and the reliability of GaN devices. The on-resistance of a GaN transistors (and thus the density of electrons in the 2DEG) strongly depends on the intrinsic (spontaneous and piezoelectric) polarization charges of GaN, as well as on the presence of charges trapped at surface states (e.g. in the passivation layer or at the interface between the passivation layer and the AlGaN barrier) or in buffer states. For this reason, it is of fundamental importance to know and manage the surface- and buffer-related trapping phenomena that may limit the dynamic performance of GaN transistors, leading to a recoverable increase in on-resistance (dynamic-Ron problem). Trapping in the epitaxial layers and/or at the gate-stack may result in positive- or negative-bias threshold instability (PBTI or NBTI), and the related processes must be investigated and understood to be able to fabricate fast and reliable devices.

Finally, GaN-based transistors are operated at field, temperature, and frequency levels which are unimaginable for conventional silicon devices. Electric fields can be in excess of 3 MV/cm, and channel temperatures can be above 300 °C during operation, if lightweight heat dissipators are used. Such conditions may favor sudden or time-dependent breakdown phenomena, leading to the failure of the devices. Furthermore, operation at high frequencies may exacerbate the degradation processes related to hard switching events. For this reason, it is of utmost importance to understand the degradation processes of GaN power devices, and to identify ways and strategies for improving the robustness of the components.

This tutorial paper presents a detailed overview on the physics, performance and reliability of GaN-based power devices. In the Section 3-5, the properties and physical parameters of gallium nitride are discussed, to help the reader understanding the unique advantages offered by GaN compared to other semiconductors. The main figures of merit (FOM) for high speed (Johnson

FOM) and high power (Baliga FOM) devices are also introduced. Finally, the properties of AlGaN/GaN heterostructures, and the related band diagrams are described in detail, and first-order formulas for the calculation of sheet electron charge and threshold voltage are introduced. In Section 6, the properties, structure and characteristics of lateral GaN devices are discussed. Specific details is given to the various approaches for normally-off operation, to the main device parameters, and to the optimization of the buffer. A perspective on AlN-based devices and on possible strategies to increase the breakdown voltage is given, also by discussing devices with local substrate removal. Section 7 deals with GaN vertical devices. First, the advantages of vertical GaN transistors are described. Attention is then given to the choice of the substrate (GaN-on-GaN vs GaN-on-Si) for vertical device manufacturing. Then, the various vertical device architectures are discussed and compared, in terms of performance and structural parameters. In Section 8, the stability of GaN devices is analyzed in detail. Specific focus is given to the role of surface traps, barrier traps and buffer traps in modifying the main device parameters, to present a clear overview of the topic. A complete overview of the dominant defects and deep levels in GaN is given in Section 8.1, to provide an exhaustive view of the problem. Finally, Section 9 describes the most relevant degradation processes that can limit the lifetime of GaN-based transistors. Specific attention will be towards the degradation mechanisms induced by exposure to off-state stress, semi-on state regime, and on-state degradation (with focus on gate reliability for p-GaN and insulated-gate devices).

Through a pedagogical approach, this paper helps the reader understanding the advantages of GaN technology, and getting familiar with the main performance, design, and reliability aspects.

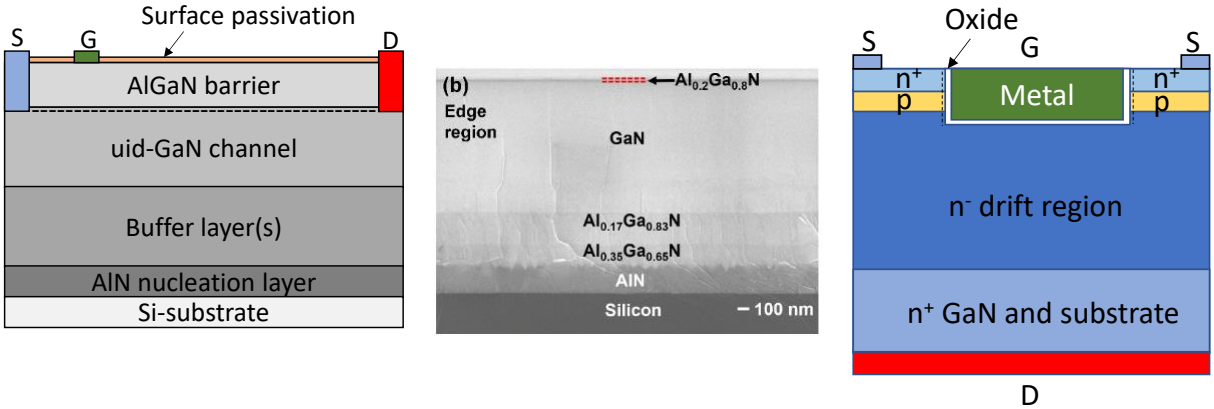


Figure 1: (a) schematic representation of the structure of a lateral GaN high-electron mobility transistor (HEMT). The main layers constituting the structure are shown, as well as the three contacts of source (S), gate (G) and drain (D). (b) Cross-sectional SEM images of the epi-structure of GaN HEMT on silicon. Reprinted from "Strain Analysis of GaN HEMTs on (111) Silicon with Two Transitional $Al_xGa_{1-x}N$ Layers", Y. Cai et al., https://doi.org/10.3390/ma11101968, licensed under CC BY 4.0 (http://dx.doi.org/10.3390/ma11101968) [30]. (c) schematic representation of a vertical GaN trench-MOSFET

3 Gallium nitride: properties and physical parameters

Gallium nitride, along with its InGaN and AlGaN alloys, represents an excellent material for both optoelectronics and electronics. In the early GaN era, the research efforts on gallium nitride have been driven by the need of fabricating high-efficiency short-wavelength (blue/violet) LEDs. GaN has a direct bandgap of 3.4 eV, thus being ideal for manufacturing ultraviolet optoelectronic devices. In addition, the energy gap of III-N alloys can be tuned between the 0.7 eV of InN and the 6.2 eV of AlN thus, in principle, allowing fabrication of LEDs with ultraviolet (UVA, UVB, UVC), visible and infrared emission.

Contrary to other semiconductors, like InP or GaAs, III-N semiconductors typically have a wurtzite crystal, with its characteristic hexagonal shape (see Figure 2). It can be easily understood that this lattice arrangement does not have an inversion plane perpendicular to the c-axis (0001) and, for this reason, the surfaces have either atoms from group III (In, Ga, Al), or nitrogen atoms [31]. The nature of the surfaces has a fundamental importance, since it determines the polarity of the polarization charges, as will be discussed in the following.

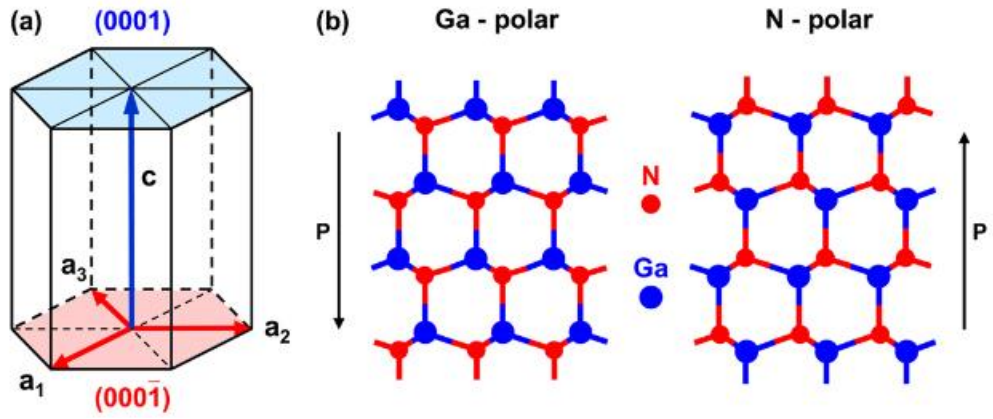


Figure 2: (a) Hexagonal unit cell and (b) atomic structure of Ga- and N-polar GaN. The arrows represent the direction of the spontaneous polarization dipole, P, in the GaN crystal. From "Recent progress in metal-organic chemical vapor deposition of (0001) N-polar group-III nitrides", S. Keller et al., Semiconductor Science and Technology, Volume 29, Number 11, 113001, August 2014, DOI: 10.1088/0268-1242/29/11/113001, IOP Publishing. Reproduced with permission. All rights reserved. (*https://iopscience.iop.org/article/10.1088/0268-1242/29/11/113001/pdf)* [32].

Table 1 reports the main parameters of gallium nitride, as compared with other semiconductor materials, including silicon, gallium arsenide, silicon carbide, aluminum nitride, diamond and gallium oxide. The materials are ordered with increasing energy gap E_G, from left to right. Excluding the three semiconductors for which commercial devices are not available (gallium oxide, diamond, and aluminum nitride), GaN is the semiconductor with the largest energy gap, the largest critical field, and the highest saturation velocity. As a consequence, it is an ideal candidate for the fabrication of power semiconductor devices, capable of operating at high temperature and voltage levels.

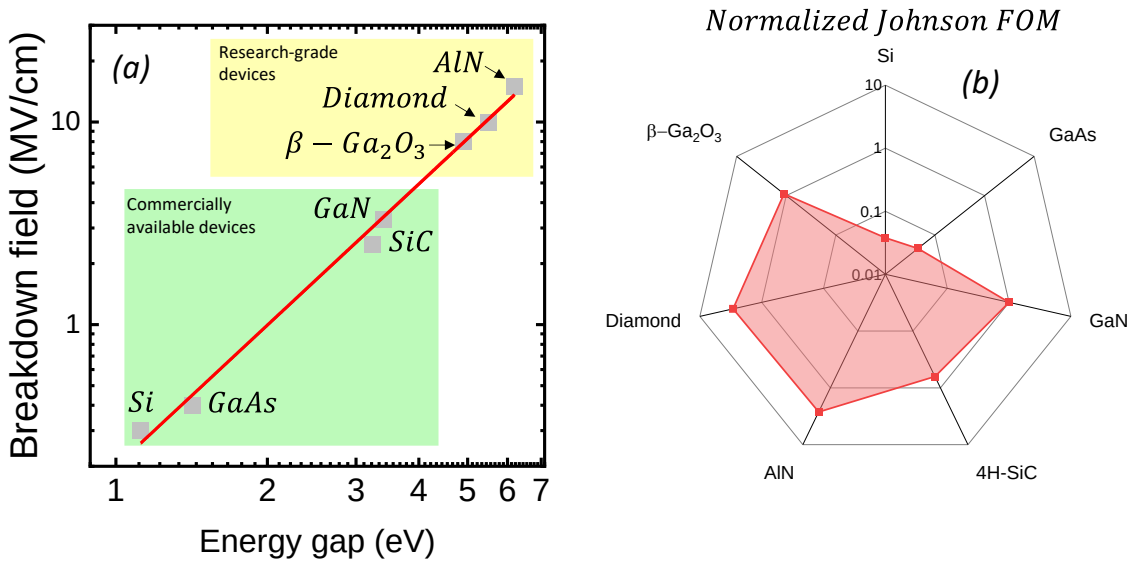


Figure 3 (a) reports the relation between breakdown field and energy gap for the semiconductor materials in Table 1. As can be noticed, breakdown field has a power-law dependence on the energy gap, in the form $E_{crit} \propto E_G^{2.3}$. This dependence is consistent with previous reports in the literature [33], and demonstrates the great advantage of using wide bandgap semiconductors for fabricating electron devices with high breakdown voltage.

Since a single parameter does not fully describe the properties of a material, semiconductors are typically compared by using figures of merit: the most commonly used are the Johnson FOM, for high-speed devices, and the Baliga FOM, for high power devices. With regard to the first, it is defined as the product of the maximum voltage and the maximum transit frequency, for a given value of the drain-source spacing (see details in Ref. [34]), i.e. as:

$$Johnson\ FOM = f_T V_{DS,max} = \frac{E_{crit} v_s}{2\pi}$$

The Johnson figure of merit indicates that, in general, devices with high breakdown voltage are typically slower than devices with lower voltage rating.

Figure 3 (b) reports the values of the Johnson figure of merit for the semiconductors listed in Table 1; all values are normalized to that of GaN, to allow an easy comparison. As can be noticed, the Johnson FOM of GaN is slightly higher than that of SiC (0.556), comparable to β-Ga_2O_3 (0.978),

and is much larger than that of silicon (0.0379) and GaAs (0.0455). AlN and diamond are better than GaN, but their Johnson FOMs are between 2.5 and 3, thus having the same order of magnitude of GaN. While there is a substantial advantage by moving from Si/GaAs to GaN, the improvement obtained by changing to AlN and diamond is only incremental, in terms of the Johnson FOM [34].

While the Johnson FOM allows to compare semiconductor materials for the fabrication of high-speed devices, the Baliga FOM has been introduced to compare semiconductors for application in power electronics. Considering a unilateral and abrupt (e.g. p^+/n^-) junction, as depicted in Figure 4 (a), the electric field profile at the n-side has a triangular shape (Figure 4 (b)), and – at the critical electric field E_{crit} – the space charge region has a width equal to

$$W_d = \epsilon_{r,GaN}\epsilon_0 E_{crit}/qN_D$$

where N_D is the donor density at the n-side of the diode, and $\epsilon_{r,GaN}\epsilon_0$ is the product between the relative permittivity of GaN and the permittivity of vacuum . The breakdown voltage is therefore

$$V_{br} = \frac{1}{2}E_{crit}W_d = \frac{\frac{1}{2}E_{crit}^2\epsilon_{r,GaN}\epsilon_0}{qN_D}$$

The resistance R_{ON} of the n-type semiconductor region is proportional to $W_d/\mu N_d$, so we can calculate [35]

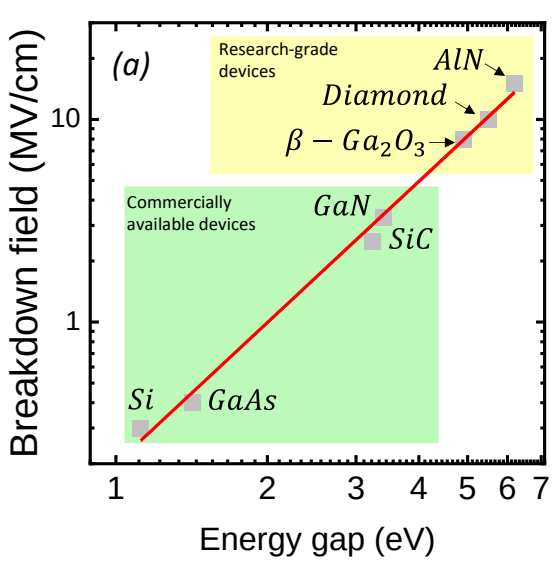
$$R_{ON} \propto \frac{W_d}{\mu N_D} \propto \frac{W_d^2}{\mu\epsilon_{r,GaN}\epsilon_0 E_{crit}} \propto \frac{4V_{br}^2}{\mu\epsilon_{r,GaN}\epsilon_0 E_{crit}^3}$$

The denominator of the last term is linked to the Baliga FOM [36], [37] (that was initially defined as $\mu\epsilon E_G^3$), and identifies the material parameters that help minimizing the conduction losses in power transistors. This FOM is defined based on the assumption that power losses only originate from the on-resistance of the FET. For this reason, it applies at relatively moderate frequencies, where conduction losses are dominant [36]. For higher frequency devices, one would have to consider also the contribution of switching losses. Figure 4 (c) reports the Baliga figure of merit (calculated as $\mu\epsilon E_{crit}^3$) for the same set of semiconductors in Table 1. All values are normalized to GaN: the plot indicates that the Baliga FOM of GaN is substantially larger than those of silicon and GaAs, higher than SiC, similar to the one of gallium oxide. Diamond and AlN (ultra wide-

bandgap semiconductors) have a much higher Baliga FOM, and can be considered as interesting alternatives to further push the limits.

Material	**Si**	**GaAs**	**4H-SiC**	**GaN**	**b-Ga_2O_3**	**Diamond**	**AlN**
E_G(eV)	1.12	1.42	3.23	3.4	4.9	5.5	6.2
ε_r	11.7	12.9	9.66	8.9	10	5.7	8.5
μ (cm^2/Vs)	1440	9400	950	1400	250	4500	450
E_{crit} (MV/cm)	0.3	0.4	2.5	3.3	8*	10*	15*
v_s (x10^7 cm/s)	1	0.9	2	2.4	1.1	2.3	1.4
κ_{th} (W/cmK)	1.3	0.55	3.7	2.5	0.1-0.3	23	2.85

Table 1: main material parameters for GaN, as compared with other semiconductors. Reported parameters are energy gap (E_G), relative dielectric permittivity (ε_r), electron mobility (μ), critical electric field (E_{crit}), electron saturation velocity (v_s), and thermal conductivity (κ_{th}). Data are taken from: P. Fay et al.,High-Frequency GaN Electronic Devices, https://doi.org/10.1007/978-3-030-20208-8_2 [34] (*Estimated). The critical electric field of GaN is taken from Ref [12]. Note that for GaN mobility values up to 2000 cm^2/Vs are reported, see for instance [12].



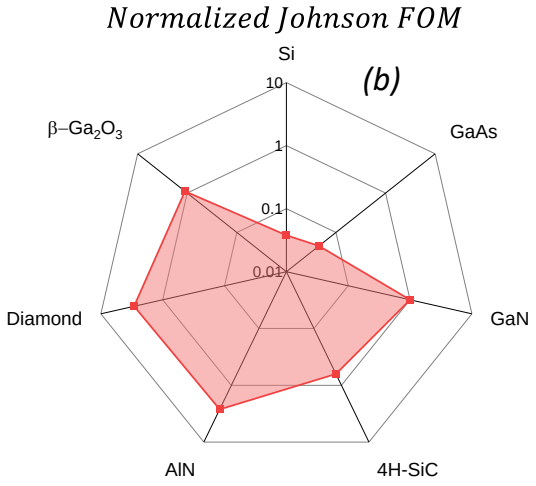


Figure 3: (a) dependence of breakdown field on energy gap for the semiconductor materials in Table 1. (b) Johnson figure of merit for the same set of semiconductors. All values are normalized to GaN, to allow an easy comparison. Data are taken from Table 1

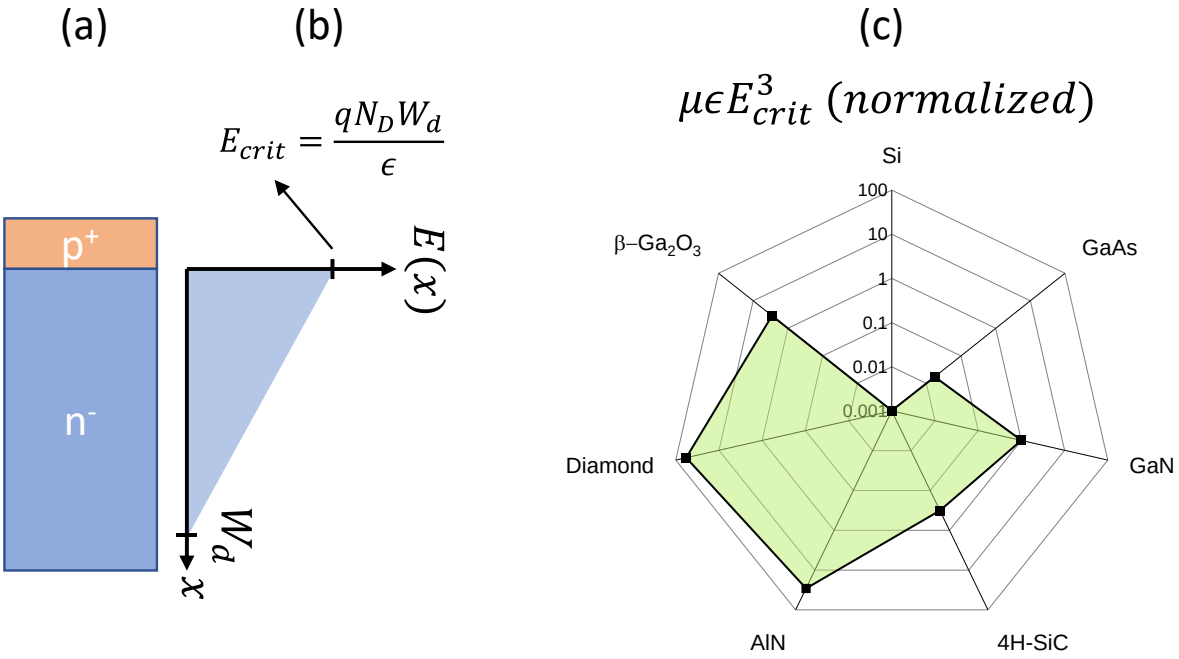


Figure 4: (a) schematic representation of a unilateral abrupt p^+/n^- junction; (b) approximated electric field profile for the junction in (a); (c) Baliga figure of merit (calculated as $\mu\epsilon E_{crit}^3$) for the same set of semiconductors in Table 1. All values are normalized to GaN, to allow an easy comparison. Data are taken from Table 1

The dependence of the bandgap of GaN on temperature follows the Varshni relation

$$E_G(T) = E_{G,0} - \frac{\alpha\, T^2}{T + \beta}$$

For GaN, AlN and InN the related parameters are summarized in Table 2. As can be noticed, by using alloys of GaN, AlN and InN it is possible to vary the bandgap of the alloy in a wide range,

from 0.7 eV to 6.2 eV. In most cases, GaN transistors are based on AlGaN/GaN heterostructures, and AlN and AlGaN layers are used as nucleation and buffer layers respectively. InAlN devices have also been investigated: lattice matched InAlN/GaN HEMTs allow an efficient down-scaling of the transistor dimensions, thus allowing to reach high cut-off frequencies [38].

For ternary alloys, such as AlGaN and InGaN, the bandgap deviates from the Vegard's rule, and follows the empirical expression

$$E_G(A_xB_{1-x}N) = xE_G(AN) + (1-x)E_G(BN) - x(1-x)b$$

where $E_G(AN)$ and $E_G(BN)$ are the bandgaps of the two materials (AN and BN), x is the molar fraction of A, and b is a bowing parameter. For AlGaN, the material of interest for $Al_xGa_{(1-x)}N$/GaN HEMTs, the relation has been determined as [39], [40]

$$E_{G(AlGaN)}(x) = [6.0x + 3.42(1-x) - 1.0x(1-x)]\ eV$$

Other bandstructure parameters of interest for GaN are the effective density of states in the conduction and valence bands ($N_C = 2.24 \cdot 10^{18}\ cm^{-3}$, $N_V = 4.56 \cdot 10^{19}\ cm^{-3}$), and the effective masses of electrons and holes ($m_e = 0.20$ and $m_h = 1.49$) [34]

	$E_{G,0}(eV)$	$\alpha\ \left(\frac{meV}{K}\right)$	$\beta\ (K)$
GaN	3.507	0.909	830
AlN	6.23	1.799	1462
InN	0.69	0.414	454

Table 2: bandgap and Varshni parameters for GaN, AlN and InN. For GaN, results data are taken from [41], for AlN from [42], for InN from [43].

4 Polarization charges in GaN

Controlled doping of wide bandgap semiconductors is not always straightforward: typically, mobile carriers in FET are induced through impurity doping, i.e. by introducing foreign atoms in

a semiconductor lattice. The energy distance between the dopant level and the related band ($E_C - E_D$ for a donor level at energy E_D, or $E_A - E_V$ for an acceptor level at energy E_A) represents the dopant binding (or ionization) energy. The best dopants are relatively shallow, with binding energies in the range 0.01 eV – 0.05 eV. For GaN, only shallow donors are available (silicon, $E_C - E_D$=0.015 eV), while the conventional acceptor is magnesium, that creates a level 0.16 eV above the valence band energy. As a consequence, it is relatively easy to achieve high electron concentrations, whereas for reaching high hole densities dopant levels in excess of $10^{19}\ cm^{-3}$ are required. It is worth noticing that even high quality GaN has a residual n-type (unintentional) conductivity, resulting in carrier densities in the range $10^{15} - 10^{17}\ cm^{-3}$, depending on material properties. Such residual conductivity has been ascribed to native defects of the semiconductor (e.g. point defects, vacancies, antisites), and impurities (like carbon, oxygen, hydrogen) [40]. The suppression of such defect-induced free carriers is very important for the fabrication of highly-insulating GaN layer, to be used in devices with extremely high blocking voltages.

Contrary to conventional semiconductors, GaN has a unique advantage, that helps obtaining high carrier densities even in absence of intrinsic doping: gallium nitride, in fact, is a polar material, and exhibits strong polarization effects.

As already mentioned, the wurtzite crystal of III-N semiconductors, which are typically grown epitaxially along the (0001) orientation, leads to the existence of polarization fields, that are both spontaneous and piezoelectric. With zero external field, the total polarization P is equal to the sum of the spontaneous polarization P_{sp} and of the piezoelectric (or strain-induced) polarization P_{pz}. Bernardini et al. [44] investigated the polarization in GaN layers along the (0001) axis. Nitrogen has a higher electronegativity, compared to gallium. As a consequence, Ga and N atoms have anionic (+) and cationic (-) characteristics, generating a spontaneous polarization P_{sp} along the (0001) axis [35]. Wurtzite is the crystal arrangement with highest symmetry compatible with the presence of spontaneous polarization [44]–[46]. The arrangement of the cation and anion sublattices can lead to a relative movement from the ideal wurtzite position, favoring the spontaneous polarization [47]. The orientation of spontaneous polarization is defined assuming that the positive direction goes from the metal (Ga) to the nearest nitrogen atom, along the c-axis [48]. Figure 5 depicts the crystal structure of GaN, and the sign and direction of the spontaneous polarization.

The values of the spontaneous polarization in GaN, InN and AlN are reported in Table 3 for binary semiconductors. In the case of interfaces between binary and ternary semiconductors, the following expressions can be used (see also [49] and references therein):

$$P_{sp,Al_xGa_{1-x}N\ /\ GaN}\ (x) = (-0.052x - 0.029)\ [C \cdot m^{-2}]$$

$$P_{sp,In_xGa_{1-x}N\ /\ GaN}\ (x) = (-0.003x - 0.029)\ [C \cdot m^{-2}]$$

$$P_{sp,In_xAl_{1-x}N\ /\ GaN}\ (x) = (0.049x - 0.081)\ [C \cdot m^{-2}]$$

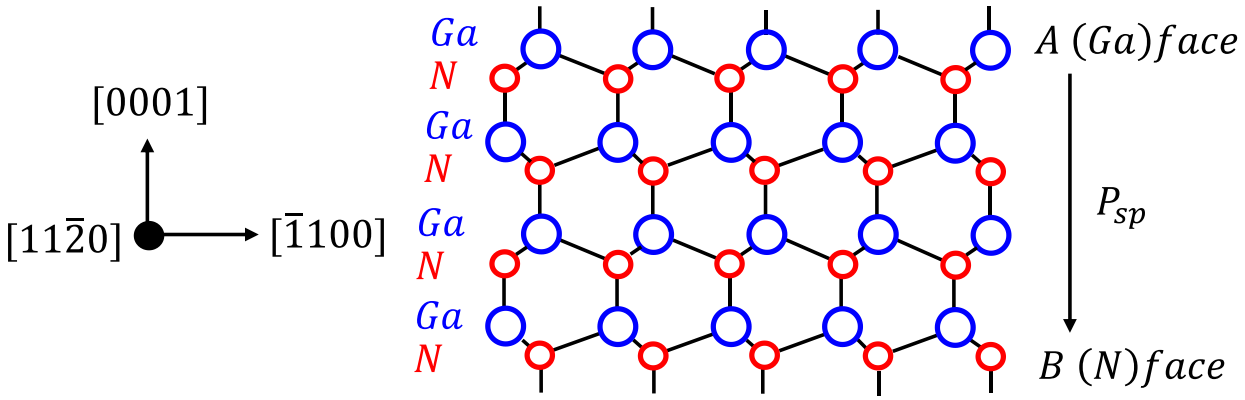


Figure 5: crystal structure of GaN, showing the sign and direction of the spontaneous polarization (adapted from Ref. [50])

Material	GaN (C m^{-2})	InN (C m^{-2})	AlN (C m^{-2})
P_{sp}	-0.029	-0.032	-0.081
P_{sp}	-0.034	-0.042	-0.090

Table 3: values of spontaneous polarization of III-N semiconductors (binary). Values in the first row are from [44], values in second row are from [51].

The strain in the crystal, and the displacement of the anion sublattice with respect to the cation sublattice, can lead to a piezoelectric polarization of the III-N semiconductors. A (simplified)

representation of the polarization is given in Figure 6, that reports a ball and stick diagram of the bond (theahedral) between gallium and nitrogen. In this figure, the Ga-polar configuration is represented. The electron cloud is closer to the nitrogen atoms, and this generates the polarization vectors. If the tetrahedron is ideal, the in-plane and vertical polarization components cancel each other [52]. When an in-plane tensile strain is applied (as shown in Figure 6, (a)) the polarization generated by the triple bonds decreases, and this generates a net polarization along the $(000\bar{1})$ direction. On the contrary, when an in-plane compressive strain is applied (as shown in Figure 6, (b)) the polarization generated by the triple bonds increases, and this generates a net polarization along the (0001) direction.

To calculate the piezoelectric polarization, one needs to refer to the piezoelectric constants of the materials under analysis. Details on the main parameters were given in [44], [48], [53], and a comprehensive summary was presented in [49]; here, in Table 4, we report the values of piezoelectric constants e_{ij} and lattice parameters a_0 and c_0 for GaN, InN and AlN.

As discussed in [48], the lattice structure of wurtzite semiconductors is defined by the length of the hexagonal edge a_0, the height of the prism c_0, and a parameter u that defines the length of the bond parallel to the c-axis ([0001]) in units of c_0. To calculate the piezoelectric polarization P_{pz} along the c-axis, the key relation is

$$P_{pz} = e_{33}\epsilon_z + e_{31}(\epsilon_x + \epsilon_y)$$

Here $\epsilon_z = (c - c_0)/c_0$ represents the strain along the c-axis, while the in-plane strain $\epsilon_x = \epsilon_y = (a - a_0)/a_0$ is assumed to be isotropic. a and c are the lattice constants of the strained layers, and differ from a_0 and c_0.

By considering that the lattice constants in a hexagonal AlGaN system are related according to

$$\frac{c - c_0}{c_0} = -2\left(\frac{C_{13}}{C_{33}}\right)(a - a_0)/a_0$$

where C_{13} and C_{33} are elastic constants, the value of piezoelectric polarization along the c-axis can be calculated as

$$P_{pz} = 2(a - a_0)/a_0\left(e_{31} - \frac{e_{33}C_{13}}{C_{33}}\right)$$

For an $Al_xGa_{1-x}N$/GaN stack, the material system of interest for GaN-based transistors, the values of the elastic constants can be calculated from the following formulas (see [49], [54] for details)

$$C_{13}(x) = (5x + 103)\ [GPa]$$

$$C_{33}(x) = (-32x + 405)\ [GPa]$$

and the variation of the lattice constant with the molar fraction is

$$a(x) = (-0.077x + 3.189) \cdot 10^{-10}\ m$$

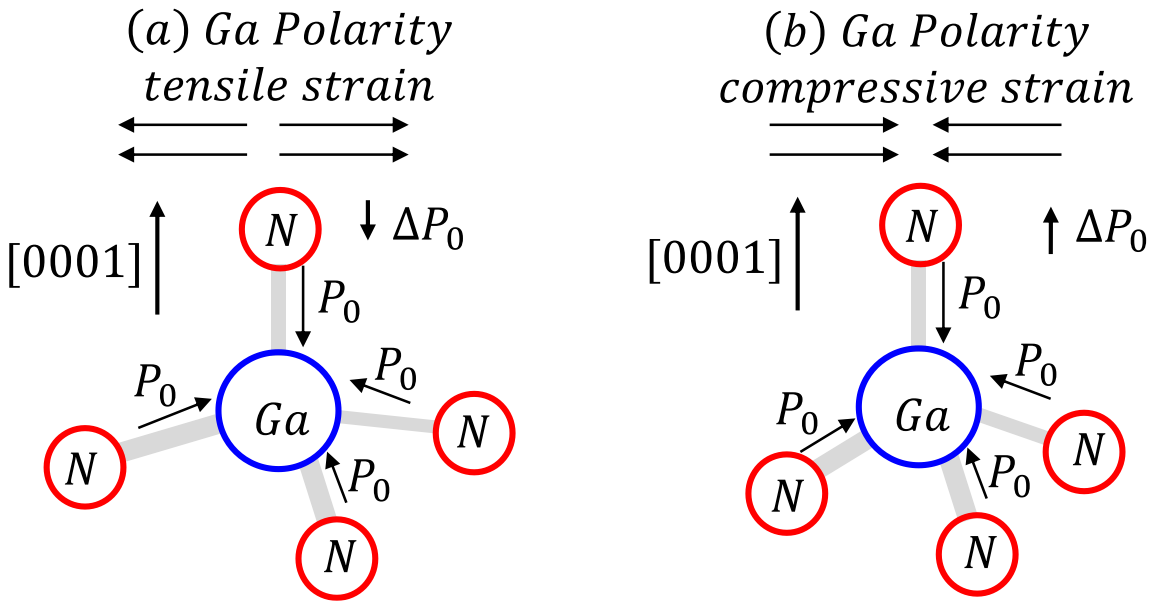


Figure 6: schematic ball-and-stick configuration of a GaN tethrahedron with in-plane (a) tensile and (b) compressive strain, showing a net polarization. A full description including also the case of N-polar material can be found in [52].

Material	GaN	InN	AlN
$e_{31}\ (C \cdot m^{-2})$	-0.49 [44]	-0.57 [44]	-0.6 [44], -0.58 [54]

e_{33} $(C \cdot m^{-2})$	0.73 [44]	0.97 [44]	1.46 [44], 1.55 [54]
a_0 (Å)	3.189	3.54	3.112
c_0 (Å) [48]	5.185	5.705	4.982

Table 4: values of piezoelectric constants e_{ij} and lattice parameters a_0 and c_0 for GaN, InN and AlN

In a GaN layer, polarization charges are present on each unit cell. As schematically depicted in Figure 7, the internal polarization charges cancel each other. Only the Q_π and $-Q_\pi$ at the N- and Ga-faces remain, and form a charge dipole (Figure 7 (c)). Based on the numbers given in Table 3, the spontaneous polarization charge in GaN has values in the range $1.8 - 2.1 \cdot 10^{13}\ e^-/cm^2$. In absence of other charges, the polarization charge would lead to the presence of a dipole, resulting in a fairly high electric field, in the range of MV/cm. Such dipole is screened through the formation of a screening dipole (Q_{scr}). In absence of the screening dipole, a non-physical situation would form. As discussed in [47], a first hypothesis would be that the screening dipole originates from ions from the atmosphere (H^+, OH^-); however, the dipole is present also in material grown in atmosphere free of counter ions, like during molecular beam epitaxy (MBE) growth.

A different interpretation can be given by considering the presence of donor states at the surface of the GaN layer [55], [56], as schematically represented in Figure 8 (a). In absence of compensating charge, due to the presence of the polarization dipole $\pm Q_\pi$, an electric field is present in the GaN layer, and the band diagram shows a linear slope (Figure 8 (b)). If the GaN layer is sufficiently thick, the donor states pins the Fermi level at the surface (at the donor level E_{DD}), and the screening charge N_{DD}^+ at the surface is formed. The presence of a surface level E_{DD} has been proved also experimentally [47]. Realistic GaN layers typically have a n-type conductivity, as mentioned above. The ionized (bulk) donors also contribute to the overall charge balance. For a thick GaN layer (see Figure 8 (d)), the bands are nearly flat (corresponding to negligible field), apart from the surface region. The polarization charge $-Q_\pi$ at the surface is compensated by the positive charge of the ionized surface defects N_{DD}^+ and by the total density of charges in the depleted n-type GaN [47].

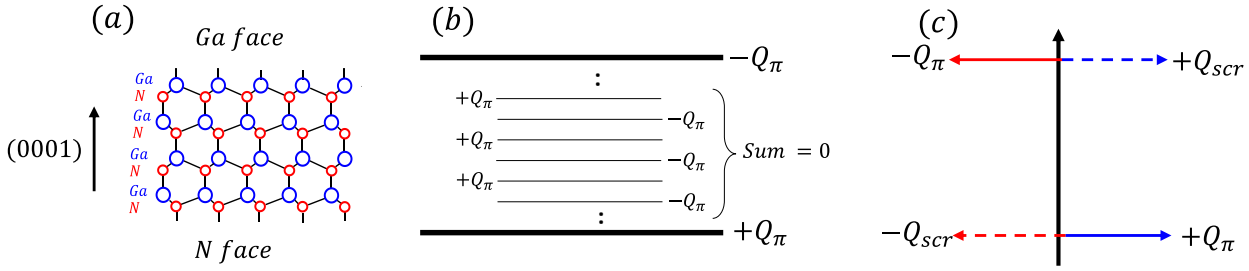


Figure 7: (a) schematic representation of a GaN lattice with ball and stick representation of the bonds, and indication of the Ga- and N-faces, along the (0001) direction. (b) model for polarization charge in a gallium nitride layer. (c) charge distribution at the Ga- and N-faces, showing the polarization and screening dipoles (see also [47])

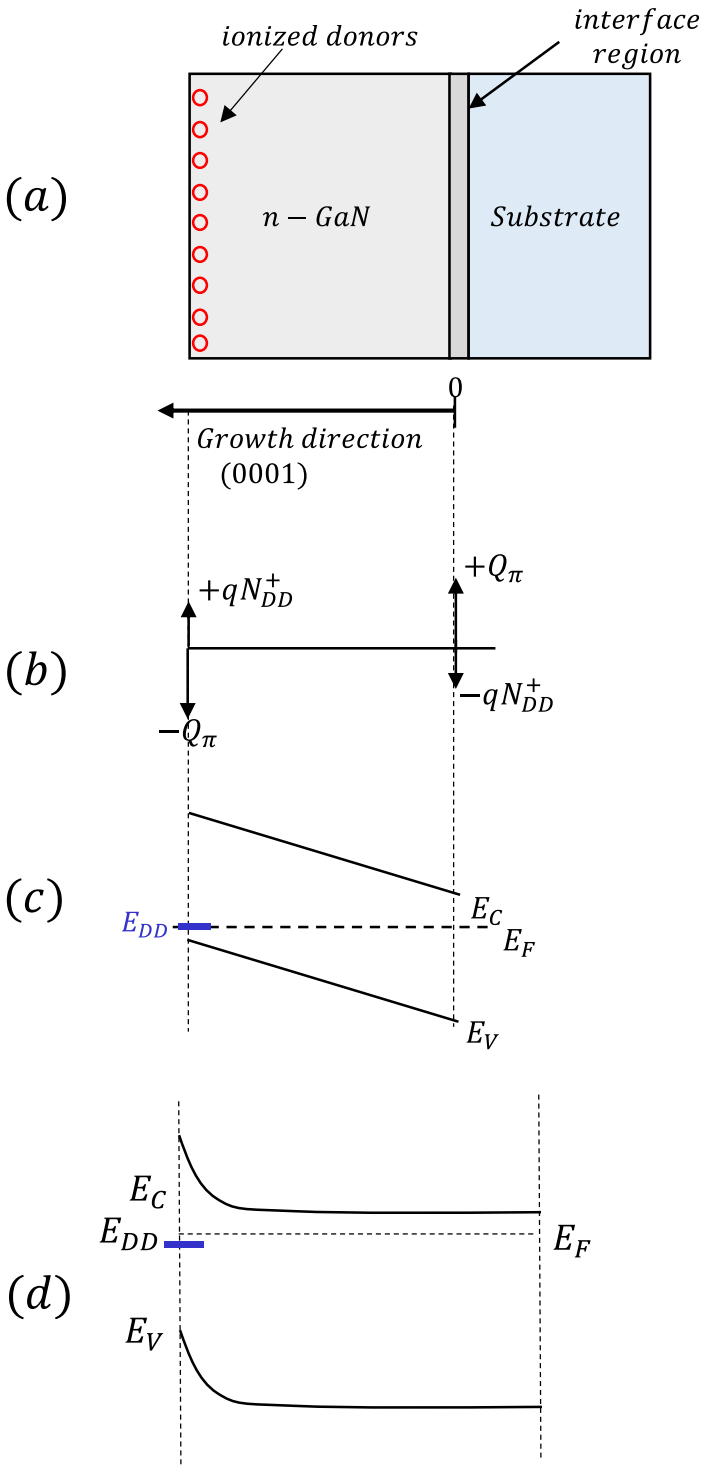


Figure 8: (a) schematic representation of a n-type GaN layer grown on a substrate. The (defective) interface region is shown. (b) charge diagram showing the screening induced by surface donors. (c) band diagram showing the surface donor level approaching the Fermi level at the surface of GaN, thus leading to the generation of the screening charge qN_{DD}^{+}. (d) band diagram for a thick

GaN (n-type), considering the presence of surface states and of donor charges (figure adapted from [47])

5 Band diagrams and charge density in AlGaN/GaN heterostructures

The core of a GaN-based HEMT is the AlGaN/GaN heterostructure. Both the GaN and the AlGaN layers are typically left undoped, to minimize electron scattering at impurities. Based on the considerations above, undoped GaN has a weak n-type conductivity, with electron densities that depend on the quality of the epitaxy, and that – even in the best case – are higher than 10^{15} cm^{-3} [47] (early GaN films were showing a high n-type conductivity, in the range of 10^{17}-10^{18} cm^{-3} [57], [58]). Optimizing the background electron density in lateral and vertical HEMTs requires a tuning of the growth process, and the control of the residual impurities (such as carbon, see for instance [59]).

Figure 9 shows the charge distribution, the electric field profile, and a schematic band diagram for an AlGaN/GaN heterostructure used in HEMT technology. In the figure, t is the thickness of the AlGaN layer, while the 2DEG is supposed to be located at a position d, a few nanometers far from the heterojunction, on the GaN side.

At the surface of the AlGaN layer, the total charge is determined by the sum of the charge of the surface donors and of the polarization charge of the AlGaN layer, $qN_{DD}^{+} - Q_{\pi(AlGaN)}$. At the AlGaN/GaN heterojunction, the total charge is given by the difference between the polarization charges of AlGaN and GaN, i.e. $Q_{\pi(AlGaN)} - Q_{\pi(GaN)}$. For gallium polar material, this is a positive number, since AlGaN has a higher polarization, compared to GaN. In the triangular potential well formed near the heterojunction, on the GaN side, a 2-dimensional electron gas is formed. For simplicity, we consider this sheet of charge to be located in $x = d$ (position of the centroid of the electron distribution).

The value of d can be easily determined by solving the Schroedinger equation in the triangular potential well formed at the AlGaN/GaN interface, that is schematically represented in Figure 10.

The electric field $\mathcal{E}_{GaN}$ is supposed to originate only from the charge in the 2DEG (n_s), and is thus equal to $qn_s/(\epsilon_0\epsilon_{GaN})$. The solution of the Schroedinger equation is approximated by the formula [60]–[62]

$$E_n \approx \left(\frac{\hbar}{2m^*}\right)^{\frac{1}{3}}\left(\frac{3}{2}\pi q\mathcal{E}_{GaN}\right)^{\frac{2}{3}}\left(n+\frac{3}{4}\right)^{\frac{2}{3}} = \left(\frac{\hbar}{2m^*}\right)^{\frac{1}{3}}\left(\frac{3}{2}\pi q\right)^{\frac{2}{3}}\left(n+\frac{3}{4}\right)^{\frac{2}{3}}\left(\frac{qn_s}{\epsilon_0\epsilon_{GaN}}\right)^{\frac{2}{3}}$$

We now consider that the first sub-band E_0 is dominant. The 2D density of states associated with a single quantized level is [62]

$$D_{DOS} = \frac{qm^*}{\pi\hbar^2}$$

The electron concentration in the 2DEG can then be calculated starting from the 2D density of states and from the position of the Fermi level, by using the Fermi-Dirac distribution as follows [62]:

$$n_s = D_{DOS}\cdot\frac{kT}{q}\cdot\ln\left[1+\exp\frac{q(E_F-E_0)}{kT}\right]$$

where k is the Boltzmann constant.

By simple calculations (see details in Ref. [47]), one can calculate the position d of the 2DEG, with respect to the heterointerface. Here the 2DEG is considered as an ideal 2D sheet of electrons located at a distance d from the interface, on the GaN side. For an AlGaN/GaN heterostructure, a typical value of d is 2 nm [47].

At the bottom of the GaN layer, at the interface with the substrate, a screening charge compensates the (positive) component $Q_{\pi(GaN)}$. The reader should note that in more realistic structures other layers (e.g. a C-doped layer, a step-graded or a superlattice-based buffer, an AlN nucleation layer) are placed between the GaN channel layer and the substrate; these layers are not shown here for simplicity.

At the surface of the AlGaN layer (if the layer is thick enough), the potential $q\phi_s$ is pinned at the surface donor level E_{DD}. The AlGaN layer is not doped, so – in absence of external bias – its electric field depends only the sheet charge densities as follows:

$$\mathcal{E}_{AlGaN} = \frac{[qN_{DD}^{+} - Q_{\pi}(AlGaN)]}{\epsilon_0 \epsilon_{AlGaN}}$$

With regard to the electric field in the GaN, we suppose that it originates only from the charge in the 2DEG, and neglect (for this analysis) the effect of the n-type donor charge in the GaN. A more realistic solution can be obtained numerically, through technology computer-aided design (TCAD) tools. Under this assumption, the electric field in the GaN is

$$\mathcal{E}_{GaN} = \frac{qn_s}{\epsilon_0 \epsilon_{GaN}}$$

The total potential drop in the AlGaN is then

$$V_{AlGaN} = -\mathcal{E}_{AlGaN} t = -\frac{[qN_{DD}^{+} - Q_{\pi}(AlGaN)]}{\epsilon_0 \epsilon_{AlGaN}} t = \frac{[Q_{\pi}(AlGaN) - Q_{\pi}(GaN) - qn_s]}{\epsilon_0 \epsilon_{AlGaN}} t$$

and, for GaN

$$V_{GaN} = \mathcal{E}_{GaN} d = \frac{qn_s}{\epsilon_0 \epsilon_{GaN}} d$$

Considering the band diagram in Figure 9, one can calculate

$$\phi_s - V_{AlGaN} - \frac{\Delta E_c}{q} + V_{GaN} = 0$$

By combining the equations above, by considering $\epsilon = \epsilon_0 \epsilon_{GaN} \sim \epsilon_0 \epsilon_{AlGaN}$, the value of the sheet-charge density n_s can be calculated

$$n_s = \frac{[Q_{\pi}(AlGaN) - Q_{\pi}(GaN)]t - \epsilon \ \ (\phi_s - \frac{\Delta E_C}{q})}{q(t+d)}$$

When a potential V_G is applied to the gate (through a suitable metal deposited on the AlGaN barrier), the charge in the 2DEG can be modulated: a more positive voltage will fill the channel, whereas moving to negative values of V_G will lead to the depletion of the 2DEG.

The dependence of n_s on V_G has the following form:

$$n_s(V_G) = \frac{[Q_{\pi}(AlGaN) - Q_{\pi}(GaN)]t + \epsilon \left[V_G - \left(\phi_b - \frac{\Delta E_C}{q}\right)\right]}{q(t+d)}$$

where ϕ_b is the barrier at the metal/AlGaN interface.

Figure 11 (a) reports the value of the polarization charge $Q_\pi(AlGaN) - Q_\pi(GaN)$ at the $Al_xGa_{1-x}N$/GaN interface as a function of the molar fraction x. The values have been calculated based on the parameters given in Ref, [54] as:

$$Q_\pi(AlGaN) - Q_\pi(GaN) = Q_{\pi,pz}(AlGaN) + Q_{\pi,sp}(AlGaN) - Q_{\pi,sp}(GaN)$$
$$= \left| \frac{2\big(a(0) - a(x)\big)}{a(x)} \left[e_{31}(x) - e_{33}(x) \cdot \frac{C_{13}(x)}{C_{33(x)}} \right] + Q_{\pi,sp}(x) - + Q_{\pi,sp}(0) \right|$$

where the spontaneous polarization charge in an $Al_xGa_{1-x}N$ layer is defined as

$$Q_{\pi,sp}(x) = (-0.052x - 0.029) \left[\frac{C}{m^2} \right]$$

A typical range of interest for the mole fraction is between 0.2 and 0.4; such values are sufficiently high to give a reasonable polarization charge (which is necessary for generating electrons in the 2DEG), and enough conduction band discontinuity at the AlGaN/GaN heterointerface (which is necessary to ensure a good confinement of the 2DEG electrons). At the same time, the use of molar fractions higher than 0.4 may be critical, since the thermal and lattice mismatch between AlGaN and GaN may lead to high defect density and rough interfaces, that may limit the overall device performance.

Figure 11 (b) reports the sheet charge density (n_s) of the 2DEG for three $Al_xGa_{1-x}N$/GaN interfaces, as a function of the Al mole fraction and of the thickness of the AlGaN layer. For the calculation, a Schottky barrier equal to

$$q\phi_b = 1.3x + 0.84\ eV$$

was used, and the conduction band discontinuity at the $Al_xGa_{1-x}N$/GaN interface was calculated as

$$\Delta E_C = 0.7[E_G(x) - E_G(0)]$$

with

$$E_G(x) = x \cdot 6.13\ eV + (1-x) \cdot 3.42\ eV - x(1-x) \cdot 1\ eV$$

in agreement with Ref. [54].

As can be noticed, when the mole fraction x is around 0.2-0.3, the sheet charge density is around $10^{13}\ cm^{-3}$. With increasing thickness of the AlGaN layer, the density of electrons in the 2DEG increases, since the conduction band at the channel edge drops further below the Fermi level at the AlGaN/GaN interface (see also the band diagram in Figure 9). As can be understood, AlGaN/GaN HEMTs are intrinsically normally-on. At zero gate bias, the channel is formed, with a high electron density. A first possible approach to change the threshold voltage (by keeping the same Al content in the barrier) is to reduce the thickness of the AlGaN barrier. For sufficiently thin AlGaN barriers, the electron density falls to zero, and the 2DEG vanishes. This effect has also been observed experimentally, see for instance Ref. [55]. This is just one of the possible approaches to achieve normally-off operation in HEMTs; an excessive thinning of the barrier, along with the related etching process, may result in a significant increase in the leakage, and counter measures are required to guarantee a good device performance. In the next sections, the various approaches for normally-off operation are compared critically.

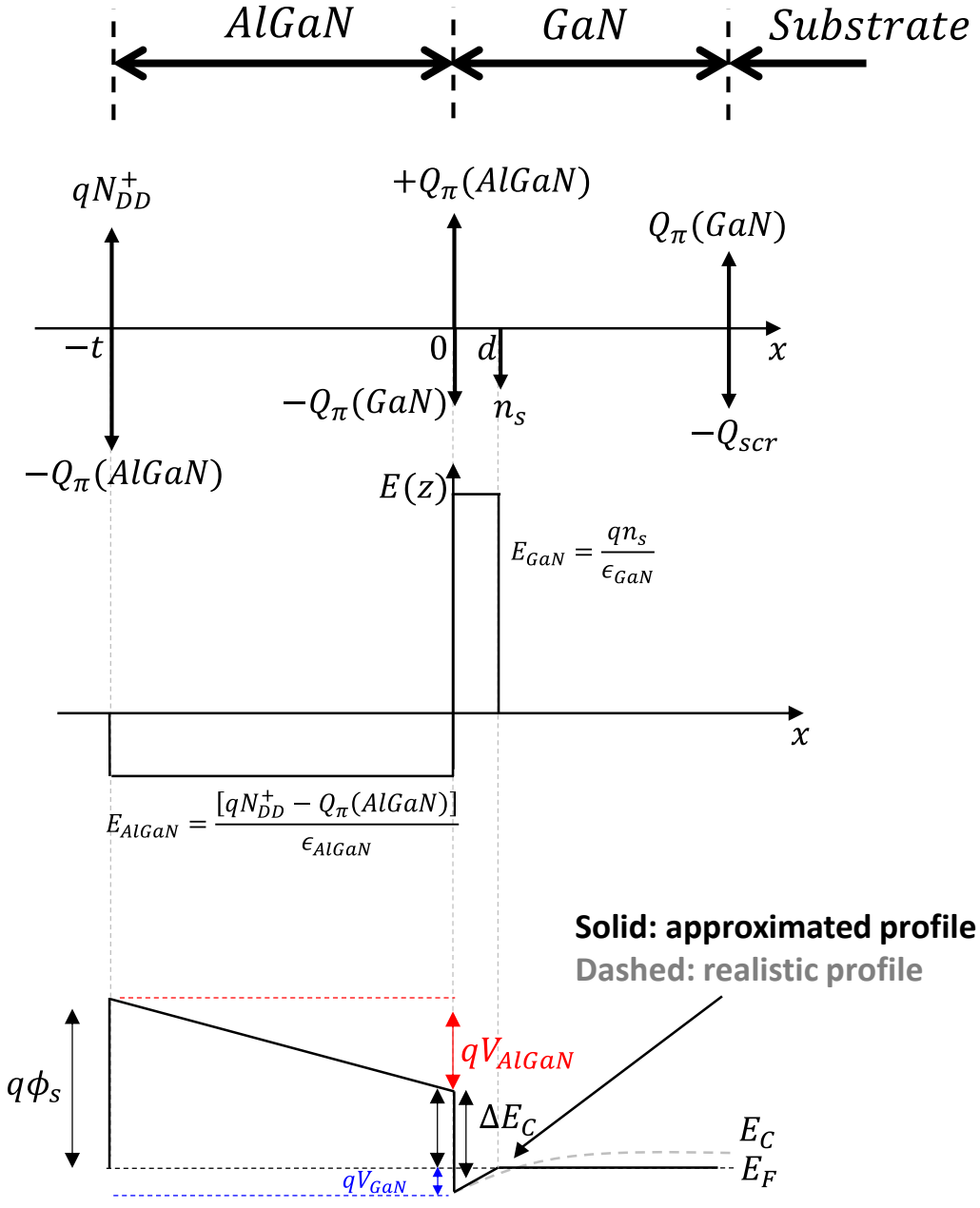


Figure 9: charge distribution, electric field profile, and schematic band diagram of an AlGaN/GaN heterostructure

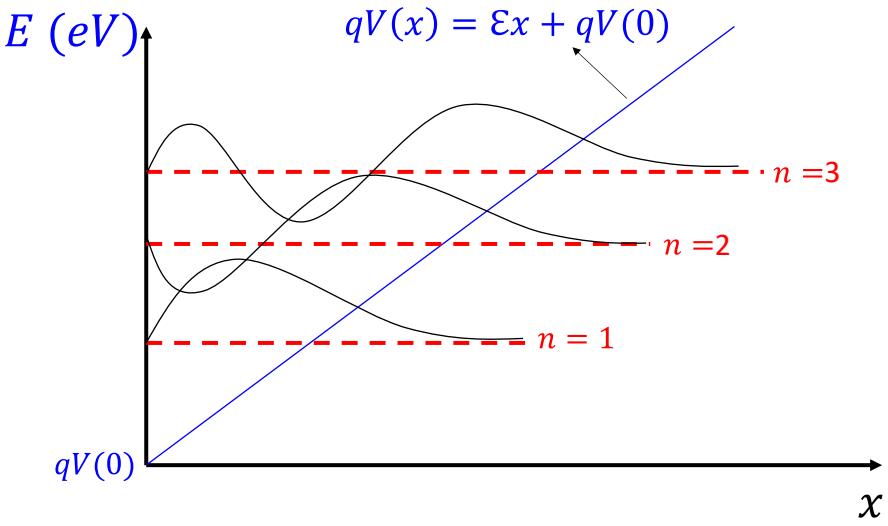


Figure 10: triangular potential well, similar to the one formed at the GaN-side of an AlGaN/GaN interface. The energy varies linearly with field Ɛ, starting from the value $qV(0)$ at the GaN-side of an AlGaN/GaN interface. The energy levels and wavefunctions are schematically drawn (not to scale). Figure is adapted from Ref [63].

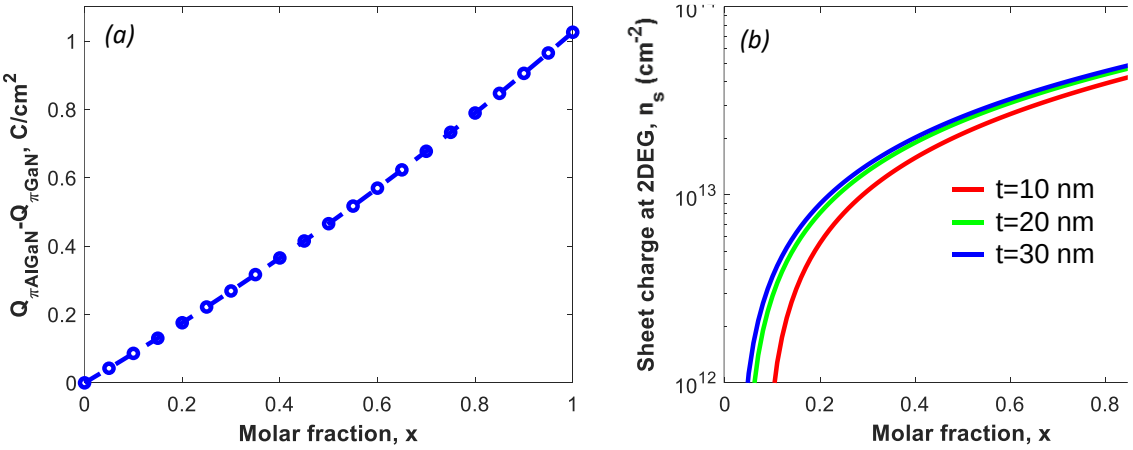


Figure 11: (a) polarization charge density at the AlGaN/GaN heterointerface ($Q_\pi(AlGaN) - Q_\pi(GaN)$) calculated as described in [54]. (b) sheet charge density calculated for the 2DEG of an AlGaN/GaN heterojunction as a function of molar fraction x and thickness t of the AlGaN layer

In a GaN-based transistor, a gate metal is placed on an AlGaN/GaN heterostructure; the resulting schematic structure is shown in Figure 12 (a). For a power semiconductor device, the most critical parameters are the on-resistance R_{on} (that needs to be as low as possible, to minimize the resistive losses in power converters) and the breakdown voltage (V_{br}, that must be sufficiently high to ensure good reliability). In AlGaN/GaN HEMTs, these two parameters are strongly correlated: carriers are generated by polarization, and the breakdown voltage scales with the distance between the gate and drain (L_{GD}) [35]. In an first-order approximation, the on-resistance of the device is the sum of the channel resistance ($R_{channel}$, originated from 2DEG under the gate) and of the drain-side access region (R_{drain}), according to the following equation [35]:

$$R_{on} = R_{channel} + R_{drain} = \frac{L_G}{W_G} \cdot \frac{1}{q\mu n_s} + \frac{L_{GD}}{W_G} \cdot \frac{1}{q\mu n_s}$$

It is worth noticing that in this calculation the contribution of the source and contact resistance is neglected, with no loss of generality. The off-state voltage is supported by the gate-drain access region; at the breakdown voltage, the relation between gate-drain spacing and the breakdown voltage is $L_{GD} = V_{br}/E_{crit}$, and we can write:

$$R_{on} = R_{channel} + R_{drain} = \frac{1}{W_G} \frac{1}{q\mu n_s} \left(L_G + \frac{V_{br}}{E_{crit}} \right)$$

In high-voltage devices, the gate-drain spacing is typically longer than the gate length. Figure 6 (b) reports the variation of the on-resistance (multiplied by the gate width W_g) as a function of the target breakdown voltage for devices having different gate lengths (0.25 µm and 1 µm). For mobility and sheet charge density values of 1400 cm^2/Vs and 10^{13} cm^{-2} were used. As can be understood, for low-breakdown voltage devices (corresponding to devices with a short gate-drain distance), the on-resistance is strongly determined by the gate length. Decreasing the gate length from 1 µm to 0.25 µm can lead to a substantial reduction in the resistive losses. On the contrary, for high breakdown voltage devices, the resistive contribution of the gate-drain access region becomes relevant, and R_{on} scales with the breakdown voltage. Figure 6 (b) also shows that the use of GaN devices with nearly-ideal breakdown field (3.3 MV/cm, see Table 1) can lead to a substantial improvement in on-resistance, compared to the more conservative case of 1 MV/cm

reported in previous publications [35]. Optimizing the breakdown field of the material is a key step for minimizing the resistive losses in power semiconductor devices.

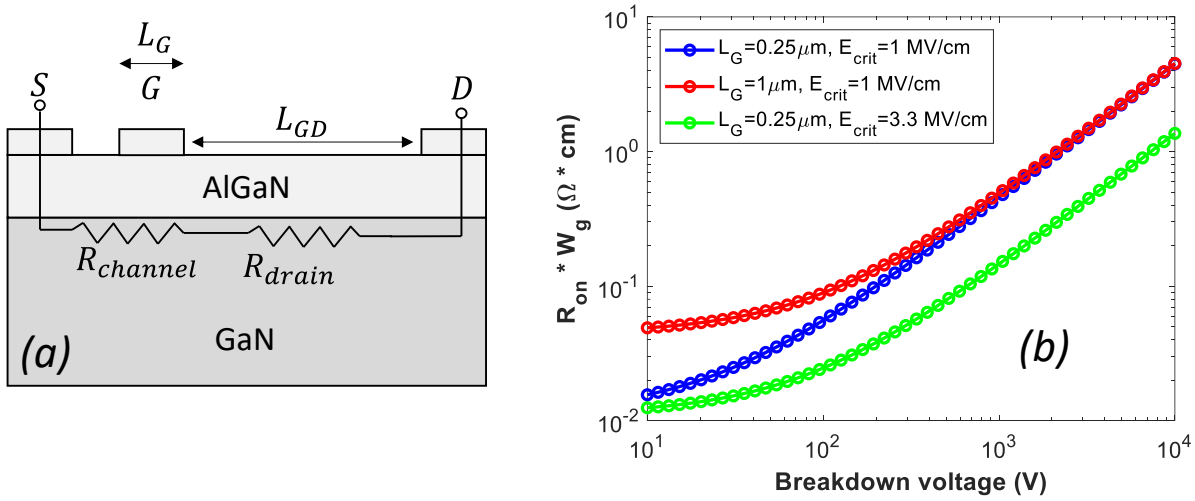


Figure 12: (a) schematic representation of the structure of a GaN HEMT, showing the parasitic resistance of the channel ($R_{channel}$) and of the gate-drain access region (R_{drain}). (b) dependence of the product $R_{on} \cdot W_g$ on breakdown voltage, for devices with different gate length, and under the hypothesis that the breakdown field is 1 MV/cm and 3.3 MV/cm

Besides resistive losses, also switching losses can play a relevant role in limiting the efficiency of a switching mode power converter. One of the parameters used to quantify the switching losses related to a specific transistor is the gate charge Q_G. For understanding the meaning of this parameter, we consider the simple circuit in Figure 12 (a). Here the FET is supposed to be ideal, and three capacitances $C_{GS}, C_{GD}, and\ C_{DS}$ are added to model the parasitic capacitive components. A fixed current is forced into the gate, and the measured gate voltage is plotted as a function of the charge flowing towards the gate. Figure 12 (b) shows the schematic gate-charging curve, during a turn-on event, i.e. when the device switches from the off-state (high drain voltage, zero current) to the on-state (low-drain voltage, high current). At device turn-on, the gate-source voltage V_{GS} increases; when V_{GS} reaches the threshold voltage V_{th}, current starts flowing through the device. At the same time, the gate-source capacitance C_{GS} is charged, until the V_{Miller} voltage (and

the corresponding plateau) is reached. At this point, C_{GS} is completely charged, and the drain current reaches the value fixed by the circuit. At the same time, V_{GS} becomes almost constant, and the drive current starts charging the Miller capacitance C_{GD}. This process goes on until the capacitance C_{GD} is fully charged. When both C_{GS} and C_{GD} are fully charged, the gate voltage starts increasing again. Through this experimental procedure the charges Q_{GS} and Q_{GD} can be calculated. The gate charge $Q_{GS} + Q_{GD}$ is the minimum charge required to turn on the transistor [64], and is thus representative of the switching losses.

A low value of $Q_{GS} + Q_{GD}$ results in the device's ability to achieve high commutation speed (dV/dt), and in a substantial reduction in switching losses [65]. A low gate charge also results in a reduced gate drive power for GaN devices, compared to silicon components [66]. Since, as stated above, the dc losses depend on the $R_{on}W_G$ product, and the ac losses are proportional to Q_G/W_G [35], the $R_{on} \cdot Q_G$ product is an important parameter describing the switching efficiency of a given device. In a recent paper [67], Chen et al. compared devices based on silicon, silicon carbide and gallium nitride in terms of figures of merit. They showed that, for devices with comparable on-resistance, the $R_{on} \cdot Q_G$ product can be around $3800\ m\Omega \cdot \mathrm{nC}$ for a silicon superjunction MOSFET, in the range $1950 - 3480\ m\Omega \cdot \mathrm{nC}$ for SiC-based FETs, and around $290 - 300\ m\Omega \cdot \mathrm{nC}$ for a E-mode GaN transistor. This result indicates that GaN E-mode HEMTs can contribute to a substantial reduction in switching losses, compared to conventional semiconductor transistors.

A further advantage of GaN-based transistors is the absence of reverse-recovery charge. Silicon-based power transistors have an intrinsic body diode, whose presence results in a large reverse recovery charge during commutation. For a silicon superjunction (SJ) MOSFET, the product of on-resistance ($R_{DS,ON}$) and reverse-recovery charge (Q_{rr}) can be in excess of 300 mΩμC [67]. On the other hand, lateral GaN devices are based on the high-electron mobility transistor (HEMT) concept, and do not have any body diode. HEMTs are majority carrier devices, and the lack of minority carriers leads to a near-zero Q_{rr} ($R_{DS,ON}$ x Q_{rr} down to 2.2 mΩμC [67]), with beneficial impact on the switching losses.

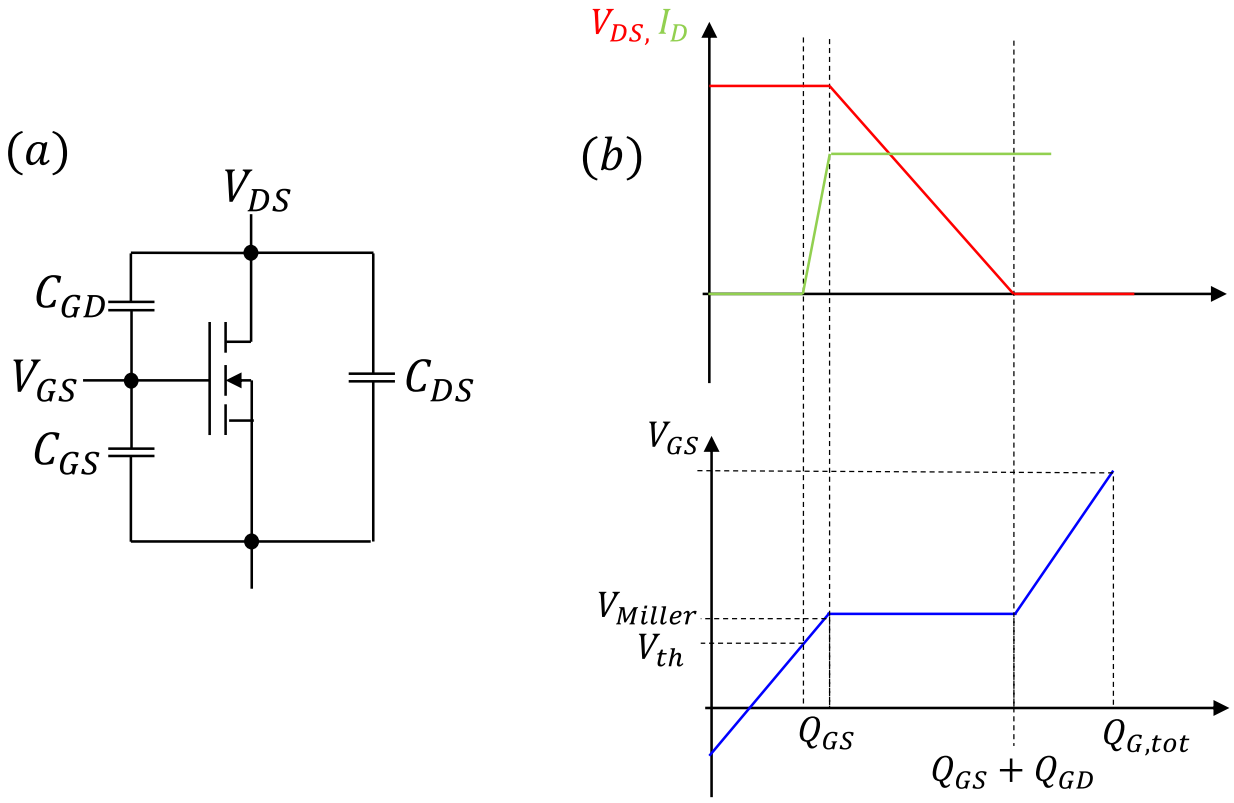


Figure 13: (a) schematic circuit for understanding the dependence of gate charge on gate voltage during device turn-on; (b) voltage, current, and gate charge characteristics for a generic field-effect transistor during a gate-charge measurement

6 Lateral GaN transistors: technology and operation

The rapid evolution of wide bandgap semiconductors in the recent years has positioned lateral GaN transistors as key enablers in the power device market. The interest in power applications has undergone a remarkable shift due to the technological advantages of GaN HEMTs, which allow for simultaneous high voltage, high current and low on-state resistance, resulting in high power and high efficiency operation. In addition, the wide bandwidth provides a robust and reliable technology capable of operating at high frequency and high temperature. This is why GaN-based lateral power electronic devices are emerging as switching components for next generation high-efficiency power converters. Furthermore, GaN-on-Silicon technology platform offers the best cost figures for commercialization of these products, although technologically very challenging. For instance, a complex GaN buffer for stress management and insulation purpose is required. This paves the way for a growing number of applications in various fields, including consumer electronics, transportation and energy, as well as several industrial, automotive and aerospace applications, such as rectifiers and high-voltage converters. As can be seen in Figure 14, each application uses a specific voltage range. In terms of device market, currently, the majority of GaN components are designed for 600/650V applications and below. However, there are few companies that offer devices for 900V applications.

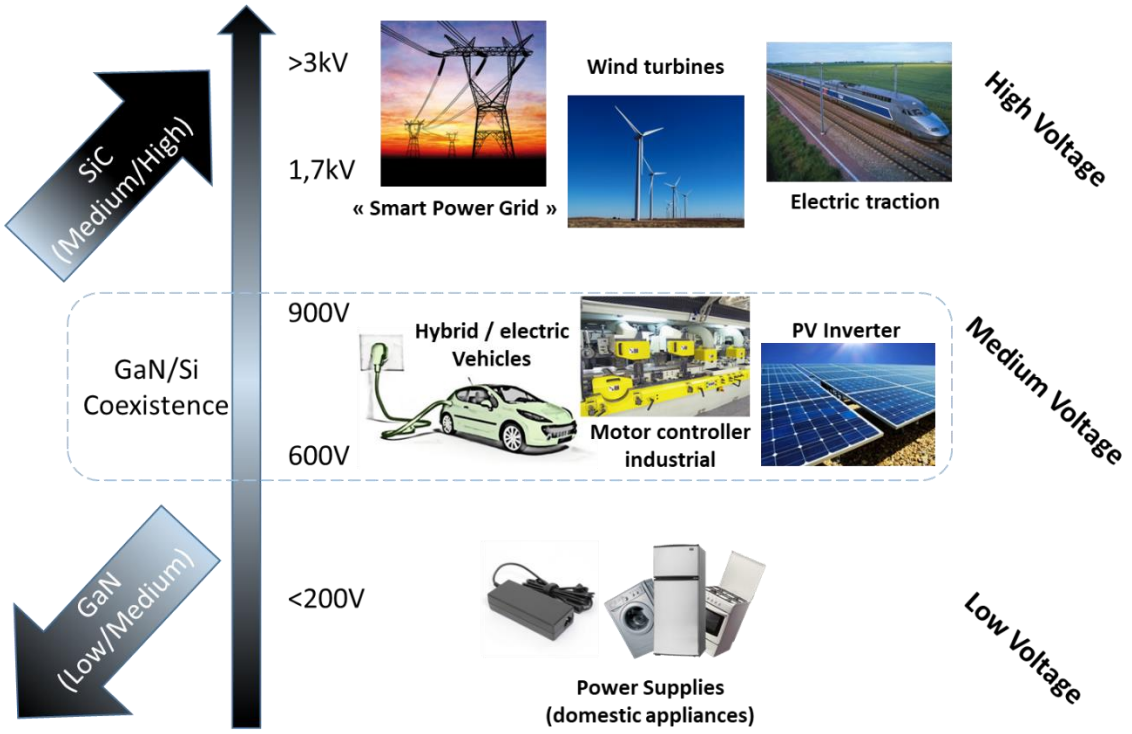


Figure 14: Examples of applications using different voltage ranges

6.1 Lateral GaN device architectures

GaN-on-Si typical HEMT structures (Figure 15) consist of several epi-layers. These layers include materials with a wider bandgap and a lower bandgap, and an AlGaN/GaN heterostructure. At the interface between AlGaN and GaN, a two dimensional electron gas (2DEG) is created with an electron channel accumulation without extrinsic doping. The 2DEG formation results from both the spontaneous and piezoelectric effects [48], [54], [68]. The thickness and Al content of the AlGaN barrier layer defines the resulting polarization. It can be pointed out that a high electron mobility above 2000 cm^2/Vs can be combined with a high carrier density within the 2DEG, thus resulting in excellent electrical performance.

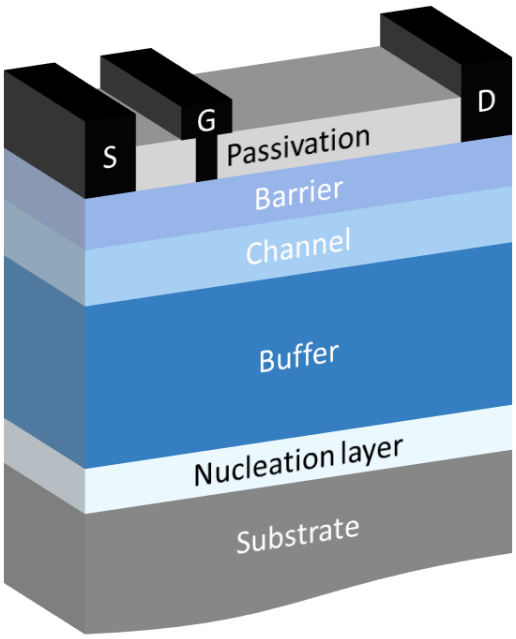


Figure 15: Cross section of a typical AlGaN/GaN HEMT structure

One of the main issues for GaN-based heteroepitaxy is the lattice mismatch and difference in thermal expansion coefficients with the substrate. This generally leads to a high dislocation density, which may be a source of leakage current under high electric field and subsequent device degradation. Residual stress may be created, inducing eventually cracks. The most common materials used as substrates are silicon, sapphire, silicon carbide and more recently bulk GaN. In all cases, the epitaxial layers have rather high dislocation density (10^3 - 10^{10} cm^{-2} [69], [70]). Some properties of the substrates typically used for GaN-based epitaxy are shown in Table 5. For power applications, the Si substrate is preferred because of its low cost and availability in large diameter (up to 12 inches), despite a 17% lattice mismatch and a strong difference in thermal expansion coefficient between GaN and Si, which makes the growth challenging. Although sapphire substrates combine a high resistivity and low cost, the low thermal conductivity leads to a significant self-heating, which is not suitable for power applications. Finally, the high cost of silicon carbide is prohibitive for large volume applications despite its outstanding properties.

Emerging GaN substrates, perfectly lattice-matched, are of interest for vertical GaN architectures, see also Section 7.

In order to grow crack-free and high quality GaN films by reducing the defect density, especially when using silicon substrates, the tensile stress during the growth and cooling process needs to be

limited. An AlN nucleation layer (NL) is typically used as an initiating layer for GaN growth. By using a AlN NL, the melt-back etching of Ga into Si can be avoided [71]. Besides, the AlN NL provides a GaN layer with a compressive strain due to the 2.5% lattice mismatch between AlN and GaN. This is necessary for compensating the tensile stress generated during the cooling process. Figure 16 shows a TEM image of the interface between the Si substrate and the AlN nucleation layer. Dislocations are reduced but still present across the buffer layers.

	Structure	Lattice constants a	Lattice constants c	Thermal conductivity	Lattice mismatch
Unit		nm	nm	W/cm.K	%
Sapphire	Hexagonal	0.476	1.2982	0.25	15
6H-SiC	Hexagonal	0.30806	1.51173	4.9	3.1
Si	Cubic	0.543102		1.56	17

Table 5: Properties of various substrates used for GaN epitaxy [72]

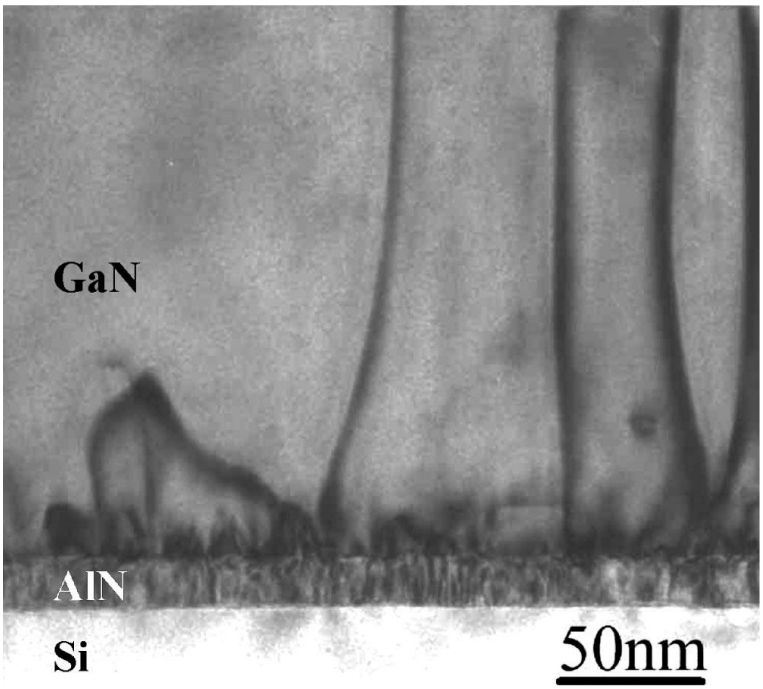


Figure 16: TEM image of a cross section of an AlN/Si interface. Reprinted from R. Liu et al., "Atomic arrangement at the AlN/Si (111) interface" , Applied Physics Letters 83 , 860-862 (2003) https://doi.org/10.1063/1.1597749, with the permission of AIP Publishing [73].

Whatever the choice of substrate, the buffer layers are critical. The high 2DEG sheet charge density in GaN-based HEMTs enables significant drain current densities. Inadequate carrier confinement within the channel leads to soft pinch-off characteristics and high sub-threshold leakage. The presence of a high defect or impurity density in the buffer produces high leakage currents and poor device reliability. Consequently, on top of a high quality AlN NL, a proper buffer configuration and material quality is mandatory.

A well-known approach is the use of a step graded AlGaN buffer, as shown in Figure 17. Several micrometers thick $Al_xGa_{1-x}N$ buffer layers with various Al-content enable to further mitigate lattice and thermal-mismatch detrimental effects. The interest of this approach is also to improve the 2DEG electron confinement under high electric field, by limiting the carrier injection into the buffer layers, i.e. to the so-called punch-through effect. Another practical route to significantly increase the buffer layers' resistivity is the introduction of intentional compensating centers. Iron or carbon doping can be used to produce highly resistive buffers (carbon being the choice for GaN-on-Si GaN devices). Finally, super-lattice (SL) buffers consisting in many periods of thin AlN/GaN pairs have been proved to be one of the most effective techniques both to control the stress and enhance the blocking voltage [74]. With thick SL buffers, a high crystal quality and smooth surface of top-GaN layer can be obtained resulting in superior performance as described further in this paper.

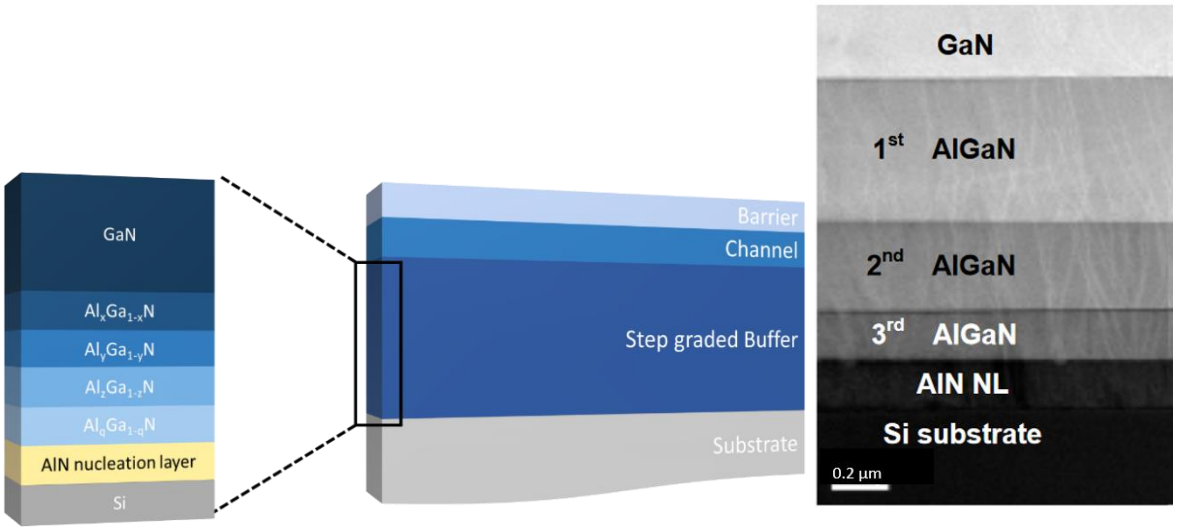


Figure 17: Schematic cross section and TEM image of AlGaN layers with various Al content between the nucleation layer and the GaN layer. Reprinted from "AlGaN/GaN HFET grown on 6-inch diameter Si(111) substrates by MOCVD", S. M. Cho et al., https://doi.org/10.7567/SSDM.2011.AL-7-3, licensed under CC BY [75].

The epitaxial heterostructure is completed with a cap layer, which is generally composed of GaN or SiN to reduce the oxidation of the underlying AlGaN film. It is important to note that surface states [55] on top of the AlGaN constitute the origin of the 2DEG, as discussed in Section 5. However, surface defects may also be detrimental to the device performance. Under operating conditions, trapping at surface defects can create a virtual gate between gate and drain terminals, depleting unintentionally the 2DEG and thus severely degrading the device performances and/or reliability. Negatively charged surface states may compensate the donor atoms, thus depleting the channel between the gate and the drain. A surface passivation layer, typically SiN, allows to mitigate the 2DEG depletion as can be seen in Figure 18.

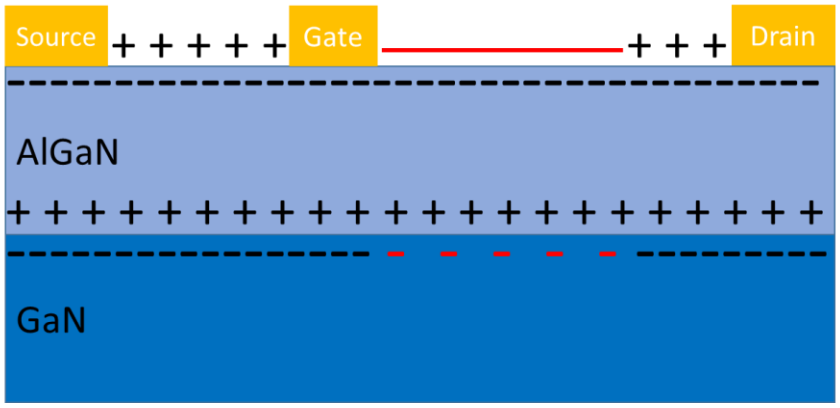


Figure 18: Schematic cross section showing surface state depletion effects within an AlGaN/GaN HEMT

Lateral heterostructure devices are inherently normally-on, i.e. they conduct current when no gate voltage is applied. This raises safety concerns because in case of a malfunctioning gate driver, the GaN transistor is not automatically switched off and an uncontrolled current flow can damage the entire system. Furthermore, normally-on transistors make circuit designs more complex because a negative-voltage supply is required. Thus, a substantial research effort was focused on creating normally-off devices in recent years.

6.2 Approaches for normally-off operation

In a conventional AlGaN/GaN HEMT, the threshold voltage V_{TH} depends on several parameters related to the gate metal and the heterojunction properties, as can be seen from the following equation [76]:

$$V_{TH}(x) = \phi_B(x) - \Delta E_C(x) - \frac{\sigma(x)}{\varepsilon_0 \varepsilon_{AlGaN}(x)} t - \frac{qN_D}{2\varepsilon_0 \varepsilon_{AlGaN}(x)} (\mathrm{t})^2$$

x represents the Al content in the barrier layer; $\phi_B(x)$ is the Schottky barrier height between the gate metal and the AlGaN barrier layer; $\Delta E_C(x)$ is the conduction band discontinuity at the AlGaN/GaN interface; $\sigma(x)$ is the polarization charge at the AlGaN/GaN interface; ε_0 is the permittivity vacuum; $\varepsilon_{AlGaN}(x)$ is the permittivity of the AlGaN layer; t is the AlGaN thickness; q is the electric charge; N_D is the doping.

Thicker AlGaN barriers and higher polarization differences between AlGaN and GaN lead to more negative V_{TH} as they increase n_s at zero bias. From this equation, it is clear that several degrees of freedom exist to tune the V_{TH}, such as changing the Schottky barrier height or the 2DEG carrier density related to the AlGaN barrier layer, which is dependent on the Al content and its thickness.

Different topologies have been proposed in order to achieve normally-off GaN HEMTs: a cascode configuration [77]–[79] combining a silicon normally-off MOSFET and a normally-on GaN HEMT, the use of a HEMT with fluorine implantation under the gate [80]–[82], a gate recessed MISHEMT (metal-insulator-semiconductor) with partial [83], [84] or complete [85] AlGaN barrier removal, and a p-GaN-gated [24], [86], [87] HEMT.

6.2.1 Cascode configuration

The cascode configuration uses a high voltage normally-on GaN HEMT connected in series with a low-voltage silicon MOSFET in the switching circuit, as can be seen in Figure 19. The silicon MOSFET controls the on and off-state switching of the GaN HEMT. When a positive gate voltage above the threshold voltage is applied to the MOSFET, the GaN HEMT gate voltage is close to zero and the device is turned on. As the two devices are connected in series, when a voltage is applied to the drain of the HEMT, the current will also flow through the MOSFET. On the other hand, when no gate voltage is applied to the MOSFET to turn it off, no current can flow through the channel of the HEMT. In addition, any increase of the drain voltage will be handled by the HEMT, thus resulting in a high reliability.

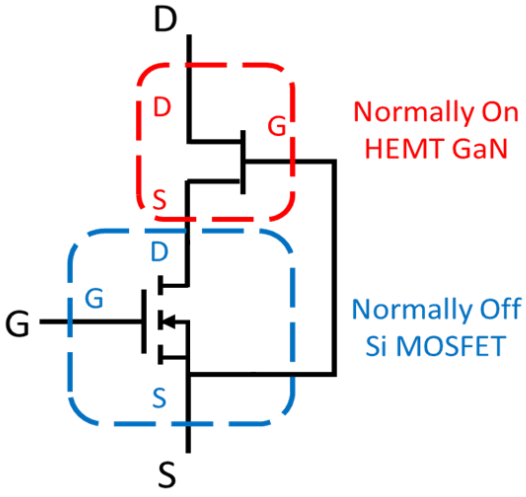


Figure 19: A cascode circuit showing the normally-on HEMT in series connection of a normally-off Si-MOSFET

Therefore, the cascode configuration enables to take advantage of the positive threshold voltage of the MOSFET as well as the low on-resistance of the 2DEG, together with the high breakdown field of the GaN HEMT in off-state conditions. However, it can be noticed that this approach limits the high temperature operation by the presence of the Si device. In addition, the packaging complexity and size are increased and parasitic inductances are introduced, and this may have an impact on the switching performance of the circuit.

6.2.2 Recessed gate MISHEMT

Another approach consists of etching the AlGaN barrier layer under the gate area followed by a deposition of a gate dielectric insulating layer. The AlGaN barrier layer is fully etched by plasma in the gate region (Figure 20). This allows for high threshold voltages, while the thick gate dielectric enables a large maximum forward gate bias (> +10 V).

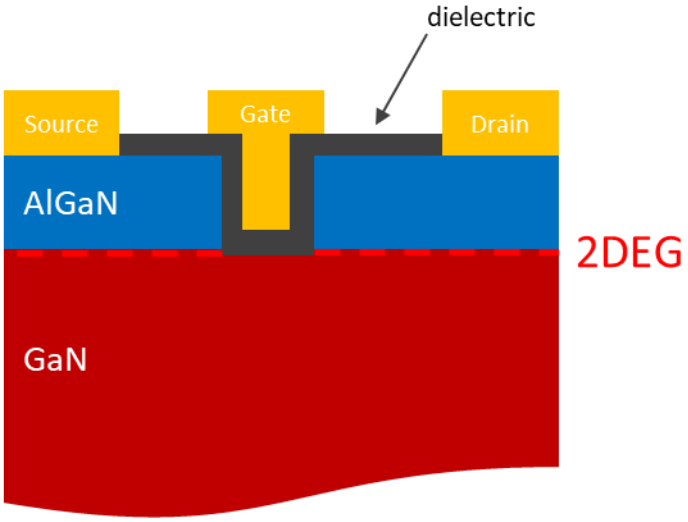


Figure 20: Schematic cross section of a recessed gate GaN MISHEMT

The choice of the dielectric is extremely important, as it will directly impact the channel mobility within the 2DEG [88] and the stability of the threshold voltage [89]. Also, the dielectric quality and surface roughness of the etched area are critical parameters and the interface charge density needs to be well controlled. Several mechanisms, involving the surface states and related trapping

have been proposed to explain the possible origin of the device degradation phenomena (see Sections 8.2 and 8.3).

6.2.3 The "fluorine gate" HEMT

Fluorine ions implanted into the AlGaN layer self-aligned to the gate (see Figure 21) can also create a normally-off behaviour. The negative ions into the barrier change the surface potential, thus depleting the 2DEG. However, the V_{TH} stability after annealing at high temperature and/or under high electric field is a source of concern for this approach [90], [91]. Moreover, previous studies have shown the relation between fluorine and current collapse [92], [93], which may be an issue for power switching applications [92], [94].

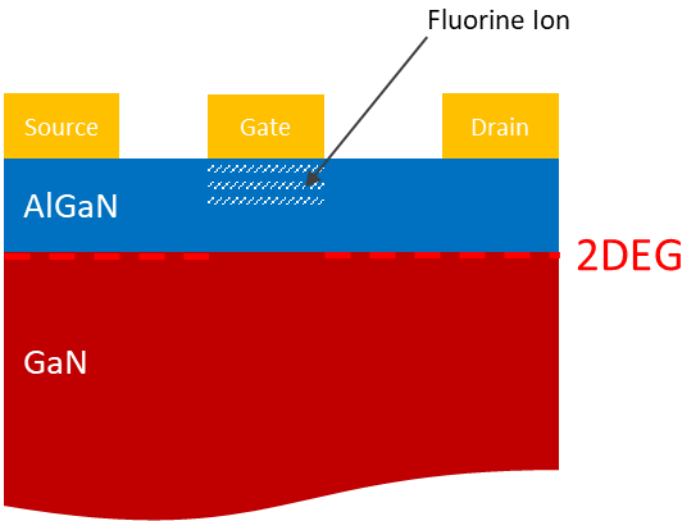


Figure 21: Schematic cross section of a F−doped GaN HEMT.

6.2.4 P-GaN Gate

An attractive method to achieve normally-off GaN transistors is the use of a p-doped GaN layer [95] under the gate area (Figure 22). The presence of the p-GaN layer lifts the band diagram to higher energies (Figure 23), so that the 2DEG depletion occurs even in the absence of an applied external bias. In order to maximize the 2DEG depletion induced by the p-GaN cap layer, the Al mole fraction in the barrier and the thickness of the barrier must be carefully optimized. It has been demonstrated that to achieve a good depletion of the 2DEG, the Al content and thickness of the barrier should be kept relatively low [96]. Greco *et al* determined the energy band diagram by

Schrödinger-Poisson (Figure 24) of two structures with an identical barrier thicknesses (25nm) but different Al content (12% and 26%), by using a p-GaN layer thickness of 50 nm with an acceptor concentration of $3\times10^{19}cm^{-3}$. Figure 24 clearly shows that despite the presence of the p-GaN layer, the high Al content structure still exhibits normally-on behaviour with the conduction band below the Fermi level at the AlGaN/GaN interface; on the contrary, the structure with reduced Al content can reach normally-off operation. Similarly, the conduction band diagram of p-GaN/AlGaN/GaN heterojunctions with two different barrier thicknesses (10 nm and 25 nm, with a fixed Al content of 26 %) has been simulated. As can be noticed, the structure with a thickness of 25 nm reveals a normally-on behavior, whereas the thinner barrier results in normally-off devices. Based on a series of tests, a summary graph can be produced showing the normally-on and normally-off area with respect to the thickness and Al content of the AlGaN barrier layer (Figure 25).

Also, a high Mg concentration in the p-GaN layer is required, which should be balanced with the deterioration of the crystal quality for too high Mg doping concentration. The p-GaN layer has shown a wide process window in terms of thickness and doping, which eases process control requirements. However, the low selectivity of the etching process between the p-GaN and the barrier layer needs to be carefully optimized in order to achieve a stable high threshold voltage [92].

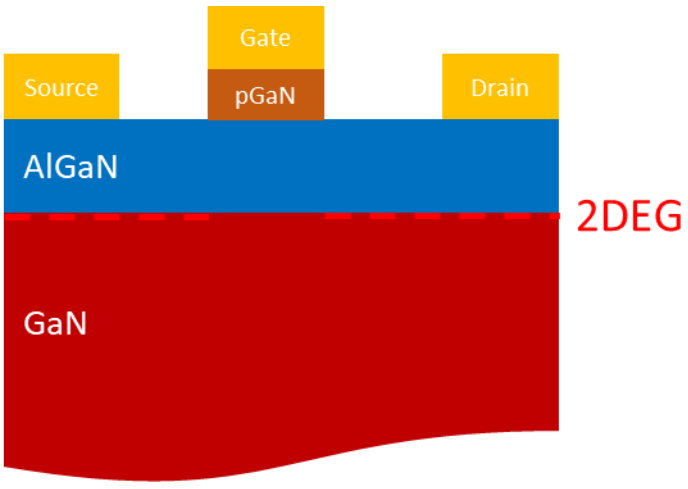


Figure 22: Schematic cross section of a p-GaN gate GaN HEMT.

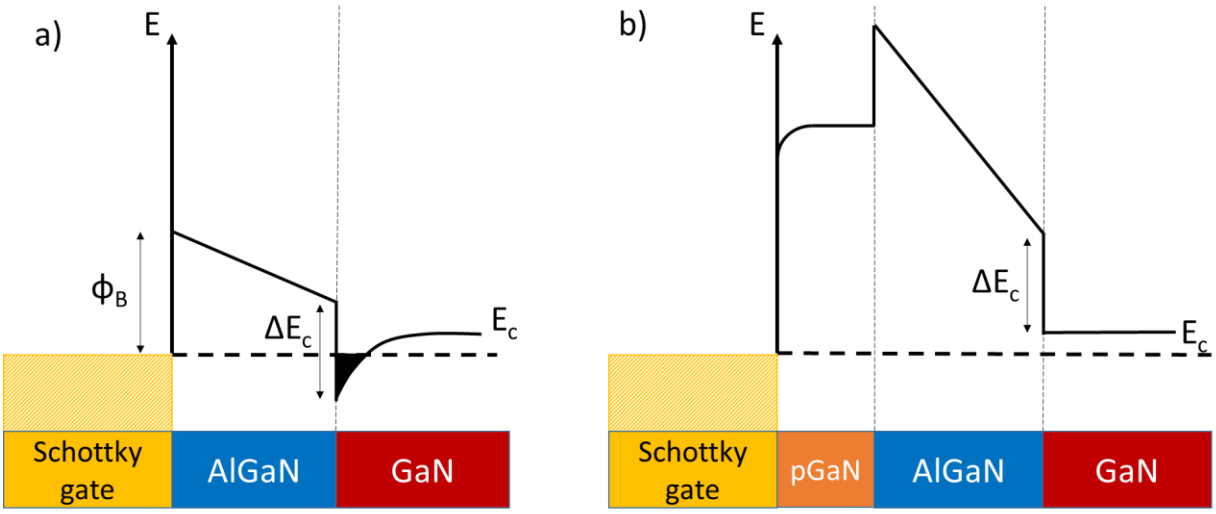


Figure 23: Band diagram of an AlGaN/GaN heterostructure with a) and without b) p-GaN layer. Reprinted from Materials Science in Semiconductor Processing, Volume 78, G. Greco, F. Iucolano, F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate", Pages 96-106, Copyright 2018, with permission from Elsevier (10.1016/j.mssp.2017.09.027) [92].

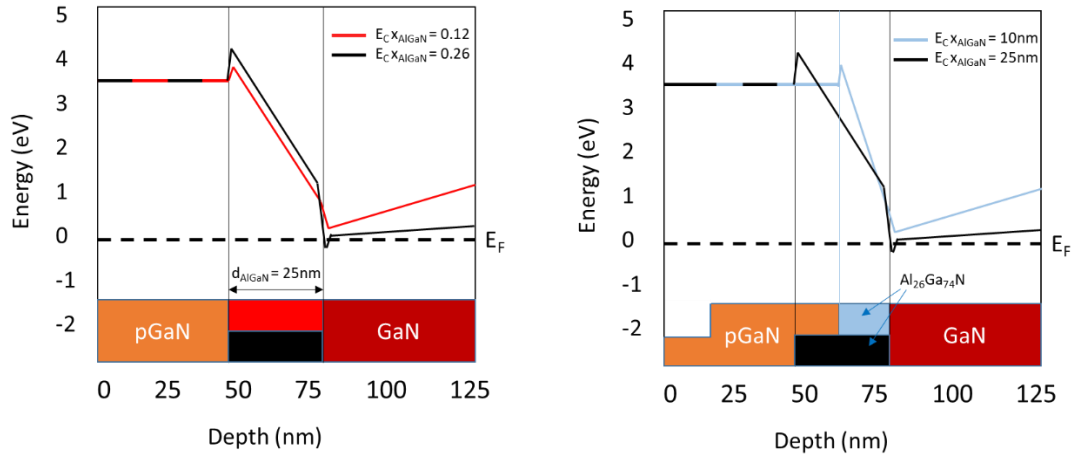


Figure 24: Simulated conduction band diagrams of a p-GaN/AlGaN/GaN heterostructure for two different Al content (12% and 26%) into the AlGaN barrier layer (left) and two different AlGaN barrier thickness (right). Reprinted from Materials Science in Semiconductor Processing, Volume 78, G. Greco, F. Iucolano, F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate", Pages 96-106, Copyright 2018, with permission from Elsevier [92].

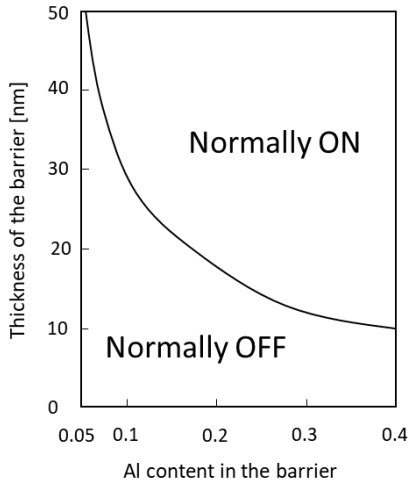


Figure 25: Device operation modes as a function of the Al content and the thickness of the barrier. Reprinted from Materials Science in Semiconductor Processing, Volume 78, G. Greco, F. Iucolano, F. Roccaforte, "Review of technology for normally-off HEMTs with p-GaN gate", Pages 96-106, Copyright 2018, with permission from Elsevier [92].

Another parameter not to be neglected is the choice of the gate metal. The Schottky barrier height between the metal and the p-GaN layer directly impacts the threshold voltage and follows the relation:

$$\phi_B = \frac{E_g}{q} - (\phi_m - \chi_s)$$

where ϕ_B is the Schottky barrier height between the gate metal and the AlGaN barrier layer; E_g is the bandgap of the semiconductor; ϕ_m is the work function of the metal; and χ_s is the electron affinity of the semiconductor.

Based on this equation, metals with a lower work function provide a higher barrier height [97].

6.3 Breakdown mechanisms

Converters based on MOSFET have the ability to survive a limited exposure to voltages above the device rating, according to the specified avalanche energy rating. However, lateral GaN HFETs do not have the potential for avalanche breakdown [98], because they do not rely on a p-n junction

for blocking voltage and may experience catastrophic dielectric breakdown when exposed to sufficient overvoltage [99]. This breakdown is destructive and non-recoverable.

The main sources of leakage current and related breakdown voltage (V_{BR}) for an AlGaN/GaN HEMT power transistor on Si substrate are the following (see Figure 26):

- Punch-through effect reflecting a parasitic electron injection into the buffer.
- Leakage current through the passivation layer and/or due to a surface related conduction.
- Vertical breakdown, through the total buffer thickness, that can be due to a poor doping compensation of the buffer.

Different approaches have been developed in order to mitigate these leakage paths and associated premature breakdown while avoiding trapping effects.

- The use of high-quality dielectric for surface passivation reduces leakage at the surface and at the interface with the barrier [100].

- Proper doping compensation into the buffer layers, generally carbon or iron doping [101]–[103] enables to significantly enhance the buffer resistivity and consequently avoid the carrier injection. Furthermore, back barrier [104], [105] based on graded AlGaN or AlN material have been developed in order to reduce this phenomenon, increasing the blocking voltage. In both cases, the thickness of the GaN channel region must be carefully optimized with the aim of achieving a high electron density in the 2DEG, a good electron confinement in the channel, and low trapping effects, especially in the case of doping compensation [106], [107].

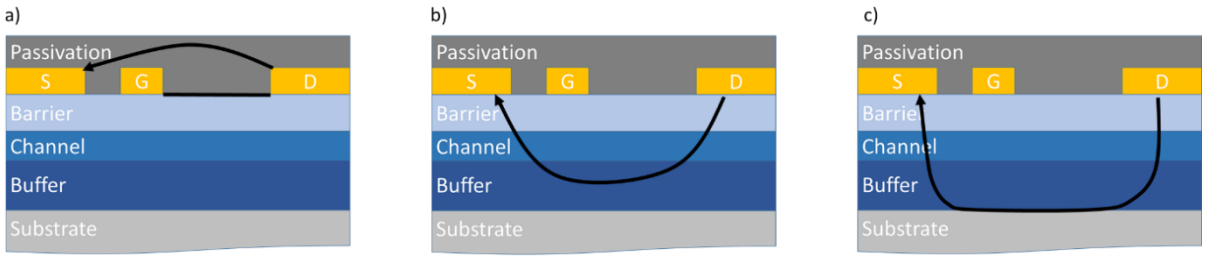


Figure 26: Schematic representation of the main sources of leakage current for AlGaN/GaN transistors on Si

It can be pointed out that the AlGaN/GaN transistor breakdown voltage scales linearly for small gate-drain distances (typically below 15 µm), while larger gate-drain distances result in a saturation of V_{BR} due to the conduction into the substrate triggered by the vertical electric field. Extensive research is carried out to overcome the breakdown mechanisms and further push the limits of GaN-on-Si HEMTs.

In addition, the crystal quality is an important factor. Considering the high material defect density in GaN/Si epilayers, recent studies [108], [109] showed that the presence of defects may impact on the breakdown voltage.

6.4 Ways to improve the breakdown voltage

6.4.1 Buffer optimization: Super-lattice buffer

Unintentionally doped GaN buffer layers deliver insufficient resistivity for high voltage operation, due to the residual n-type conductivity of GaN, which can induce parasitic leakage paths, thus increasing the off-state leakage current. As previously mentioned, high resistivity can be achieved by doping with deep acceptor impurities (such as C atoms), to compensate the background donors. However, this approach can generate severe current collapse, if the buffer is not carefully optimized [110]–[112].

To further improve the carrier confinement while suppressing undesirable trapping effects, the doping compensation can be combined with the use of an AlGaN back barrier [74] or super-lattices [113], [114] consisting in AlN/GaN pairs (see Figure 27). By alternating thin layers of high crystalline quality wide-bandgap semiconductors (e.g. AlGaN, AlN or GaN), the accumulation of internal stress can be minimized, thus creating a highly insulating buffer with low buffer trapping effects.

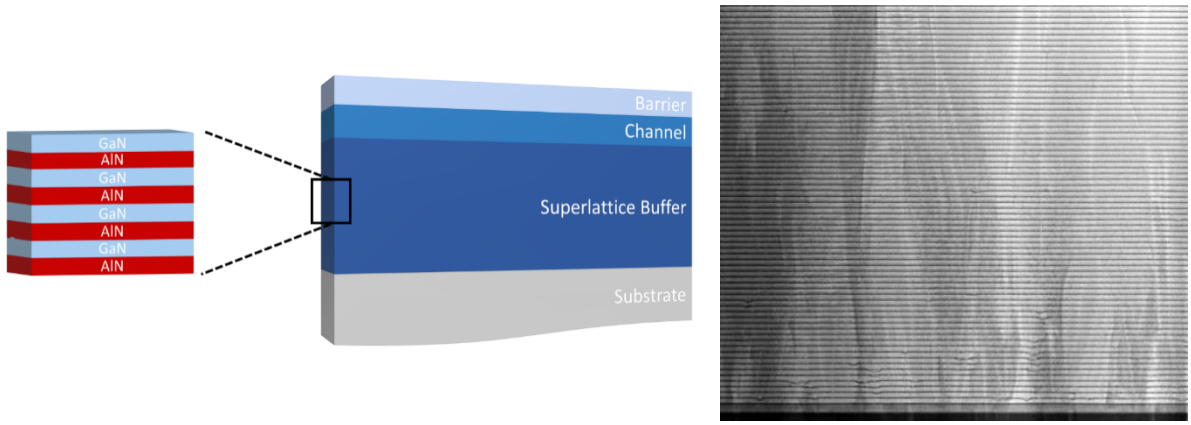


Figure 27: Schematic cross section of a GaN HEMT using a super-lattice-based buffer and TEM image of an AlN/GaN superlattice

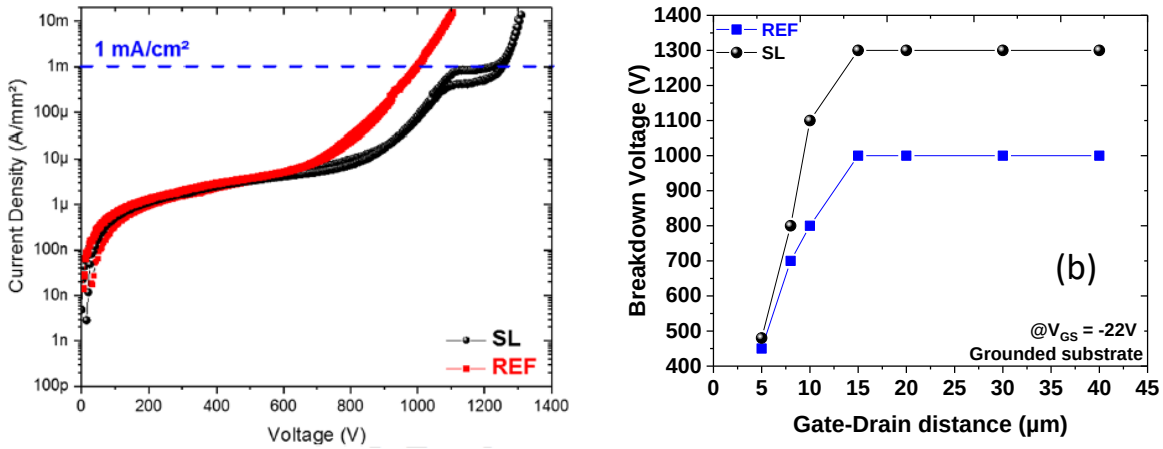


Figure 28: Vertical breakdown of a step-graded GaN Carbon doped buffer (REF) and a SL structure (black) at room temperature. Reprinted from "High Breakdown Voltage and Low Buffer Trapping in Superlattice GaN-on-Silicon Heterostructures for High Voltage Applications", A. Tajalli et al., https://doi.org/10.3390/ma13194271, licensed under CC BY 4.0 [74].

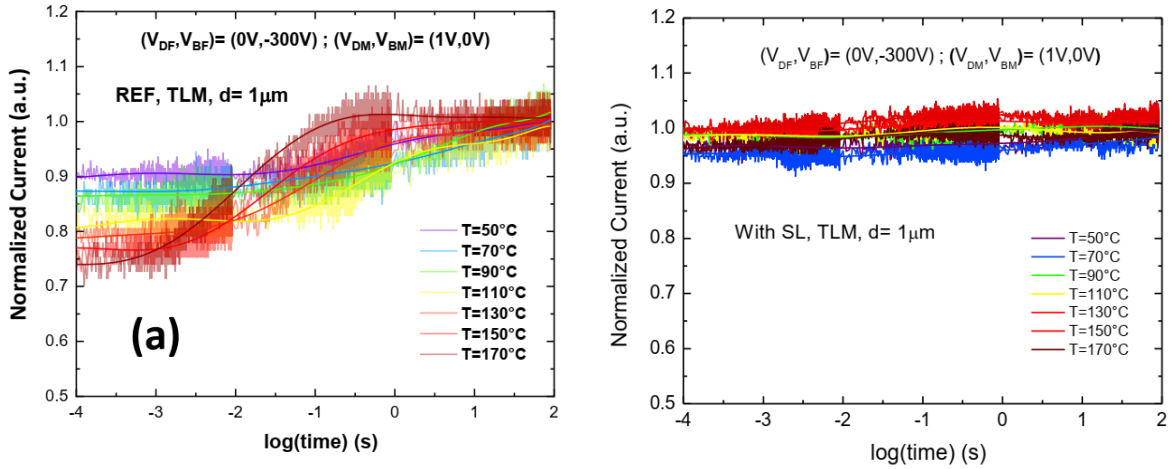


Figure 29: Current transient behavior at multiple temperatures up to 170 °C using a 1 µm distance TLM on a step-graded buffer (left) and a super-lattice buffer (right). Reprinted from "High Breakdown Voltage and Low Buffer Trapping in Superlattice GaN-on-Silicon Heterostructures for High Voltage Applications", A. Tajalli et al., https://doi.org/10.3390/ma13194271, licensed under CC BY 4.0 [74].

A. Tajalli *et al* showed that the insertion of super-lattices (SL) into the buffer layers allows pushing the vertical breakdown voltage above 1200 V without generating additional trapping effects as compared to a more standard optimized step-graded AlGaN-based epi-structure using a similar total buffer thickness (see Figure 28). dc characterization of fabricated transistors by means of back-gating transient measurements reflect the much lower trapping effects and the benefit of the SL (Figure 29).

6.4.2 Local substrate removal

A limiting factor for the breakdown voltage of GaN-on-Si transistors is the poor critical electrical field strength of the Si substrate, together with a parasitic conduction at the buffer/substrate interface. In order to suppress the parasitic conduction phenomenon, local Si substrate removal (LSR) [115] has been shown to be very effective leading to significantly improved blocking voltage up to 3 kV [25], [116].

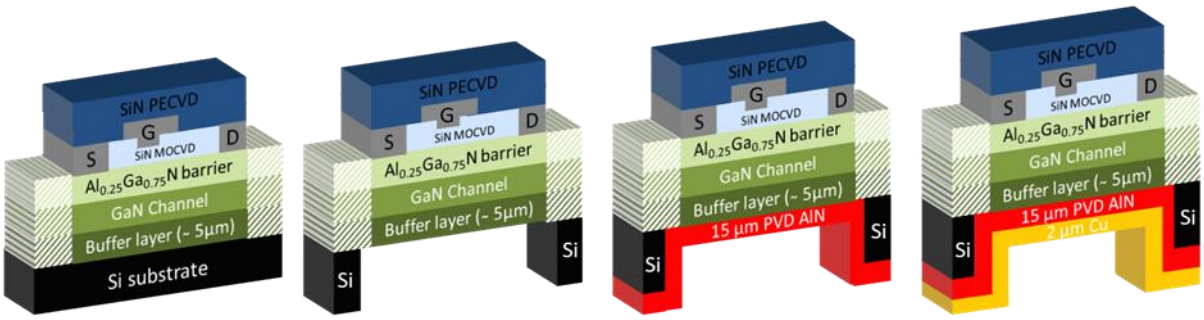


Figure 30: Schematic cross-section of AlGaN/GaN MISHEMT including the front side process, the LSR technique, a thick PVD AlN and metal backside deposition. Reprinted from "GaN-on-silicon high-electron-mobility transistor technology with ultra-low leakage up to 3000 V using local substrate removal and AlN ultra-wide bandgap", Ezgi Dogmus et al., Appl. Phys. Express, https://doi.org/10.7567/APEX.11.034102, licensed under CC BY 4.0 [25].

E. Dogmus *et al* used the following device processing, which consists in ohmic contacts formed directly on top of the AlGaN barrier by rapid thermal annealing. After device isolation, a metal-insulator-semiconductor gate structure was employed by depositing Ni/Au metal stack on top of the in-situ SiN cap layer. Once the front-side processing was completed, the Si substrate is locally etched up to the AlN nucleation layer around the entire device (see Figure 30). Devices with and without LSR have been fabricated on the same samples, eliminating any processing or epi variation during the device characterization. Electrical characterization showed a slight decrease of the maximum current density after LSR as can be seen in Figure 31 due to self-heating effects [33]. Further improvement of the heat dissipation would be required to avoid the decrease of the current density. On the other hand, a drastic enhancement of the blocking voltage is achieved by locally replacing the substrate with a wider bandgap material (Figure 32).

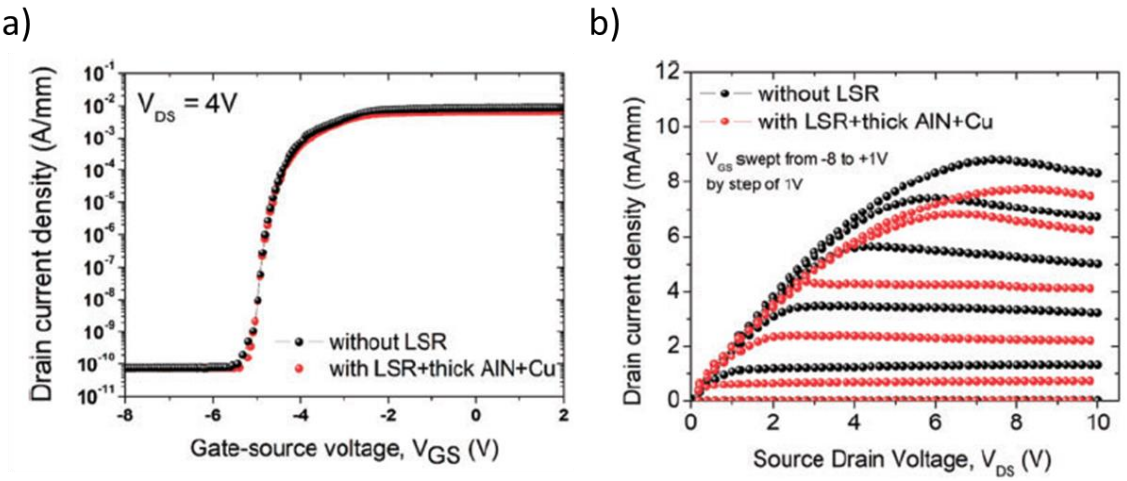


Figure 31: (a) Transfer and (b) output characteristics of GaN-based MISHEMTs with and without LSR/backside AlN and Cu. Reprinted from "GaN-on-silicon high-electron-mobility transistor technology with ultra-low leakage up to 3000 V using local substrate removal and AlN ultra-wide bandgap", Ezgi Dogmus et al., Appl. Phys. Express, https://doi.org/10.7567/APEX.11.034102, licensed under CC BY 4.0 [25].

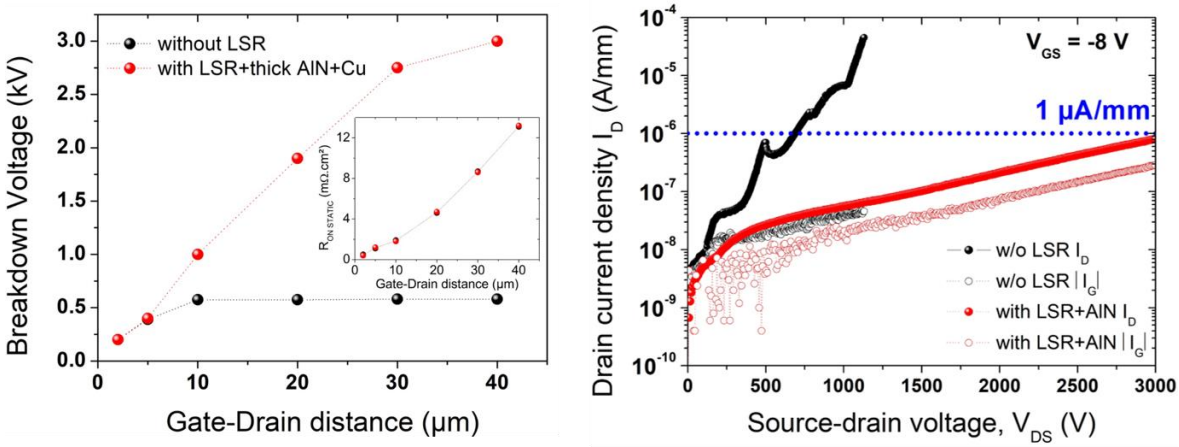
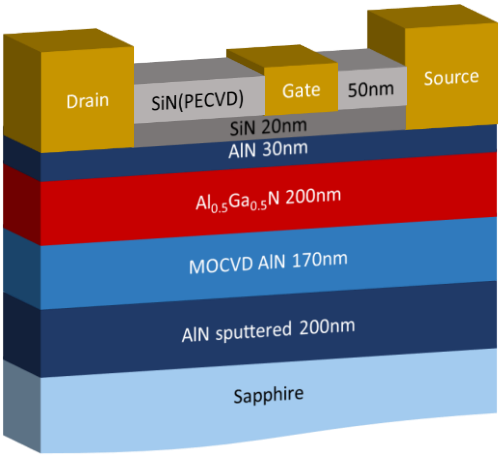


Figure 32: (left) Evolution of L_{GD}-dependent device V_{BR} and specific on-resistance (inset) of AlGaN/GaN HEMTs with and without LSR by defining the blocking voltage at I_D =1μA/mm, and (right) off-state leakage current characteristics of AlGaN/GaN MISHEMTs with and without LSR. Reprinted from "GaN-on-silicon high-electron-mobility transistor technology with ultra-low leakage up to 3000 V using local substrate removal and AlN ultra-wide bandgap", Ezgi Dogmus et al., Appl. Phys. Express, https://doi.org/10.7567/APEX.11.034102, licensed under CC BY 4.0 [25].

Furthermore, the effects of Si removal were investigated by Raman thermometry [116], [117], which revealed a worsening of the thermal performance. A significant improvement of the thermal dissipation is obtained after the AlN and copper deposition.

6.4.3 AlN-based power devices

Ultra-wide band gap materials such as AlN (6.2 eV) and related Al-rich AlGaN channel could allow for further improvement, especially in terms of voltage and temperature operations. This is primarily due to their much higher critical electric field resulting from a wider bandgap (see Figure 3). In addition, the use of an AlN back barrier would enable to both increase the electron confinement in the transistor channel and enhance the thermal dissipation. It has already been demonstrated that for extremely high temperature electronics, the properties of Al-rich transistors [118]–[120] are showing favorable comparisons to conventional wide bandgap materials. Despite the difficulty to achieve very high voltage operations due to the material quality and the ability to implement high Al content above 50%, some recent attempts showed the premise of voltage enhancement with AlGaN channels together with superior thermal stability.



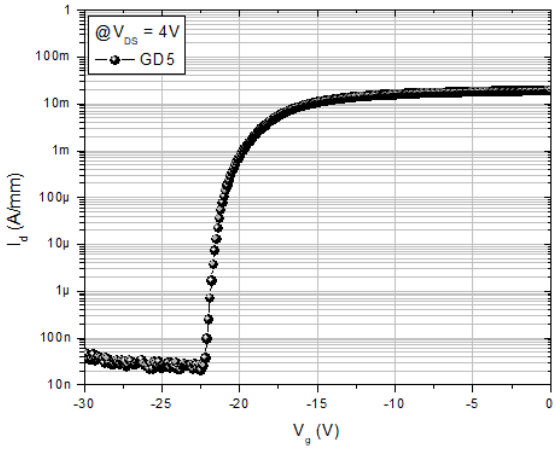


Figure 33: Schematic cross section and typical transfer characteristic at V_{DS} = 4V of an Al-rich AlN/AlGaN/AlN HEMTs [121]

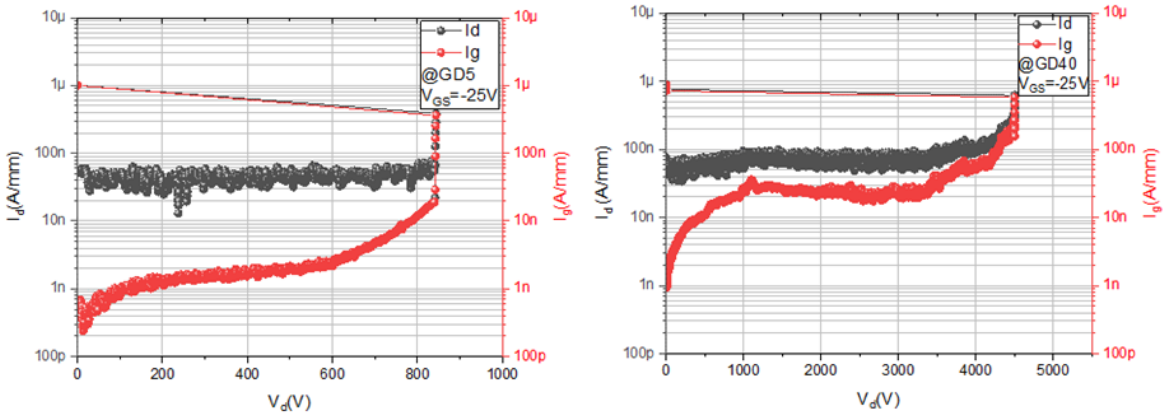


Figure 34: Three-terminal breakdown voltage of AlN/AlGaN/AlN with L_{GD}=5 µm (GD5) (left) and L_{GD}=40 µm GD40 (right) [121].

Abid *et al*. used an AlN barrier on top of an $Al_{50}Ga_{50}N$ channel grown on an AlN/sapphire template (Figure 33). The heterostructure provides a high carrier concentration close to 1.9×10^{13} cm^{-2} with a rather limited electron mobility of 145 $cm^2/V.s$. Low leakage current is obtained without the use of any field plates, confirming that tunneling mechanisms are not present in Al-rich transistors. In general, Al-rich transistors are less prone to gate leakage than AlGaN/GaN HEMTs. Despite the rather high defect density, a blocking voltage above of 4000 V with an off-state leakage current below 0.1 µA/mm is achieved for AlGaN-based channel HEMTs (Figure 34). It can be noticed that low gate-drain distance of 5 µm yields a breakdown field of 3.5 MV/cm, which is well-beyond that of SiC and GaN devices. Furthermore, these transistors show a very stable behavior as a function of temperature, with no threshold voltage variation and low off-state leakage increase up to 200°C.

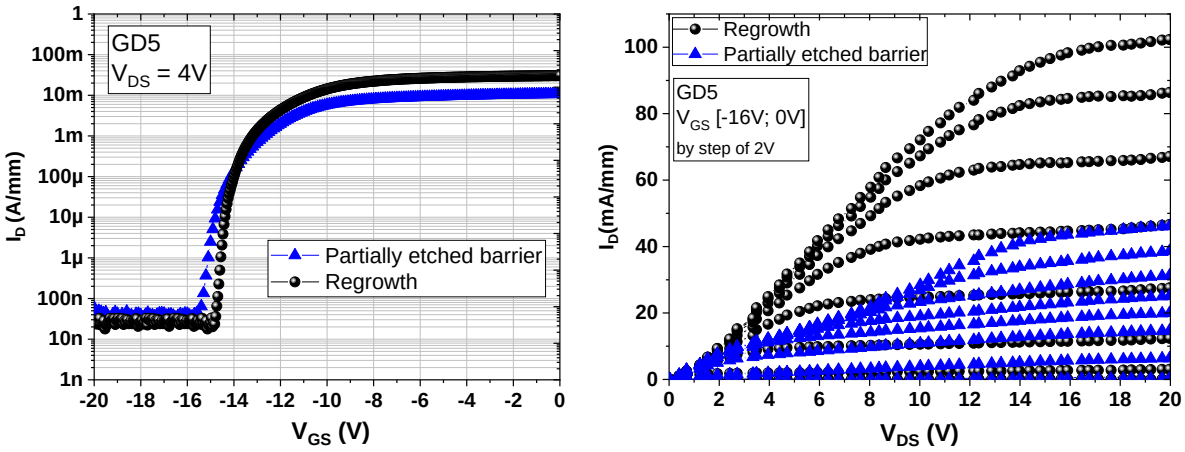


Figure 35: Transfer characteristics (left) and output characteristics (right) of AlN/AlGaN/AlN HEMTs using regrown ohmic contacts and partially etched barrier

One of the major challenges limiting the research progress of Al-rich AlGaN transistors is the optimization of ohmic contacts. High resistance of the source and drain electrodes, and the possible Schottky-like behavior, lead to a reduced current density. Low resistance ohmic contacts are fundamental performance enablers in wide bandgap HEMTs. Several approaches [122]–[125] are under development to mitigate this issue, namely based on tuning the heterostructure and/or the subsequent annealing. For instance, regrown ohmic contacts using a SiO_2 mask can be applied. The reduction of the contact resistances has been verified at the transistor level. Output characteristics of transistors with regrown non-alloyed contacts showed a significant current density increase above 100 mA/mm as compared to identical devices with partially etched barrier and annealed contacts (see Figure 35). This is clearly resulting from the drastic drop of the contact resistances. In spite of these obstacles, preliminary results show that contact resistivity will improve over time and that advanced approaches such as the etch and regrowth processes will ensure successful achievement at even higher Al-composition.

6.5 Future perspectives

As the AlGaN/GaN power technology is reaching its maturity and increasing its market share, the research on this topic is likely to follow two parallel paths. On one hand, there will be a growing interest on the aspects directly related to the realization of a successful commercial product such as trapping, reliability, stability, packaging, and circuit operation. On the other hand, researchers

will continue to come up with novel device structures and designs to improve performance and take full advance of the GaN material properties for future generations of high efficiency devices. Under this point of view, a few recent promising directions are presented below which are rapidly growing and offer a significant advance in device performance.

6.5.1 Multi-channel devices

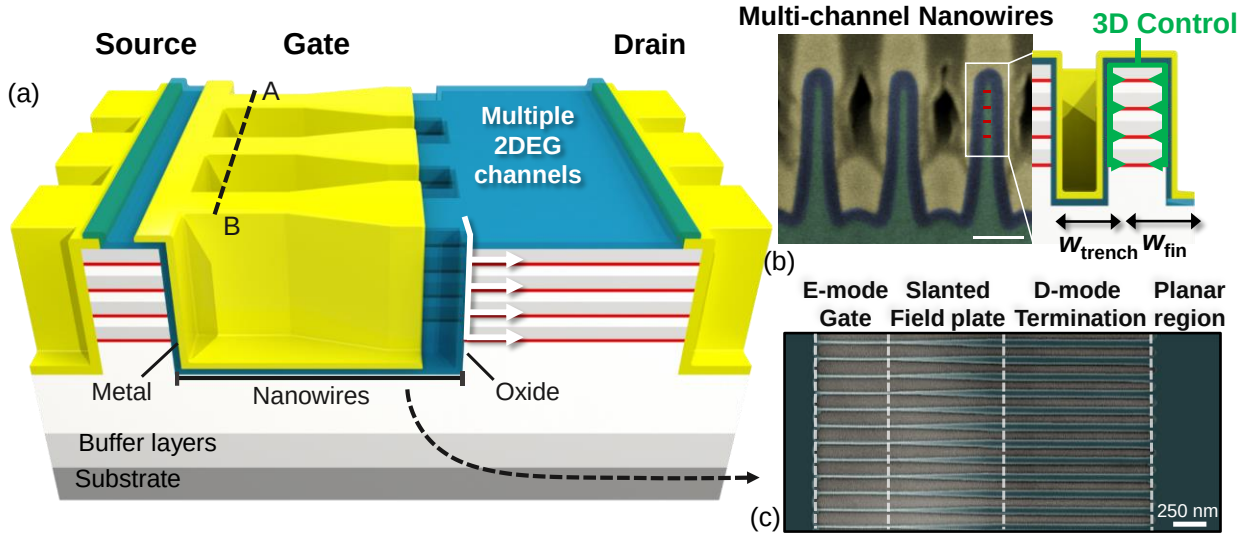


Figure 36: Three-dimensional schematics of the multi-channel power device, featuring multiple parallel channels, controlled 3-dimensionally by a tri-gate electrode. (b) FIB cross-section and schematics of the multi-channel nanowires covered by the tri-gate structure along the AB line in figure (a). The scale bar is 100 nm. (c) Top SEM image of the tri-gate area which includes, starting from the source side, an e-mode region achieved by 15 nm-wide nanowires, and a slanted region terminated on 100 nm-wide d-mode nanowires for optimal electric field management. Reprinted by permission from: Springer Nature, Nature electronics, "Multi-channel nanowire devices for efficient power conversion", L. Nela et al., Copyright 2021 [126].

Despite the recent progress, the performance of AlGaN/GaN devices is still far from the theoretical limit predicted for the GaN materials [127]. A direct way to improve the device's performance is represented by increasing its carrier concentration, which directly leads to a reduced on-resistance. Yet, achieving a large n_s leads to major challenges for the heterostructure and device design. First, a large n_s severely impacts the mobility (μ) due to the increased electron-to-electron scattering,

limiting the reduction of the heterostructure R_{sh}. Secondly, a large n_s leads to a difficult control of the channel, which results in negative V_{TH} and degrades the device voltage blocking capability.

A promising approach to address these challenges is represented by the use of a multi-channel heterostructure, in which several barrier/channel layers are stacked to achieve multiple 2DEGs [128]–[131] (Figure 36 (a)). This allows to distribute a large n_s in several parallel channels thus overcoming the trade-off between n_s and μ and considerably increasing the heterostructure conductivity. On the other hand, the multi-channel heterostructure can be combined with a tri-gate architecture which allows to gain excellent control over all of the embedded channels and manage the large off-state electric field (Figure 36).

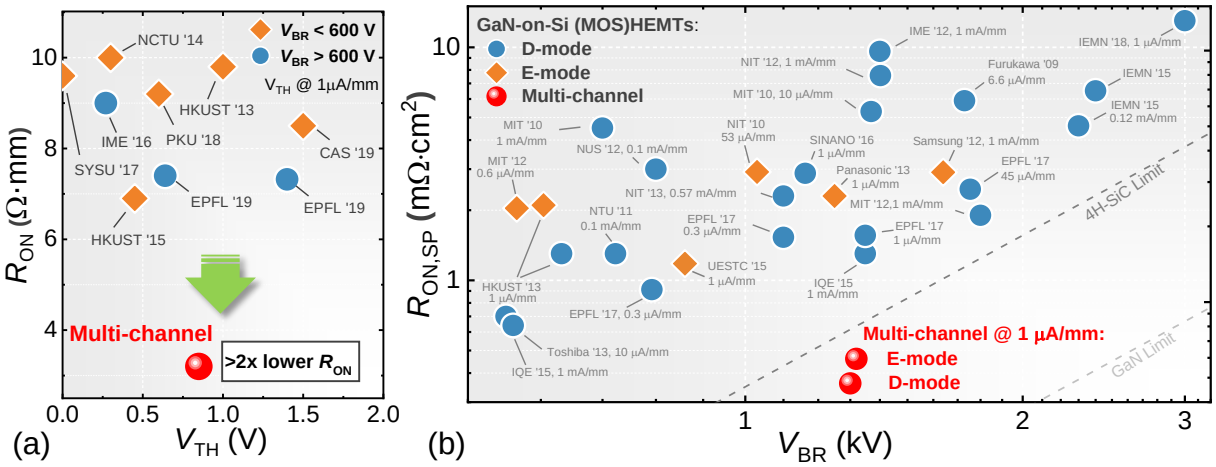


Figure 37 R_{ON} vs V_{TH} benchmark for the multi-channel device against state-of-the-art power devices. V_{TH} has been defined at 1 μA/mm. (c) $R_{ON,SP}$ vs V_{BR} benchmark for normally-off and D-mode Multi-channel devices with respect to state-of-the-art GaN-on-Si (MOS)HEMTs. Reprinted by permission from: Springer Nature, Nature electronics, "Multi-channel nanowire devices for efficient power conversion", L. Nela et al., Copyright 2021 [126].

While multi-channel devices have first been proposed for RF applications [132]–[135], there has been a growing interest in their use in power electronics applications. However, power devices present very specific requirements such as normally-off operation, large blocking voltage capabilities and good stability during switching operation, which need to be separately addressed and solved. The first power multi-channel power HEMT was reported in 2018 [136], followed by the demonstration of a high-voltage multi-channel SBD [137]. While these early works showed the concept of multi-channel power devices, their performance improvement was still quite limited due to the relatively high sheet resistance (~ 240 Ω/sq) of the multi-channel heterostructure employed. More recent works [126], [138], [139], however, showed the full potential of the multi-

channel technology for power devices. By employing a highly conducting multi-channel heterostructure (R_{sh} of 83 Ω/sq) in combination with a carefully designed slanted tri-gate structure, multi-channel power devices showing normally-off operation with V_{TH} of 0.85 V (at 1 μA/mm), on-resistance of 3.2 Ω·mm and breakdown voltage of 1300 V (at 1 μA/mm) were demonstrated [126]. Such performance considerably surpasses the state-of-the-art of conventional single-channel devices and opens new perspectives for GaN power devices (Figure 37). Besides, multi-channel devices passivated by low-pressure chemical vapor deposition (LPCVD) Si_3N_4 presented reduced current collapse up to high voltage stress and excellent V_{TH} stability both during switching and high-temperature operation, showing the potential of such technology [140]. Further research on this topic will likely concentrate on the optimization of the multi-channel heterostructure and on additional methods to achieve large positive V_{TH}.

6.5.2 Super Junctions

Super Junction (SJ) devices have revolutionized silicon power devices leading to unprecedented performance well beyond the one-dimensional material limit [142], [143]. It is thus likely that eventually power devices based on other semiconductor material will embrace this technology too. In particular, the demonstration of SJs realized with wide bandgap (WBG) semiconductors would result in a major further improvement for power devices performance [144]–[146].

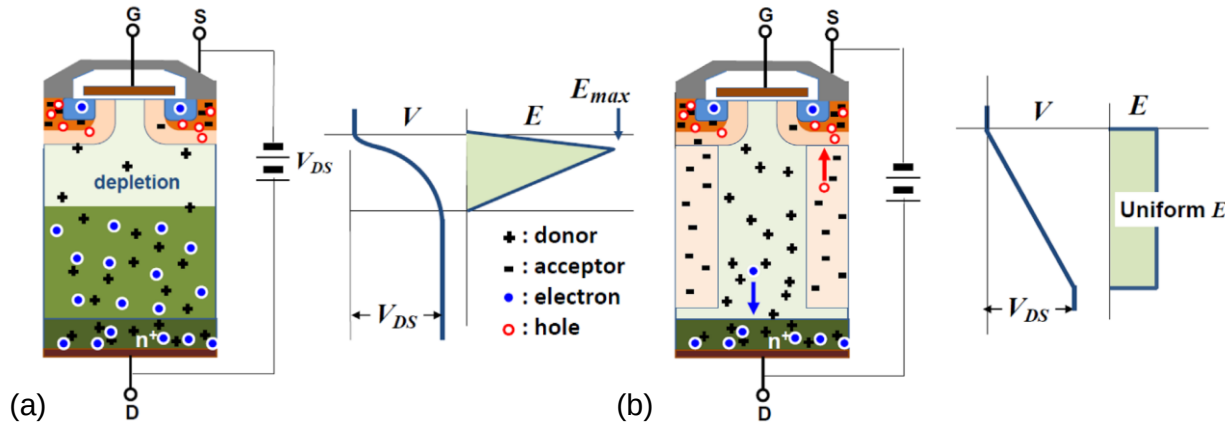


Figure 38 Schematic of the cross-section of a conventional power MOSFET (a) and a super junction device (b) with the corresponding electric field distribution under off-state conditions. Reprinted from: H. Kawai et al., "Low cost high voltage GaN polarization superjunction field effect transistors", Wiley & Sons, Copyright 2017 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim [141].

The realization of conventional vertical SJ (Figure 38) in GaN is however not straightforward due

to difficult technological challenges, among which the inefficient Mg-based *p*-doping of GaN is one of the most relevant. On the one side, the reduced Mg activation ratio results in relatively low doping concentrations, which, combined with the difficult control of the exact doping level, make charge-matching extremely challenging. On the other side, the absence of efficient implantation doping and high-quality *p*-GaN regrowth, hinder the realization of the typical vertical SJ pillars. These challenges make the demonstration of vertical GaN SJ devices still out of reach and, until more efficient p-GaN doping is achieved, it is unlikely that this technology could progress significantly.

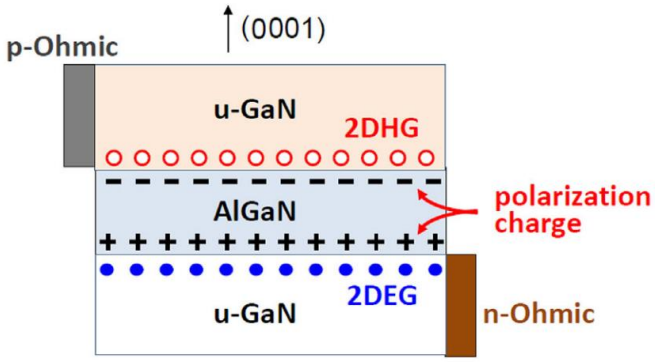


Figure 39 Schematic illustration of a PSJ structure. Reprinted from: H. Kawai et al., "Low cost high voltage GaN polarization superjunction field effect transistors", Wiley & Sons, Copyright 2017 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim [141].

Yet, alternative solutions to realize SJ devices have been proposed in AlGaN/GaN lateral architectures. In these structures, it is possible to obtain a two-dimensional electron and hole gas (2DEG and 2DHG) of equal concentration thanks to the presence of matching polarization charges. Such devices are typically referred to as polarization super junctions (PSJs) (Figure 39) and can result in similar behavior to conventional, doping-based SJs, thus yielding much-improved off-state performance. While these devices were first proposed in 2008 [147]–[149], technical challenges in achieving a good match between the 2DEG and 2DHG concentrations have slowed the development of this technology. After some years, the research on this subject has regained a strong interest and several works have recently appeared on this topic [141], [150]–[152], providing further insight on the devices working principle and showing its potential. Fast development of this field in the next years is thus expected, which could result in a new generation of GaN super-junction devices.

7 Vertical GaN device structures

7.1 Why Vertical GaN?

The most common GaN-based power devices available presently are GaN HEMTs, which have been discussed in detail in the previous sections. GaN HEMTs rated for 650 V/900 V breakdown voltage (BV) and maximum output DC current (I_{DS}) as high as 150 A are available commercially [153]–[155] for a broad spectrum of applications, such as on-board battery chargers, high-efficiency and high-density power converters, solar panel inverters, among many others. However, the lateral topology of HEMTs presents some pertinent limitations related to reliability and breakdown voltage scaling, which hinder the usability of these devices for high voltage applications requiring breakdown voltages above 700 V, for example in electric and hybrid electric vehicles (EVs and HEVs), photovoltaic (PV) inverters, wind turbines, traction systems for trains, to name a few.

Most of the limitations associated with GaN HEMTs arise from the lateral electron flow between the source and drain terminals, very close to the device surface. The density of electrons in the channel is sensitive to the presence of surface traps, that may degrade the electrical performance [156]–[158] of the transistors. This leads to issues like current collapse and dynamic degradation of the on resistance, which are more severe with increasing the BV rating of the device (see Sections 8.2 and 9). In addition, the lateral nature of the transport results in a very inhomogeneous distribution of the electric field in the device, peaking in specific regions (e.g. the edge of the gate, or of the field plate, on the drain side). This may enhance electron trapping at surface states, and may lead to premature breakdown of the semiconductor and of dielectrics. This ultimately degrades the forward and reverse performance of the device [158], [159], and limits its full voltage blocking potential. For traditional GaN HEMTs, the BV is dictated by the gate to drain spacing (provided this value is smaller than the drain-to-substrate BV) and thus larger breakdown voltages require larger device sizes, which also increases the device cost. Another major concern is that GaN HEMTs are in general normally-on devices: this is not desirable for power electronics applications from a safety perspective and for simplicity of the gate drivers, which are currently designed for normally-off devices. As discussed in Section 6.2, Several methods to achieve normally-OFF operation have been developed including cascode [160]–[162] configuration (based on GaN HEMT combined with a Si MOSFET), fluorine ion implantation [80], [94], [163] under

the gate region, recessing the barrier layer [83] in the gate region, by applying tri-gate structures [138], [164]–[167] to the gate region, among others. However, in many cases and even for commercial devices, the threshold voltage (V_{th}) that can be achieved is only around 1-2 V, which may not be ideal for fail-safe operation. Finally, GaN HEMTs do not present avalanche capability, which can prevent device failure under short term over-voltage conditions. Thus, for a GaN HEMT to qualify for a certain BV rating, the device has to be overdesigned to sustain a much higher BV, which increases the device size and cost.

Vertical GaN power devices are different from their lateral counterparts as the current flows vertically, i.e., parallel to the growth direction of the epitaxial GaN layers. The vast majority of the Si and SiC power devices available commercially are based on this design philosophy and are capable of delivering high ON-state currents (> 7000 A) and high BVs (> 8000 V) [168]. For GaN, the vertical topology offers distinct advantages over lateral power HEMTs. The BV can be increased by increasing the thickness of the voltage blocking layer, generally formed by an un-intentionally or low doped GaN layer (also referred to as the drift layer or i-GaN layer), independent of the size of the device. The R_{ON} in PiN diodes increases only slightly [169] with increasing the thickness of the drift layer as a result of extrinsic phenomena like conductivity modulation [170], [171]. Vertical devices are also not affected by surface traps as in GaN HEMTs, and the electric field peaks well inside the GaN layers, away from the surface, thus improving the device breakdown voltage and reliability. In addition, vertical MOSFETs can provide high positive V_{th} of 5-15 V, which is well suited for higher power applications like in automobiles. Another major advantage is the existence of avalanche breakdown [172]–[174] for GaN vertical power devices. This greatly improves the reliability, and eliminates the need to overdesign the device.

7.2 Choice of substrate:

The ideal solution for obtaining high quality GaN epitaxial layers is by homo-epitaxy i.e., GaN layers grown on bulk GaN substrates. These substrates are mainly produced by hydride vapor-phase epitaxy (HVPE), although several other methods like Na-flux or ammonothermal growth are currently being investigated [175]–[180]. The major advantages of growing GaN by homoepitaxy are their low dislocation density of 10^4 -10^6 /cm^2 and the inherently matched lattice and coefficient of thermal expansion (CTE) to the grown GaN layers. As a result, thick GaN layers

suitable for achieving high-voltage (~ 5000 V) [181], [182] vertical power devices can be easily grown on these substrates. The downside is that these substrates are very expensive, at about 50 $/cm^{2,} and mostly available in small 2-inch wafer diameters [183]; strategies for larger size substrates are currently under investigation [175], [184] []. This hinders the widespread commercialization of devices grown on bulk GaN. The bulk GaN market is also highly concentrated, as three companies based out of Japan hold about 85% stake in the bulk GaN market [185]. Currently, these expensive substrates are being used only for special applications, like laser diodes and high-brightness LEDs [185], for which low dislocation densities are essential. Hence, in order to take advantage of the material benefits offered by GaN materials for power device applications, further improvements in wafer size and reduction in cost are highly desirable. However, over the past decade, improvements in wafer size have been relatively slow, which is a critical aspect for reducing the production cost per device. A strategy to tackle this issue would be by hetero-epitaxy i.e., GaN layers grown on foreign substrates like Si, SiC and sapphire, which are cheaper than bulk GaN and are available up to 12-inch diameters [186], [187]. However, these substrates are both lattice and CTE mismatched to GaN, as shown in Table 6. This results in a high defect density in the GaN crystalline structure as a result of the stress built up during growth. Growth of thick layers of GaN (> 7µm) on 6-inch Si substrates also results in significant wafer bowing and cracking [183], [188], [189]. Thus, further improvements in the dislocation density and investigation of stress-relaxation buffer layers for the growth of thick GaN layers on these substrates are essential.

Parameter	GaN-on-Si	GaN-on-SiC	GaN-on-Sapphire	GaN-on-GaN
Defect density	~ 10^9 /cm^2	~ 5×10^8 /cm^2	~ 10^9 /cm^2	~ 10^4-10^6 /cm^2
Lattice mismatch %	17	3.5	16	0
CTE mismatch %	54	25	34	0

Table 6. Comparison of material properties of GaN grown on various substrates [190]

The majority of the reported GaN vertical power devices are based on bulk GaN substrates as a result of their low dislocation density, which provide a fair representation of the superior material properties of GaN as compared to Si. Even though these bulk GaN substrates have a defect density

higher than Si or SiC, these devices have been shown to pass reverse leakage tests, high temperature reverse bias (HTRB), high temperature operating life (HTOL), temperature humidity bias (THB), temperature cycling (TC) and inductive avalanche ruggedness stress tests [191], which is of paramount importance from the point of view of commercialization of these devices in the future. This section aims to summarize the research development on vertical GaN devices, providing an extensive review encompassing the fabrication and performance of various vertical devices reported till today. The development of vertical devices on sapphire and bulk GaN will be first presented followed by the recent development of GaN-on-Silicon vertical devices.

7.3 Vertical device architectures:

7.3.1 Development of vertical devices on sapphire and bulk GaN

7.3.1.1 PiN diodes:

P-i-N junctions are ubiquitous structures that compose many electronic devices. In wide-band-gap semiconductors however, the large turn-on voltage and high reverse recovery times of such diodes due to the large band gap hinders their applications in efficient power electronics. Even though Schottky diodes are preferable in power applications, due to their low turn-on voltage and reverse recovery time during switching transients, PN junctions are also an integral part of a number of modern vertical power devices, including IGBTs, junction barrier Schottky (JBS) diodes, merged p-i-n Schottky diodes, junction termination extensions (JTEs), etc. and thus merits a comprehensive study. Furthermore, the well-known and simple physics of p-n junctions is helpful in elucidating various material parameters, such as critical electric field (E_c), doping density, impact ionization coefficients, generation-recombination rates, mobility of electron and holes, temperature related effects, etc. [192] These properties are of utmost importance for the design and understanding of the power device.

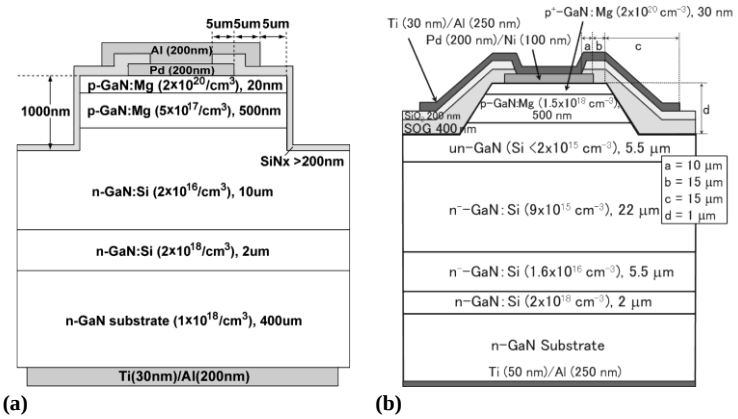
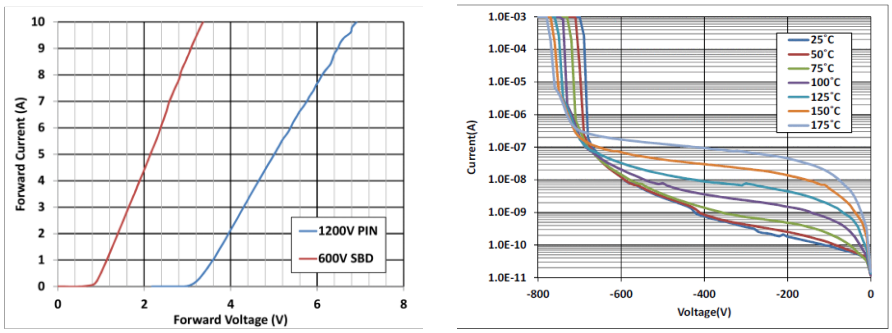


Figure 40 (a) Schematic cross sections of the GaN p-n junction diodes with SiNx passivation and the FP structure (https://ieeexplore.ieee.org/abstract/document/6042353) [193]. (b) Schematic cross sections of the GaN p-n junction diodes with the triple drift layers and the FP structure. (https://ieeexplore.ieee.org/document/7273835) [182].

The first report on GaN power p-i-n diodes on sapphire substrates date back to 2000 [194], [195] and the first GaN p-i-n diodes on bulk GaN substrates were reported in 2005 [196]. However, high-voltage p-i-n diodes with BV > 1 kV were reported only in 2011 [197]. Rapid developments in the growth and fabrication of p-i-n diodes ensued, mainly by startups like Avogy Inc. and researchers from institutions like Cornell University, Hosei University, Toyoda Gosei, etc [192], [198]–[201]. The schematic of a p-i-n diode with BV of 1100 V [193] as reported by Hosei university is shown in Figure 40 (a). A mesa termination with SiO_2 passivation and a field plate structure were employed to improve the BV from ~ 450 V to 1100 V along with a small $R_{on,sp}$ (given by R_{ON} × Active area of the device) of 0.4 mΩcm^2, thus achieving an excellent Baliga's figure of merit (BFOM = $\frac{BV^2}{R_{on,sp}}$) > 3.0 GW/cm^2. Subsequently, a low-damage field plate process involving the use of a bilayer spin-on-glass (SOG)/ sputtered SiO_2 as the field plate dielectric along with a drift layer thickness of 20 µm were developed to achieve the first demonstration of GaN p-i-n diodes with very high BV of over 3 kV [199]. The SOG protected the p-GaN anode contact area from damages related to the SiO_2 sputtering process. A low $R_{on,sp}$ of 0.9 mΩcm^2 along with this high BV resulted in record BFOM of 10 GW/cm^2 in 2013. A p-i-n diode [182] with triple drift layer to improve the distribution of the electric field was proposed in 2015 (Figure 40 (b)). The drift layer forming the p-n junction was doped to low 10^{15} /cm^3 to create a near-flat electric field profile and thus reduce the electric field. Subsequent drift layers were moderately doped to reduce

the $R_{on,sp}$ to 1.7 mΩcm^2, while still presenting a high BV of 4.7 kV. In 2018, a novel p-i-n diode with a guard-ring termination [181] was presented which resulted in lower leakage current and an improvement in BV by 200 V to obtain a high blocking voltage of 5 kV.



(a) **(b)**

Figure 41 (a) Forward I-V characteristics of SBDs and PiN diodes (https://ieeexplore.ieee.org/document/6694455). (b) Reverse I-V characteristics of the PiN diodes as a function of temperature with BV demonstrating positive temperature coefficient indicative of avalanche breakdown. (https://ieeexplore.ieee.org/document/6694455). [191]

Avogy Inc. first reported on the avalanche capability in p-i-n diodes with BV of 2.6 kV and 3.7 kV [192], [198] (Figure 41). The device structure is as shown in Figure 42 (a). An ion-implantation-based proprietary edge termination was employed for better redistribution of electric field peaks to realize breakdown voltages approaching 85% of that in theoretical parallel-plane junction breakdown, and also to achieve avalanche capability. The role of substrate orientation on the reverse leakage current and reliability of the devices revealed that a slight miscut angle of several tenths of a degree is very beneficial. This results in the elimination of hillocks on the surface of the as-grown GaN layers and reveals a surface with a smooth morphology which is essential for achieving reliable devices with low reverse leakage currents [192] (Figure 42 (b)). These devices were qualified with HTRB, THB, HTOL and TCT tests, indicating that even with a defect density of 10^4-10^6 /cm^2, GaN vertical devices could be adopted for fast commercialization [191]. Avogy p-i-n diodes also fared extremely well against Si fast diodes when used in power converter topologies, like the hard-switched boost circuit with little or no ringing as well as no reverse recovery loss as compared to the Si fast diodes [202], [203]. They also demonstrated large area 16 mm^2 PiN diodes with current capability of 400 A in pulsed operation [204]. These diodes provided 100 A at 4.5 V forward bias in DC operation together with an excellent BV of 700 V.

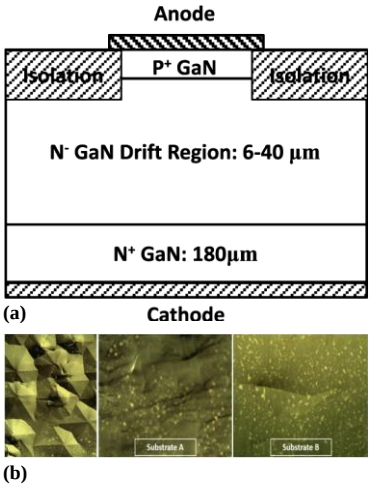


Figure 42 (a) Schematic of a vertical GaN p-n diode with ion-implanted edge termination (https://ieeexplore.ieee.org/document/6919319) [192]. (b) Nomarski image of surface morphology observed on devices grown on GaN substrates. The image on the left demonstrates hillocks formed on the GaN surface in growth on low miscut angle substrates. Devices fabricated using substrate B will consistently have lower reverse leakage currents compared to those on substrate A. Reprinted from Microelectronics Reliability, Volume 55, Isik C. Kizilyalli et al., "Reliability studies of vertical GaN devices based on bulk GaN substrates", Pages No. 1654-1661, Copyright 2015, with permission from Elsevier. (https://www.sciencedirect.com/science/article/pii/S0026271415301013) [191].

Cornell University demonstrated the growth of high-quality GaN layers by metal organic chemical vapor deposition (MOCVD) resulting in a Shockley-Read-Hall (SRH) lifetime of 12 ns. As a consequence, their p-i-n diodes exhibited ultra-low $R_{on,sp}$ of 0.12 $m\Omega cm^2$ coupled with a high BV of 1.4 kV, thus resulting in a BFOM of 16.5 GW/cm^2 [205]. GaN p-i-n diodes incorporating a bevel termination and a long field plate were also presented in 2015 with an improvement in BV by more than 3-fold to ~ 4 kV[206], as compared to a p-i-n diode with no termination. In order to circumvent the issues faced during p-GaN growth by MOCVD, like the Mg memory effect and the hydrogen passivation of Mg dopants in p-GaN, high BV GaN p-i-n diodes with molecular beam epitaxy (MBE) grown p-GaN were also reported [207], [208]. This study also provides an alternative strategy for p-GaN regrowth by MOCVD, which could result in impurity incorporation at the growth interface and issues arising from non-planar growth, like high leakage currents [200], [201], [209].

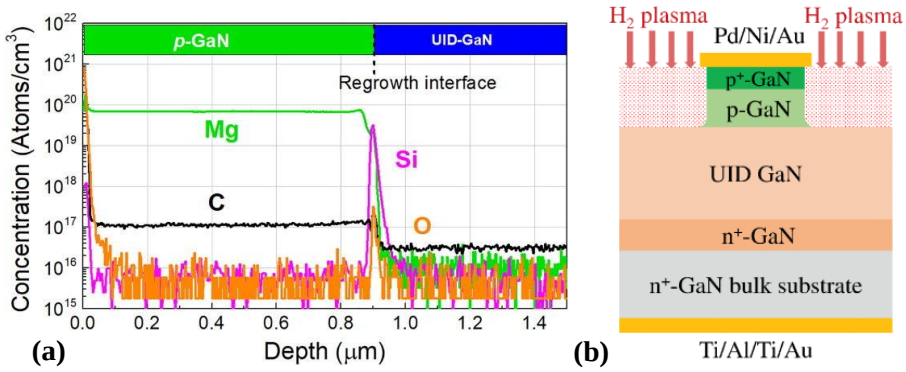
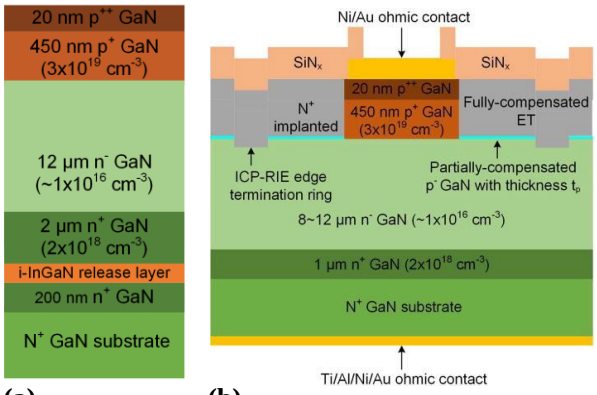


Figure 43(a) SIMS profile of the regrown p-n junction showing high levels of Si and O atoms at the regrowth interface. Reprinted from K. Fu et al., "Investigation of GaN-on-GaN vertical p-n diode with regrown p-GaN by metalorganic chemical vapor deposition" , Applied Physics Letters 113, 233502 (2018), https://doi.org/10.1063/1.5052479, with the permission of AIP Publishing. (https://aip.scitation.org/doi/full/10.1063/1.5052479) [200]. (b) Schematic cross-section of GaN-on-GaN p-n diodes with hydrogen plasma based edge termination (https://ieeexplore.ieee.org/document/8360159). [210]

Arizona State University reported on the beneficial effects of growing a thick buffer layer of about 1 µm on the bulk GaN substrate prior to subsequent growth [211]. They also investigated in details the regrowth of p-GaN layers on etched GaN surfaces [200], [212]. Regrowth of p-GaN is an important topic, especially since ion implantation schemes for the realization of JTE (junction termination extension) structures similar to Si and SiC carbide vertical power devices are very complicated in GaN and still not available. The study revealed that the regrowth process could result in a slight increase in the edge dislocations and a high concentration of Si and O impurity atoms at the growth interface (Figure 43(a)). In a subsequent work [212], the reason for this high impurity atom concentration was shown to be from the defective etching process, and a low power etching coupled with UV-ozone/acid treatment of the etched surface prior to the p-GaN regrowth was presented as a remedy to this issue. A novel edge termination scheme was also introduced by passivating the p-GaN around the anode region by hydrogen plasma [210], to obtain significant gains in the BV (Figure 43 (b)).



(a) **(b)**

Figure 44(a) Schematic of the heterostructure used for the epitaxial liftoff devices clearly showing the i-InGaN release layer (https://ieeexplore.ieee.org/document/8457225). [213] (b) Schematic cross-section of GaN-on-GaN p-n diodes with nitrogen implanted edge termination Reprinted from J. Wang et al.,"High voltage, high current GaN-on-GaN p-n diodes with partially compensated edge termination", Applied Physics Letters 113, 023502 (2018) https://doi.org/10.1063/1.5035267, with the permission of AIP Publishing. (https://aip.scitation.org/doi/full/10.1063/1.5035267). [214]

Besides these developments, several other groups demonstrated important advances in the growth, termination and improvements to the on-state electrical performance. University of Notre Dame and Sandia National Laboratory demonstrated the use of nitrogen implantation to form edge termination for p-i-n diodes [214], [215] (Figure 44(b)). Devices with ultra-low $R_{on,sp}$ of 0.15 $m\Omega cm^2$ and BV of 1.68 kV corresponding to Baliga's figure of merit of 18.8 GW/cm^2 were obtained. Another type of termination is a bevel edge termination, which was studied extensively for GaN p-i-n diodes by researchers from Kyoto University [174]. The study set forth important design instructions, particularly the angle of the bevel, the thickness and the doping of the GaN layers, etc.

Bulk GaN substrates are typically around 350-400 µm thick and serve the purpose of providing a lattice and CTE matched template for epitaxial growth of GaN layers. However, after the growth of the low defective GaN layers, the bulk GaN substrate could be effectively removed and reused. This concept was demonstrated by introducing a thin i-InGaN layer between the bulk GaN substrate and a p-i-n heterostructure [213] (Figure 44(a)). This i-InGaN layer can be photo-electrochemically etched resulting in an epitaxial liftoff from the bulk GaN substrate. The epitaxial

layers can then be bonded to a high thermal conductivity material and processed further. The bulk GaN substrate can then be reused many times for growing new epitaxial layers by a similar process. The p-i-n diodes fabricated by using this method demonstrated an excellent $R_{on,sp}$ of 0.2-0.5 $m\Omega cm^2$ and a BV of 1300 V similar to a control device fabricated without epitaxial lift off, thus confirming no degradation in the performance as a result of this special fabrication process.

These results revealed the excellent progress made for GaN PiN diodes providing important insights into the material properties like critical electric field, reliability, avalanche capability, etc. Si and SiC devices normally employ junction termination extension structures formed by selective p/n- type doping by ion implantation to achieve reliable devices. Due to the difficulties involved in achieving selective doping in GaN, several other methods based on N_2/H_2 plasma treatment, field plate deposition and ion implantation schemes to form resistive regions around the anode were employed to obtain high BV devices.

7.3.1.2 Schottky Barrier Diodes (SBDs):

Unlike PiN diodes, SBDs are unipolar devices, which find applications in power converters by virtue of their low turn-on voltage as well as absence of reverse recovery charge. Due to the absence of a p-type layer, and thus conductivity modulation, SBDs normally have a higher R_{ON} compared to PiN diodes [216]. The reverse leakage current is also higher as the reverse voltage is held by the depletion at the metal-semiconductor Schottky barrier. Vertical GaN SBDs on sapphire substrates were first reported in 2000 with a BV as high as 550 V [217], [218]. In 2001, vertical GaN SBDs on bulk GaN substrate were demonstrated by incorporating a Mg^+-ion implanted p-guard rings at the edge of the Schottky contacts. The device presented a $R_{on,sp}$ of 3.01 $m\Omega cm^2$ and a BV of 700 V. The first high voltage SBDs on bulk GaN substrates, presenting BV > 1 kV were only demonstrated in 2010 by Sumitomo electric industries [219]. The growth was optimized leading to an excellent electron mobility of 930 cm^2/Vs in the undoped GaN layer resulting in an ultra-low $R_{on,sp}$ of 0.71 $m\Omega cm^2$. A field plate termination was employed to obtain an excellent BV of 1100 V using just a 5 µm-thick undoped GaN as the voltage blocking layer, leading to a BFOM of 1.7 GW/cm^2 (Figure 45(a)). Large-area SBDs with 1.1 × 1.1 mm^2 Schottky electrode area provided a forward current of 6 A at 1.46 V and a $R_{on,sp}$ of 0.84 $m\Omega cm^2$ while still exhibiting a high BV of 600 V. This revealed the potential for scaling up these devices for commercial applications. The switching characteristics of these large area diodes compared against Si fast

recovery diodes (FRDs) and SiC SBDs, which revealed the smallest reverse recovery time, reverse recovery charge and losses for GaN SBDs [220] (Figure 45(b)). Their study also confirmed stable forward and reverse aging characteristics for 1000 hours. Further advances in the material quality of the bulk GaN substrates and optimizations in the MOCVD growth of GaN epitaxial layers led to improvement in the electrical characteristics of SBDs, with forward currents of 50 A at 2.05 V while sustaining a high enough BV of 790 V, as reported by Toyoda Gosei [221]. The 3 × 3 mm^2 SBDs included a mesa termination with a field plate to improve the BV, while an excellent electron mobility of 1200 cm^2/Vs for the undoped GaN layer provided a low differential ON-resistance of 25-29 mΩ.

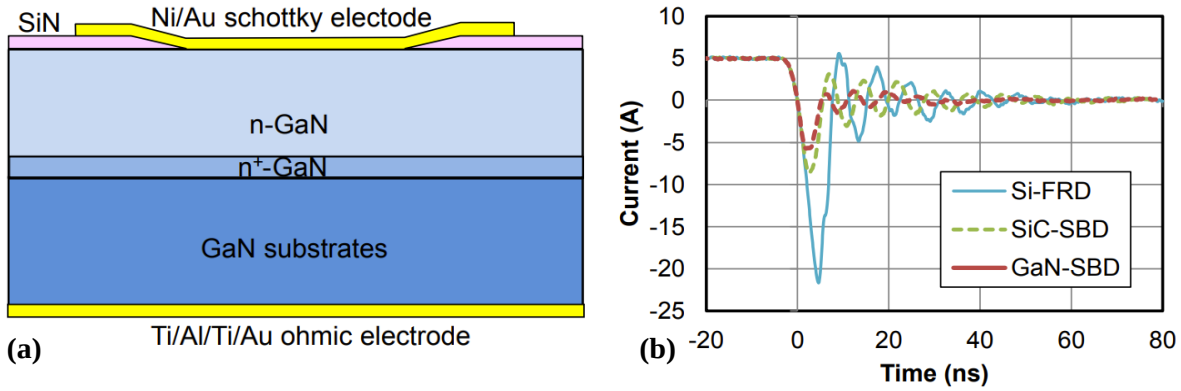


Figure 45: (a) Schematic cross section of the vertical GaN SBD (https://ieeexplore.ieee.org/document/6856038). (b) Reverse recovery characteristics of GaN SBD, SiC SBD, and Si FRD at I_F of 5A, a reverse voltage of 380V, and dI/dt=3.4kA/µsec. (https://ieeexplore.ieee.org/document/6856038). [220]

From 2015-2020, significant progress was made in improving the quality of the epitaxial GaN layers and termination methods for SBDs. Cao et al., from HRL laboratories demonstrated an SBD with graded AlGaN cap layer on top of the voltage blocking drift layer (i-GaN) [222] as shown in Figure 46.

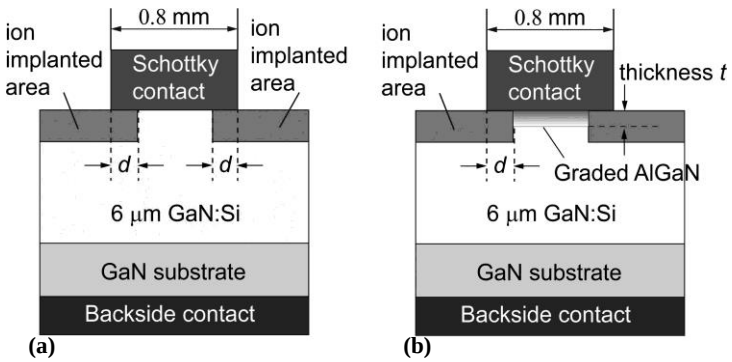


Figure 46 (a) Schematic cross section of the control vertical GaN SBD (https://aip.scitation.org/doi/full/10.1063/1.4943946) and (b) the SBD with the graded AlGaN cap layer (https://aip.scitation.org/doi/full/10.1063/1.4943946) [222]

This reduced the reverse leakage current by three orders of magnitude while the polarization field in the graded AlGaN effectively shortened the depletion width leading to the formation of a tunneling current at relatively lower bias, thus providing a low turn-on voltage to 0.67 V. These AlGaN capped SBDs with a Schottky contact area of 0.8×0.8 mm^2 improved the BV by more than 2-fold, to 700 V, as compared to a control SBD with no AlGaN cap layer. The effect of C incorporation during the MOCVD growth was investigated on both the forward as well as the reverse characteristics of SBDs [223]. By varying the growth pressure and V/III ratio, different C concentrations from $\leq 3 \times 10^{15}$ to 3×10^{19} /cm^3 could be obtained. Their study revealed that lower C incorporation is better for both forward and reverse performance, resulting in SBDs with small turn-on voltage of 0.77 V and high BV of 800 V for a large Schottky contact area (0.8×0.8 mm^2) devices. Prof. Amano's group at Nagoya University also studied the effect of C impurity accumulation on the leakage current of GaN SBDs [224]. In their study, initial failure of SBDs at low voltages were ascribed to leakage current path through polygonal pits created by C impurity accumulation during the growth process. Their group also perfected the method of achieving low impurity levels in m-plane GaN, approaching c-plane values by using a quartz-free flow channel [225]. In 2019, they reported on the effect of drift later thickness on BV, along with the demonstration of vertical GaN SBD with the highest reported BV of 2.4 kV for a drift layer thickness of 30 μm [226]. A reduction in the effective donor concentration with increasing the thickness of the drift layer was observed by SIMS, and is believed to have a positive effect on achieving such a high BV. In a recent publication, their group presented their results on SBDs with

a drift layer compensated for the un-intentional n-type doping by introducing Mg dopants during the growth [227]. The resulting SBDs provided more than 3x-higher BV as compared to a non-compensated SBD, but the on-state current and $R_{on,sp}$ suffered as a result of the high resistivity of the drift layer. Arizona State University investigated ways to balance the interplay between $R_{on,sp}$ and BV with the introduction of double drift layers (DDL) for SBDs [228]. Basically, the SBDs consisted of an unintentionally-doped (UID) drift layer on the top and a slightly doped drift layer at the bottom. The UID drift layer at the top could suppress the peak electric field at the Schottky metal – UID interface and thus improve the BV.

Several implantation-based termination methods were demonstrated in the recent years. Han et al. demonstrated a planar nitridation based-termination, by subjecting the area around the Schottky contact to a N_2 plasma from a plasma-enhanced chemical vapor deposition system (PECVD) [229]. From ultraviolet photoelectron spectroscopy, it was inferred that the Fermi level at the GaN surface which underwent the N_2 plasma treatment, went down by 0.68 eV possibly by the passivation of the Ga dangling bonds and thus, an enlarged energy barrier height and/or effective barrier thickness is presented at the junction edge. This suppressed the thermionic field emission (TFE)/ tunneling at this region, and the leakage current reduced as a result. The SBDs with this termination scheme presented 4 orders of magnitude lower leakage current as compared to a control SBD with no termination and improved the BV from 335 V to 995 V. These devices also provided excellent switching behavior with current-collapse free operation and zero reverse recovery characteristics [230]. Han et al., also demonstrated fluorine implanted edge termination schemes for GaN SBDs based on the principle that the implanted fluorine ions act as fixed negative ions in GaN [231] (Figure 47(a)). This results in spreading of the electric field and prevents the localized peaking at the Schottky contact edge, thus improving the BV as shown in Figure 47(b). The implantation was done at energy levels of 30, 60 and 100 keV followed by post implantation annealing at 450 °C in N_2 ambient for 10 mins. The BV was boosted from 260 V for the unterminated SBD to 800 V. Further improvement in the BV to 1020 V was achieved by capping the drift layer with a thin 5 nm layer of graded AlGaN, similar to that reported by Cao et al. Wang et al., demonstrated an identical edge termination scheme with boron implantation [232]. Similar to the fluorine implanted device described before, the boron implanted SBD provided 5 orders of magnitude improvement in the leakage current and improved the BV from 189 V for the unterminated SBD to 585 V.

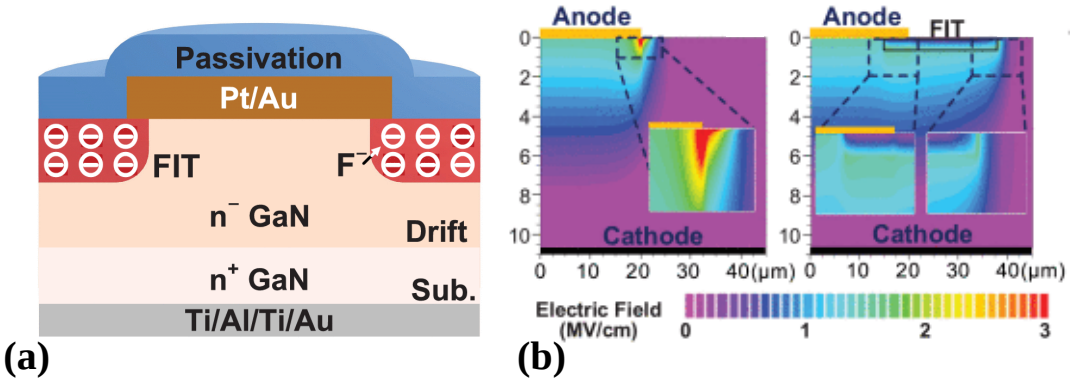


Figure 47 (a) Schematic cross section of the control vertical GaN SBD with fluorine implanted termination (https://ieeexplore.ieee.org/abstract/document/8709951) and (b) show simulated electric field distribution in the unterminated-SBD and FIT-SBD at −600 V, respectively (https://ieeexplore.ieee.org/abstract/document/8709951). [231]

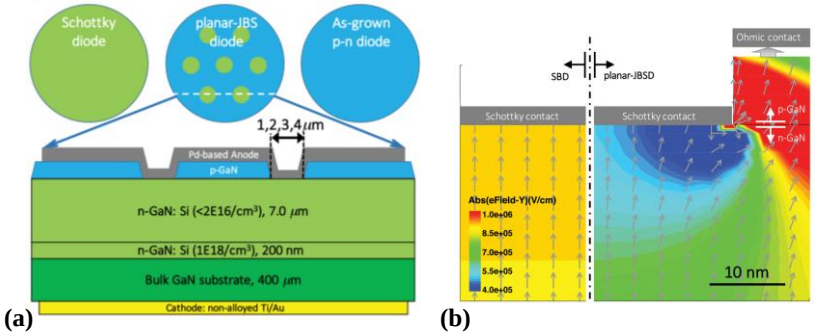


Figure 48(a) Schematic device top view and cross section of the fabricated trench JBS diode (https://ieeexplore.ieee.org/abstract/document/7859485) and (b) show simulated electric field distribution at -200 V clearly showing the reduction in electric field due to RESURF action from adjacent p-GaN later (https://ieeexplore.ieee.org/abstract/document/7859485). [233]

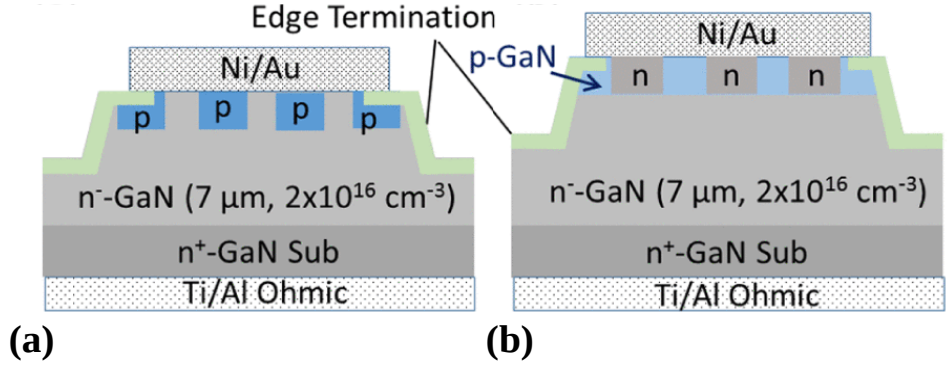


Figure 49: Schematic cross section of a JBS diode by (a) Mg ion implantation in n-GaN https://ieeexplore.ieee.org/document/7959570) and (b) Si ion implantation in p-GaN (https://ieeexplore.ieee.org/document/7959570) [234].

Junction Barrier Schottky (JBS) diodes are another type of device that combines low turn-on voltage from the Schottky contacts and low leakage current provided by p-i-n diodes. This is achieved by having alternate undoped and p-type regions below the anode contact which can be easily formed for Si and SiC by ion implantation methods. Since ion implantation of dopants to GaN is very difficult, other methods to achieve JBS structures were pursued. Cornell University created a trench JBS diode by selectively etching away portions of p-GaN layer form a p-i-n diode followed by Schottky contact formation [233], as presented in Figure 48(a). The reduced surface field (RESURF) effect at the Schottky surface as a result of the adjoining p-GaN layers were elaborately studied using TCAD (Figure 48(b)). Hayashida et. al. from Mitsubishi Electric Corporation demonstrated a merged p-i-n Schottky diode [235] based on a trench JBS diode achieving a BV of 2 kV along with surge current capability. However, the leakage current was as high as 10^{-3} A/cm^2 at ~ 750 V and reached 10 A/cm^2 at 2000 V which needs to be further improved. Ion implantation methods have also been tried to achieve JBS structures in GaN. First reported in 2016 by Koehler et. al [236], the p-doped regions were formed by Mg ion implantation followed by symmetrical multi-cycle rapid thermal annealing (MRTA) for activation. The JBS action was confirmed from reverse bias measurements, which presented much improved leakage current and BV as compared to a normal SBD. Shortly after, Zhang et al. demonstrated vertical GaN JBS diodes [234] by (a) Mg implantation into n-GaN to form p-wells and (b) Si implantation into p-GaN to form n-wells (Figure 49). The implantation and the activation scheme was similar to that used by Koehler et al. $R_{on,sp}$ values of 1.5-2.5 mΩcm^2 and 7-9 mΩcm^2 were observed for the Mg implanted and Si implanted JBS diodes. Both sets of devices provided 100x-reduction in reverse leakage current at high reverse bias and presented a BV of 500-600 V.

Trench Metal Barrier Schottky (TMBS) diodes first demonstrated in GaN by Zhang et al. in 2016 [237] represents a device topology which can provide a better control of the reverse leakage current in an SBD. A TMBS diode consists of a trench metal insulator semiconductor (MIS) structure as shown in Figure 50(a). The MIS structure does not contribute to the forward conduction phase but in the reverse bias condition, the two adjacent MIS structures deplete the semiconductor region

between them, thus reducing the leakage current and improving the BV. However, since the Schottky contact is formed only in a portion of the anode, the $R_{on,sp}$ is higher than in a conventional SBD with Schottky contact in the entire anode area. The leakage current can be controlled by optimizing the trench depth and the TMBS pillar width (Figure 50(b)). But too deep a trench will also result in premature breakdown of the SiN_x dielectric layer due to electric field peaking at the trench bottom corner. To address this issue, argon-implanted field rings were employed to protect the base of the TMBS anode. The TMBS diode improved the leakage current by 10^4-fold and improved the BV from 400 to 700 V.

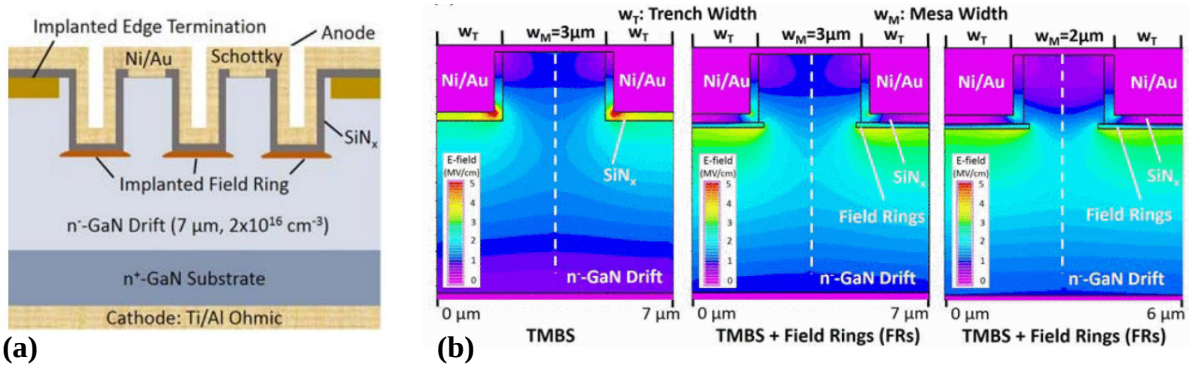


Figure 50 (a) Schematic cross section of a TMBS diode (https://ieeexplore.ieee.org/abstract/document/7838386) and (b) TCAD simulation of electric field at a reverse bias of -1000 V displaying (i) how with the implementation of a field ring at the base of the trench, the electric field peak can be reduced and (ii) how the leakage current can be reduced by making the TMBS pillar narrow from 3 µm to 2µm (https://ieeexplore.ieee.org/abstract/document/7838386). [237]

Thus, high performance vertical SBDs with low $R_{on,sp}$ and high BV have been demonstrated in bulk GaN and sapphire substrates by improving the material quality of the GaN epitaxial layers as well as by employing various leakage current mitigation and edge termination schemes. Current collapse free operation with zero reverse recovery characteristics could be achieved, thus making GaN SBDs an ideal candidate for low loss rectification purposes.

7.3.1.3 GaN Current aperture vertical electron transistors (CAVETs)

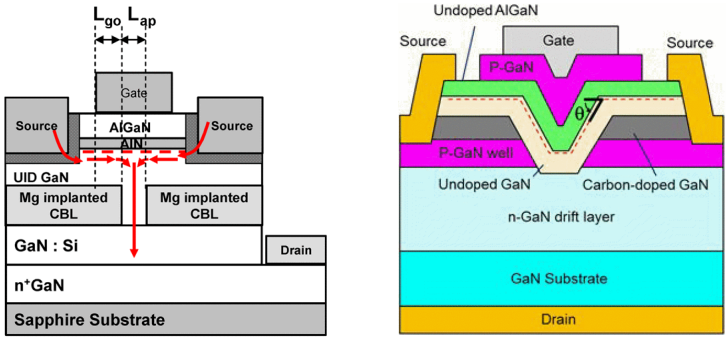


Figure 51 (a) Schematic cross section of a GaN CAVET (https://ieeexplore.ieee.org/document/4526759) [238]. (b) Schematic cross-section of an improved version the GaN CAVET with normally-off behavior and 1.7 kV BV (https://ieeexplore.ieee.org/document/7838385) [239].

The first GaN-based CAVET structure for high voltage applications were proposed by Yaacov et. al in 2004 [240]. The CAVET structure is similar to double-diffused MOS [241] (DDMOS) structure and comprises of an AlGaN/GaN heterostructure at the top, current blocking layers (CBLs) and a n-type doped GaN layer at the bottom as shown in Figure 51(a). The source terminals form ohmic contact to the 2DEG and the gate forms Schottky contact to AlGaN. The CBL implemented using Mg-ion implantation restricts the flow of current to a small aperture region which sits just below the gate. By applying a gate bias, the 2DEG below the gate can be switched on/off, thus resulting in a transistor behavior. The main foreseen advantage is that under voltage blocking condition, the high field region would sit under the gate in the bulk of the device, unlike a lateral HEMT, and thus may support large BV as surface related breakdown was eliminated. However, CAVETs are generally normally-ON devices, as they rely on an AlGaN/GaN channel which is modulated by the gate. Chowdhury et al., in 2008 [238] demonstrated the first E-mode CAVET with a threshold voltage of 0.6 V achieved by CF_4 treatment in the gate region prior to gate metallization. Since the AlGaN/GaN layers are regrown by MOCVD after the formation of CBL, the device threshold voltage varied considerably due to Mg diffusion to the regrown layers. Chowdhury et.al, in 2012 [242] demonstrated a GaN CAVET with MBE regrown AlGaN/GaN layers which provided a low $R_{on,sp}$ of 2.2 $m\Omega cm^2$ and a BV of 200-260 V at a V_{GS} of -15 V. The $R_{on,sp}$ was reduced to 0.4 $m\Omega cm^2$ [209] by using a buried conductive p-GaN layer as the CBL. Avogy developed on this idea and in 2014 demonstrated a modified version [243] of these CAVET

structures with a p-GaN gate layer between the gate electrode and the AlGaN barrier for normally-off operation. Their device provided a forward current as high as 2.3 A and a threshold voltage of 0.5 V. A high BV of 1.5 kV was observed at a V_{GS} of -5 V aided by implanted edge termination structures. Panasonic corporation [239] demonstrated a similar device by placing a portion of the channel on the sidewall of an etched trench (forming the gate) and a p-GaN gate (Figure 51 (b)). They could achieve a low $R_{on,sp}$ of 1 mΩcm^2 and an excellent BV of 1.7 kV (Figure 52). Ji et al. [244] demonstrated a GaN CAVET with a similar gate trench structure but without the p-GaN gate and achieved 20 V threshold voltage, and a BV of 225 V. A higher BV of 880 V was achieved by Ji et al. [245] in a subsequent report by improving the gate trench etching quality and by using a gate dielectric, which reduced the gate to drain leakage. However, as a result of using a MIS structure for the gate, the V_{GS} shifted to -21 V from 20 V for the previous report.

Some aspects associated with the GaN CAVET need to be addressed to make this transistor viable for commercial use. The main issue stems from the regrowth process, which introduces high source to drain and gate to drain leakage currents in the majority of the reported devices. The on-state performance is also very sensitive to the doping and dimension of the aperture region formed between the adjacent CBLs, which is difficult to control due to the relatively complicated fabrication process.

Vertical trench gate MOSFETs:

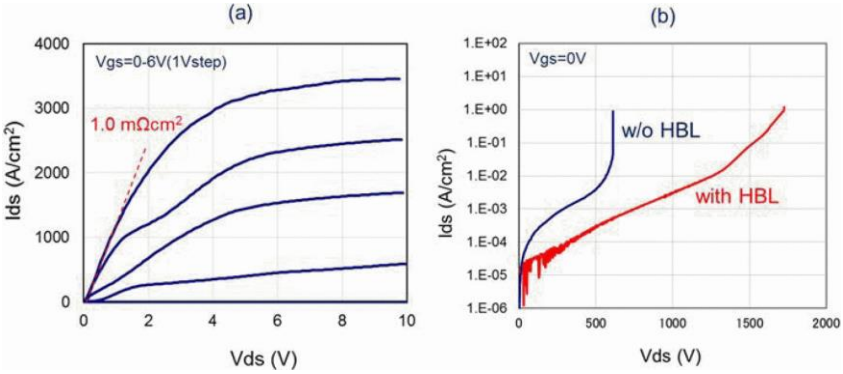


Figure 52 (a) DC output characteristics of the GaN transistor mentioned in https://ieeexplore.ieee.org/document/7838385 (b) OFF-state comparison with and without the carbon doped GaN layer (HBL) (https://ieeexplore.ieee.org/document/7838385). [239]

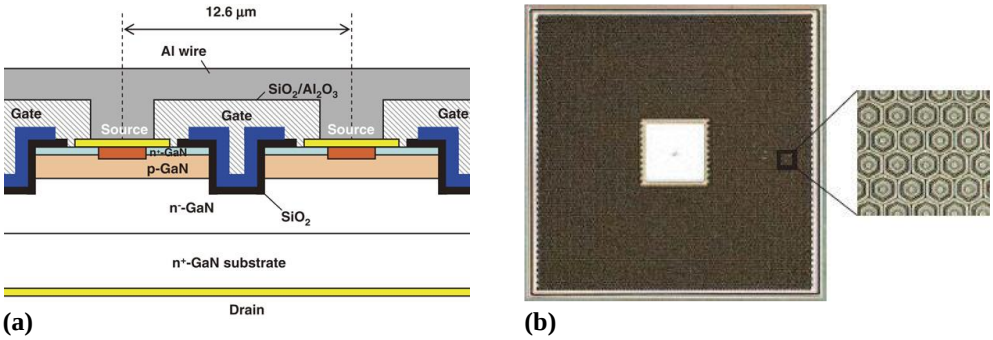


Figure 53(a) Schematic cross section of a GaN trench MOSFET (https://iopscience.iop.org/article/10.7567/APEX.8.054101/meta) [246]. (b) Chip micrograph of a 1.8 mm^2 large area multi-cell trench MOSFET. (https://ieeexplore.ieee.org/abstract/document/7520877) [247].

GaN trench MOSFETs were first reported by ROHM Co. Ltd. in 2007 [248]. These MOSFETs were fabricated on GaN layers grown by MOCVD on sapphire substrates. Two different gate dielectrics were investigated: electron-cyclotron-resonance (ECR) deposited SiO_2/Si_xN_y and PECVD SiO_2. A reduction in threshold voltage from 25.5 V to 5.1 V was observed by using the ECR deposited dielectric pair. This work also reported on a high channel mobility of 133 cm^2/Vs. In 2008, the same group demonstrated the first fully-vertical MOSFET [249] on bulk GaN substrates with similar performance figures as the previous report. Kodama et al. from Toyota Central R&D Labs [250] devised a method of achieving a smooth m-plane trench sidewall by dry etching followed by tetra methyl ammonium hydroxide (TMAH) wet etching. TMAH etches m-plane and c-plane of GaN at a much slower rate than the other facets. Hence sufficient treatment of the dry etched trench sidewall in heated TMAH results in a smooth surface, which is predominantly m-plane. This is very beneficial for achieving smooth vertical sidewalls, which could improve the channel mobility of the MOSFETs. Improvements in BV and $R_{on,sp}$ of GaN trench MOSFET were reported by Toyoda Gosei corporation in 2014 [251] (Figure 53 (a)). They demonstrated a GaN trench MOSFET with a field plate termination achieving a BV of over 1.6 kV and $R_{on,sp}$ of 12.1 $m\Omega cm^2$. In 2015 [246], they reported a similar device with $R_{on,sp}$ improved to 1.8 $m\Omega cm^2$, along with a high BV of 1.2 kV. This was achieved by tuning the doping and thickness of the p-GaN channel region and the i-GaN layer. The Mg doping of the p-GaN channel

layer was reduced, which resulted in lower scattering of inversion channel electrons by the dopant atoms, and they also slightly increased the doping of the i-GaN layer. Large area trench MOSFETs [247] with on-state current over 10 A while still maintaining a high BV of over 1.2 kV was also reported by the same group in 2016, which indicates that dislocation densities from bulk GaN substrates do not necessarily become a bottleneck for obtaining both high BV and high on-state current with large area devices (Figure 53(b)). A hexagonal cell array was employed for achieving a high gate width per unit cell area, leading to an increase in a current density and, thus, a reduction in the $R_{on,sp}$. Very recently [252], their group also demonstrated a vertical trench MOSFET with a current distribution layer (CDL) below the p-GaN as shown in Figure 54 (a). The CDL consists of a thin slightly n-type doped ($2 \times 10^{16}/cm^3$) layer which can better distribute the current from the base of the gate trench. This resulted in 1.17x-higher forward current density and an absolute value of current of 100 A was achieved for large area MOSFETs using the CDL (Figure 54 (b)). HRL Laboratories developed a method to avoid plasma etch damage to the p-GaN body contact region by selective area regrowth of n-GaN on top of the p-GaN. They demonstrated a 0.5 mm^2 large area trench MOSFET with an $R_{on,sp}$ of 8.5 $m\Omega cm^2$, threshold voltage of 4.8 V and a BV of 600 V. A detailed analysis of the dependence of main device parameters on gate dielectric thickness, body layer doping level and cleaning process was presented recently in [253].

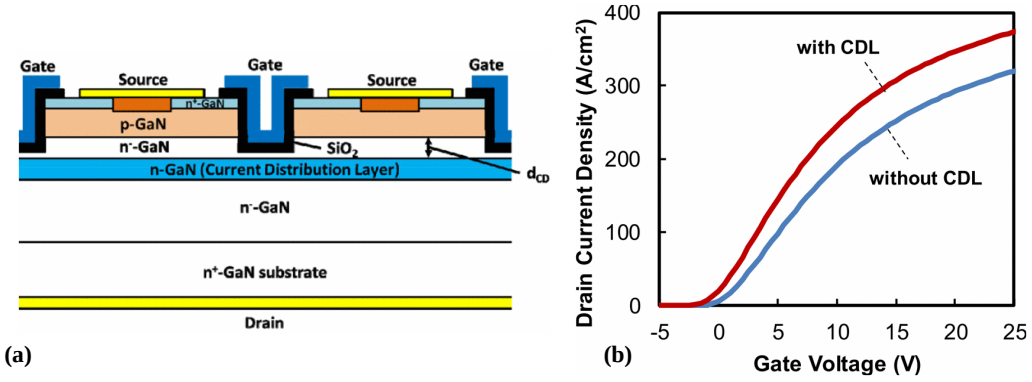


Figure 54 (a) Schematic cross section of a GaN trench MOSFET with CDL (https://ieeexplore.ieee.org/abstract/document/8757621) [252] (b)Transfer characteristics measured at VDS of 0.5 V for the MOSFET with and without the CDL (https://ieeexplore.ieee.org/abstract/document/8757621).
(https://ieeexplore.ieee.org/abstract/document/7520877) [247], [252].

*In-situ oxide GaN interlayer-based vertical trench MOSFET (OGFET)***:**

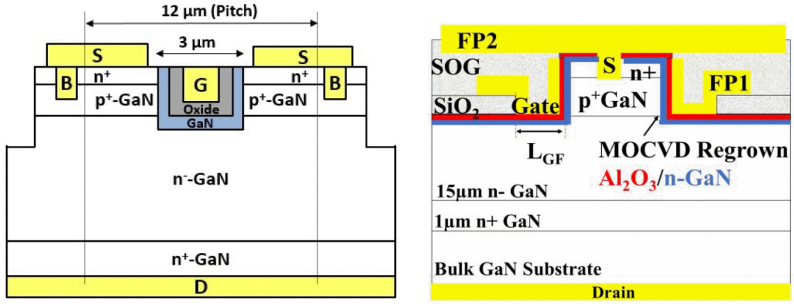


Figure 55 (a) OG-FET cross-sectional schematic (https://ieeexplore.ieee.org/abstract/document/7811227) [254]. (b) Schematic cross section of the GaN OG-FET with a double field-plate structure (https://ieeexplore.ieee.org/abstract/document/8268359) [255].

In a traditional vertical trench gate MOSFET with a n-p-i-n heterostructure, the channel region is formed by the n-p-i sidewall of the trench gate structure; on the application of a positive gate bias above the threshold voltage, an inversion sheet charge of electrons is formed in the p-GaN layer adjacent to the gate dielectric. Since the channel is formed by dry etching, the field effect mobility of the inversion channel electrons is degraded by the defects in the sidewall formed during the etching process. In order to alleviate this issue, Prof. Mishra's group at UCSB devised a technique [256] whereby a thin undoped GaN layer is regrown in the gate trench region by MOCVD, followed by in-situ Al_2O_3 dielectric deposition as shown in Figure 55(a). The initial reports on these devices presented 60% reduction in $R_{on,sp}$ as compared to traditional trench gate MOSFETs. A normally-off operation with a threshold voltage of 2 V was also achieved along with a BV of 195 V. Subsequent devices [254] on bulk GaN substrates provided a higher BV of 990 V aided by a low damage gate trench etching process. Ji et al. reported large-area (0.2 mm^2) OGFETs with an output current close to 0.5 A and a BV of 320 V. Further optimizations on the growth, design and fabrication of these devices resulted in OGFETs presenting a record channel mobility of 185 cm^2/Vs and a low $R_{on,sp}$ of 2.2 $m\Omega cm^2$ [255]. The adoption of a novel double field plate design helped achieving a high BV of 1.4 kV for a single device and 0.9 kV for a large-area (0.2 mm^2)

device (Figure 55(b)). Variations of the OG-FET have been reported by other groups as well. Li et. al. reported [257], [258] on an trench MOSFET similar to the OGFET but with an MBE regrown channel rather than by MOCVD. The main aim was to improve on the issue of re-passivation of p-GaN during regrowth of the interlayer by MOCVD. They could achieve a record high BV of 600 V among GaN transistors with a MBE regrown channel along with reduced thermal budget.

*GaN vertical fin power transistors***:**

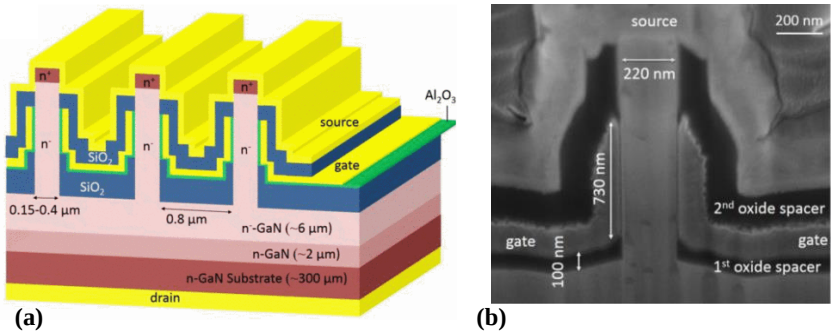


Figure 56 (a) Schematic of a vertical fin power transistor (https://ieeexplore.ieee.org/abstract/document/8268357). (b) cross sectional SEM image of the fin area with ~ 220 nm channel width. (https://ieeexplore.ieee.org/abstract/document/8268357). [259]

In recent years, vertical fin power FETs [260] have been demonstrated, with sub-micron fins on bulk GaN substrates. The advantage over classical trench MOSFETs is that they do not require a p-GaN layer to provide normally-off operation and blocking under off-state. The gate region of these devices consists of dielectric/gate metal on the fin sidewalls, which deplete the charge carriers in the fin due to the work function difference between the gate metal and the GaN, providing a normally-off operation (Figure 58). [261]

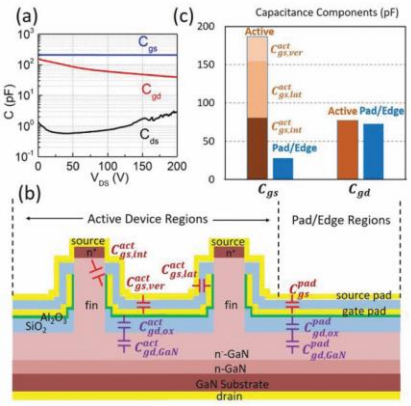


Figure 57 (a) Measured device junction capacitances C_{ds}, C_{gs} and C_{gd} .(b) Schematic of the various Cgs and Cgd components of the FinFET (c) Capacitance component break-out of the measured C_{gs} and C_{gd}. https://ieeexplore.ieee.org/document/8528328 [262]

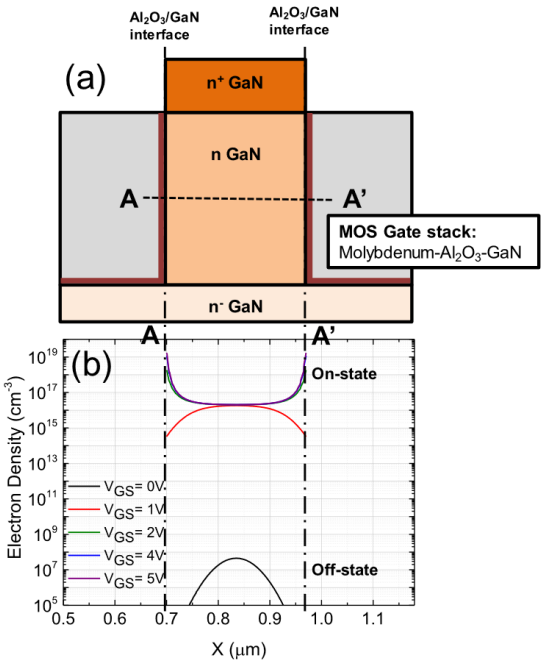


Figure 58 (a) Structure of the GaN VFET. (b) Electron density simulation in the n-GaN channel (along the A-A′cut) under different gate bias: for V_{GS}=0V the device is in OFF condition, hence the electron density in the channel is low and the maximum is located in the center of the n-GaN region far from the interfaces. At low gate voltage (V_{GS}=1V), the e-density is still relatively low

($\leq 10^{15} cm^4$). At high gate voltages (V_{GS}>2 V), the electron density peaks at the Al_2O_3/GaN interface [https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7968303] [261]

However, the fin needs to be sufficiently narrow (< 500 nm) to be completely depleted, which degrades the current capability of the device. The initial devices presented by Sun et al. [260] from MIT revealed a threshold of 1 V, $R_{on,sp}$ of 0.36 mΩcm^2, and a BV of 800 V with a fin width of 450 nm. The device works by accumulation of electrons rather than by inversion as in the case of trench gate MOSFETs and high electron mobility of 150 cm^2/Vs was obtained in the accumulation layer. Zhang et al. [259] further optimized the fin width to obtain a higher BV of 1200 V and a lower $R_{on,sp}$ of 0.2 mΩcm^2 , normalized to the total device area (Figure 56(b)). Large area devices with a current capability of 10 A and a BV of 800 V were also demonstrated simultaneously. Switching characteristics [262] of these fin power FETs with a BV of 1200 V and output current capability of 5 A were compared against commercial 0.9-1.2 kV class Si and SiC power transistors, revealing the lowest input capacitance (C_{ISS}), output capacitance (C_{OSS}), gate charge (Q_G), gate to drain charge (Q_{GD}), and reverse recovery charge (Q_{rr}). These devices exhibited high-frequency (~MHz) switching capabilities and superior switching figure of merits (FOMs) as compared to Si and SiC devices used for comparison. However, these devices break catastrophically, which is possibly due to the absence of p-GaN layers to modulate the electric field peaks. Also, the fabrication and control of the fin width could increase the fabrication complexity compared to other vertical devices. Since the threshold voltage is relatively low ~ 1V, a well-designed gate driver is required to ensure fail-safe operation. Recently, fin-FET and nanowire-based structures based on a npn vertical stack have been proposed to obtain robust normally-off operation [263], [264]: the integration of a p-type layer in a 3D stack (either nanowire- or fin-based) was demonstrated to be a good strategy for achieving robust normally-off operation, also under gate-stress experiments [265] (Figure 59).

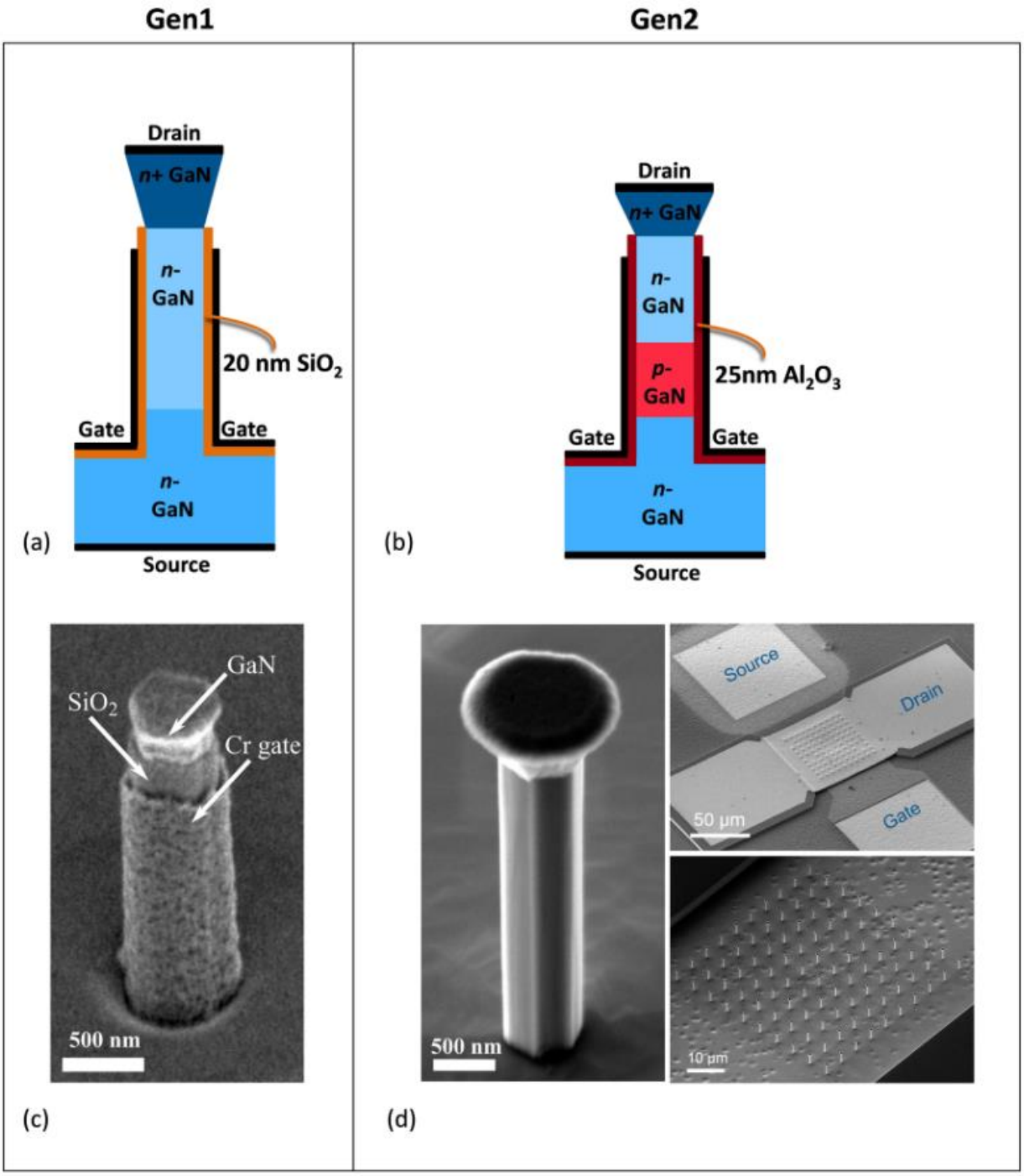


Figure 59: Cross section of a nanowire GaN device processed on a sapphire substrate. (a) The n-channel device (Gen1) consists of a 2.5 µm-GaN buffer layer, a 2 µm-GaN channel layer, a 0.5 µm-GaN top layer, and a 20 nm-SiO2 gate dielectric. (b) The p-channel device (Gen2) comprises a 2.5 µm-GaN buffer layer, a 0.5 µm p-GaN channel layer, 0.73 µm -GaN and 0.5 µm-GaN as the top layer, and 25 nm-Al_2O_3 as the gate dielectric. (c) SEM image of a nanowire of the n-channel device(Gen1); (d) SEM images of a nanowire

of the p-channel device (Gen2) and bird's-eye view of vertically aligned n-p-nGaN nanowire (NW) arrays with top contacts [265].

*Recent development of vertical devices on GaN on Silicon***:**

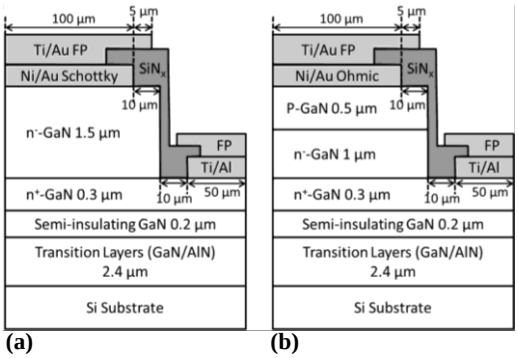


Figure 60 Schematic structure of a GaN-on-Si (a) Schottky diode (https://ieeexplore.ieee.org/abstract/document/6786327) and (b) p-i-n diode. (https://ieeexplore.ieee.org/abstract/document/6786327). [266]

As presented in the previous sections, the ideal solution for obtaining high quality GaN layers with defect density less than $10^6/cm^2$ would be homo-epitaxy i.e., GaN grown on bulk GaN, as there would not be any lattice mismatch between substrate and epitaxial layer. However, even after the demonstration of high-performance diodes and transistors with excellent ON- as well as OFF-state characteristics, the commercialization of vertical GaN power devices have been hindered by the high cost and the small diameter of these bulk GaN substrates. Currently, these expensive substrates are being used only for specific applications in lasers and LED [185]. Hence, in order to take advantage of the material benefits that GaN offers for power device applications, further improvements in wafer size and reduction in cost are highly desirable. A strategy to tackle this issue is by adopting GaN grown on cheaper foreign substrates like Si and sapphire. GaN-on-Si growth has been widely researched and commercialized for the lateral GaN HEMT technology. A similar approach could be embraced for vertical power devices as well. Furthermore, GaN-on-Si growth could give 10-100 times lower wafer + epitaxy cost [183], [267] as compared to bulk GaN. Silicon substrates also provide better thermal and electrical conductivity as compared to sapphire, in addition to more mature fabrication processes for the back-end processing. But the main

advantage of GaN on Si is that Si substrates are commercially available up to 12-inch diameters which could drastically reduce the overall cost per unit of the device. The adoption of Si substrates could also allow current CMOS compatible fabs to mass produce GaN-on-Si device thus saving the high cost normally required for setting up new technology fabs. Recently, a new class of engineered substrates with poly-AlN has been introduced [268]–[271]. The main advantage of these substrates is their coefficient of thermal expansion (CTE) matched to GaN and thus enabling the growth of thick, high-quality stress-free GaN with lower defect density as compared to GaN-on-Si substrates [30, 102]. Thus, the future for GaN-on-Si vertical devices seems very promising.

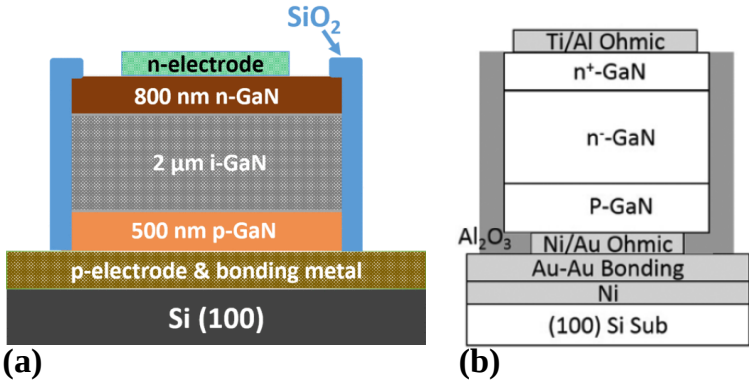


Figure 61 Schematic structure of a completed GaN-on-Si fully-vertical p-i-n diode fabricated by substrate removal and bonding to a carrier wafer by (a) Zou et.al (https://ieeexplore.ieee.org/document/7444154) [272] and (b) Zhang et al.. (https://ieeexplore.ieee.org/abstract/document/7802635) [273].

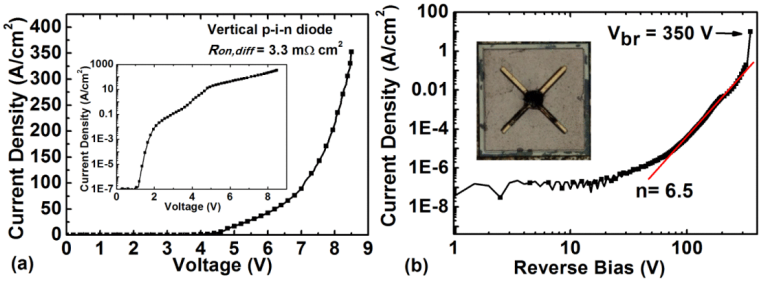


Figure 62 Forward and (b) reverse I-V characteristics of vertical PiN diodes. Inset shows the anode region after destructive breakdown. https://ieeexplore.ieee.org/document/7444154 [272]

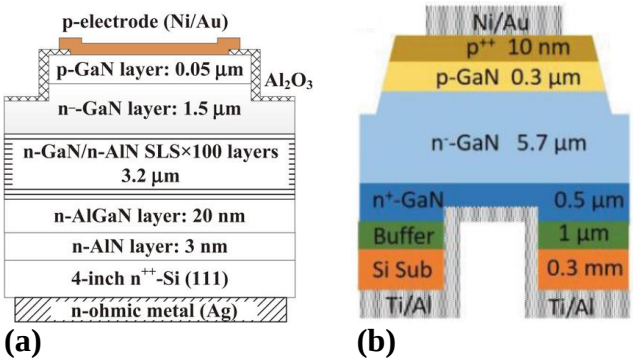


Figure 63 (a) Schematic cross section of the a fully vertical GaN p-i-n diode on Si substrate grown by MOCVD (https://iopscience.iop.org/article/10.7567/APEX.9.111005/meta) [274]. (b) Fully vertical GaN-on-Si p-in diode by selective substrate removal. (https://ieeexplore.ieee.org/abstract/document/8325453) [275].

GaN-on-Si p-i-n diodes have been demonstrated since 2014. Zhang et al. demonstrated the first GaN-on-Si p-i-n and Schottky diodes [266] with a BV of 300 V and 205 V respectively (Figure 60). Even with a high defect density of $10^9/cm^3$, a peak electric field of 2.9 MV/cm could be achieved. The current leakage paths, leakage mechanisms and methods to improve the leakage current were thoroughly researched and identified in a later work [267]. A device termination scheme based on ion implantation and anode field plate was found to reduce the leakage current by almost two orders of magnitude. For GaN layers grown on Si substrates, the traditional device structure is quasi-vertical, in which both top and bottom layers are accessed through the device top surface. This results in a non-uniform distribution of current from the anode and current crowding at the bottom GaN layer near the cathode terminal. In order to alleviate this issue, Zou. et al., demonstrated a method of making a fully-vertical p-i-n diode [272] by removing the Si substrate below the GaN layers, followed by transfer of GaN epilayers to a carrier wafer as shown in Figure 61(a). The finished p-i-n diode presented an $R_{on,sp}$ of 3.3 $m\Omega cm^2$ and a BV of 350 V (Figure 62). Excellent temperature stability up to 175 °C was also observed during ON- as well as OFF-state measurements. Zhang et al. demonstrated a similar method of achieving fully-vertical p-i-n diodes [273] but with better $R_{on,sp}$ of 1 $m\Omega cm^2$ and BV of 500 V (Figure 61(b)). A low reverse recovery

time of 50 ns comparable to bulk GaN diodes were extracted along with excellent thermal stability of the devices up till 300 °C. Mase et al. [274], demonstrated a novel method of achieving a fully vertical GaN-on-Si p-i-n diode by using a conductive n-type Si substrate along with n-type buffer layers (Figure 63(a)). An interesting feature of their p-i-n heterostructure was the use of a 3.2 µm thick strained super lattice (SLS) of n-GaN/n-AlN. Sufficiently thick SLS layer (~ 3 µm) was necessary to control the edge dislocations to an appreciable value ~ 2×10^9 /cm^2 which also dictated the lowest doping level possible for the GaN layers grown over the SLS layer. The devices presented an $R_{on,sp}$ of 7.4 mΩcm^2 and a BV of 288 V. A detailed analysis of current crowding effect in quasi-vertical structures were provided by Zhang et al. in 2017 [169]. According to this research, the thickness and the doping of the bottom n-GaN current collecting layer determines the $R_{on,sp}$ and a thick highly doped bottom n-GaN is required to ensure lower levels of current crowding. High voltage GaN-on-Si p-i-n diodes were demonstrated by Khadar et al. in 2018 [276]. These diodes had a BV of 820 V with just a 4 µm thick drift layer and an ultra-low $R_{on,sp}$ of 0.33 mΩcm^2 resulting in a record value of 2 GW/cm^2 for the BFOM. The growth of these layers was optimized to obtain i-GaN layers with an excellent electron mobility of 720 cm^2/Vs and a low defect density of 2×10^8/cm^3 for GaN grown on Si. Shortly after, Zhang et al. [275] demonstrated a new method of achieving fully-vertical operation for GaN-on-Si p-i-n diodes by selective Si removal underneath the active area of the device followed by metallization (Figure 63(b)). An $R_{on,sp}$ of 0.35 mΩcm^2 and a BV of 720 V was achieved.

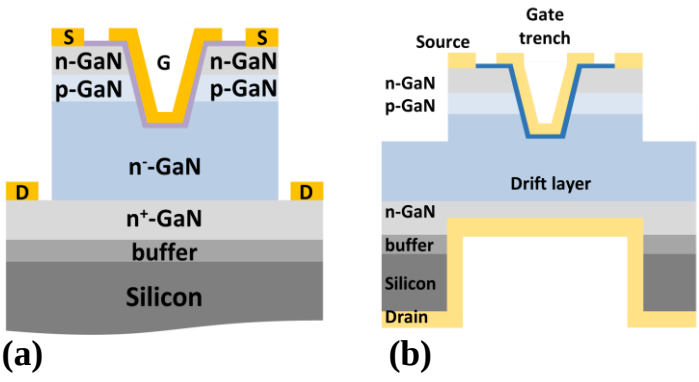


Figure 64 (a) Schematic cross section of the a quasi-vertical GaN power MOSFET on Si substrate (https://ieeexplore.ieee.org/abstract/document/8125763) [277] (b) Fully-vertical GaN-on-Si

power MOSFET by selective substrate removal. (https://ieeexplore.ieee.org/abstract/document/8621009) [278].

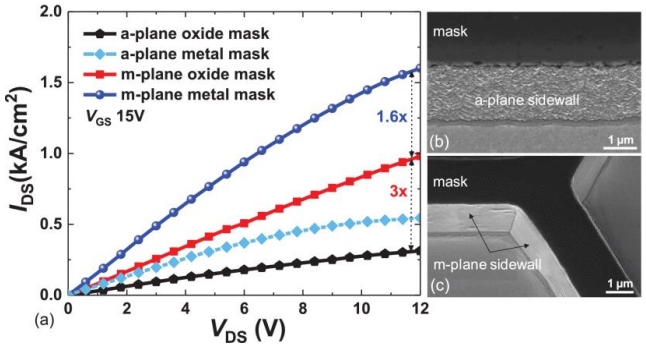


Figure 65 (a) Comparison of the I_{DS} -V_{DS} of the fabricated vertical MOSFETs with gate trench aligned along m- and a-plane, using metal and oxide hard masks. SEM images of the trench sidewall aligned along the (b) a-plane and (c) m-plane, after TMAH wet treatment. Notice the much smoother m-plane sidewalls compared to the a-plane. https://ieeexplore.ieee.org/document/8621009 [278]

GaN-on-Si vertical power MOSFETs have been also demonstrated, with the first demonstration being from Liu et al. in 2017 [277] (Figure 64(a)). Normally-off operation with a threshold voltage of 6.3 V, which is ideal for power converter applications, along with an ON/OFF ratio of over 10^8 were achieved. The device presented a low $R_{on,sp}$ of 6.8 mΩcm^2 and a BV of 645 V which is comparable to bulk GaN power MOSFETs. The first demonstration of fully-vertical MOSFETs was subsequently devised by Khadar et al. [278] (Figure 64(b)). The method involved a robust fabrication process including selective substrate removal underneath the MOSFET followed by ohmic contact deposition and copper electroplating to provide strength to the thin free standing epitaxial GaN layers. An $R_{on,sp}$ of 5 mΩcm^2 and a BV of 520 V was obtained. These devices exhibited 2.8x-higher current density and 3x-lower $R_{on,sp}$ as compared to quasi-vertical control power MOSFETs, due to absence of current crowding. Also, insights into the impact of hard mask selection for gate trench etching and gate trench alignment to either the m- or a-plane sidewall, on the output current density was analyzed (Figure 65). Devices having gate trench aligned along the m-plane provided 3x-higher output current as opposed to those with gate trench aligned along the

a-plane. The use of a metal mask for gate trench etching provided a high inversion channel field-effect mobility of 41 cm^2/Vs for electrons.

GaN-on-Si technology offers a unique advantage for the possible integration of several different devices on the same chip to realize integrated circuits (IC) which have evident benefits like smaller IC foot print, greatly reduced parasitic capacitance and resistance arising from wire bonding of discrete devices leading to higher efficiency, lower cost, etc. To date several different integration schemes on GaN-on-Si lateral technology has been demonstrated with HEMTs [279]–[282]. Liu et al. demonstrated the first vertical monolithically integrated device [283] in 2018, where a freewheeling Schottky barrier diode was integrated with the power MOSFET (Figure 66), to overcome the lossy body diode by using a fast low turn-on voltage SBD. In several topologies of power converters, such as buck/boost converters, voltage-source inverters, and resonant converters, where an inductive load is controlled by switches, a freewheeling diode parallel to the power MOSFET is required to allow a reverse flow of current when the supply current to the load is suddenly interrupted. The integrated SBD was created by dry etching the top n- and p-GaN layers followed by TMAH treatment to smoothen the surface and then Schottky metallization. The integrated MOSFET/diode provided excellent forward and reverse characteristics. In particular, the freewheeling diode presented a low turn-on voltage of 0.76 V, low $R_{on,sp}$ of 1.6 $m\Omega cm^2$, ideality factor of 1.5 and an excellent BV of 254 V achieved without any additional termination mechanisms.

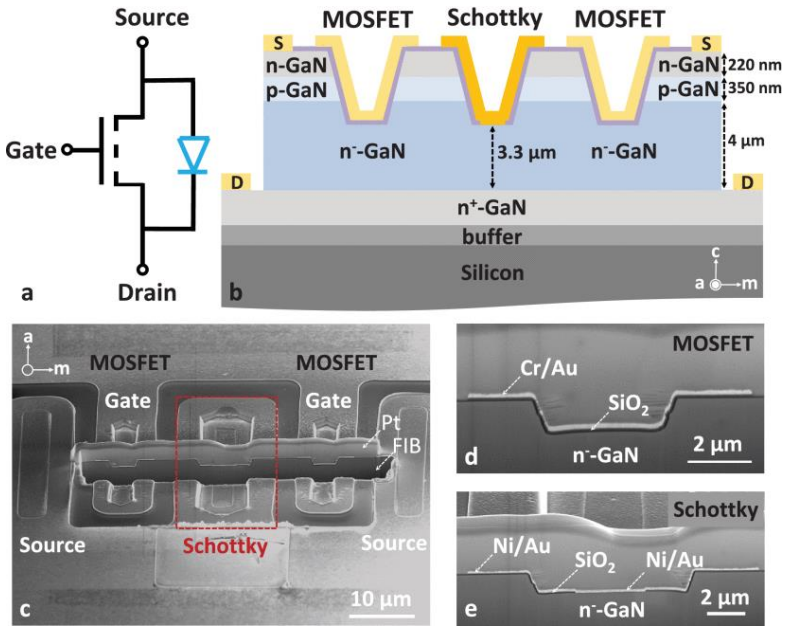


Figure 66 (a) Equivalent circuit, (b) Schematic of integrated vertical MOSFET-Schottky barrier diode (SBD). (c) SEM image of integrated vertical MOSFET-SBD, (d) Cross-sectional SEM image of the integrated vertical MOSFET, and (e) of the integrated vertical SBD. (https://ieeexplore.ieee.org/abstract/document/8370664) [283]

Recently, the optimization of GaN-on-Si semivertical devices has been the subject of pioneering projects in the field, working with silicon substrates up to 200 mm in diameter. As an example, we mention recent papers aimed at optimizing the full GaN-on-Si structure, with focus on the Mg-doping in the p-body layer [253], the thickness of the gate insulator [253], and the dielectric material used at the gate [284], with the aim of minimizing on-state resistance and charge trapping, and of obtaining high breakdown voltage [285].

7.4 Open Challenges:

GaN based vertical power devices could be used for realizing the next generation power efficient converters provided that pertinent issues related to material quality, device fabrication and performance can be solved. Compared to Si and SiC, bulk GaN crystal growth process is highly challenging requiring high temperatures > 2200 °C and nitrogen pressure > 6 GPa making it impossible to crystallize GaN from the melted compound [175]. Hence, lower pressure and temperature methods like hydride vapor phase epitaxy (HVPE), sodium flux and acidic/basic

ammonothermal growth method has been utilized to realize bulk GaN substrates. Even so, the defect density in these substrates are around 10^4-10^6 /cm^2, the effect of which has to be closely scrutinized for use in commercial applications. In general, Si and SiC devices are qualified by the fully Joint Electron Device Engineering Council (JEDEC), which will also have to be done for GaN-based vertical power devices. For GaN HEMTs it was realized that conventional JEDEC guidelines for Si based devices are not sufficient and led to the creation of new JEDEC standards JC-70, JEP-180 and JEP-173 for GaN based devices [286]–[288]. A similar situation may arise for vertical GaN, and guidelines used for Si, SiC and lateral GaN may be adopted or refined, following a in depth discussion by the involved community.

Conventional Si and SiC power devices rely on the selective doping capability by ion implantation or by diffusion to achieve junction termination structures (JTEs) which have been proven to be indispensable for achieving reliable devices with avalanche capability [289]. However, for GaN, doping by ion implantation is still a highly complex process requiring specialized instruments capable of high-temperature [290] (> 1200 °C) and high-pressure conditions [291] (> 1 GPa). Selective area growth is another option which has been investigated but with little success due to the presence of high concentration (> 10^{18} /cm^3) of Si atoms at the regrowth interface [200], [292]. Several schemes like Ar ion implantation, plasma-based treatments described in the previous sections, have been adopted for GaN based vertical devices, however their suitability for large scale production and long-term reliability is still unclear. There are also concerns related to the low activation efficiency (~ 1%) of p-GaN grown by MOCVD due to the high bond energy of the stable Mg-H complexes formed during the growth process [293]–[295]. Even high temperature annealing (~ 750 – 850 °C) activates only a small fraction of the dopant atoms (Mg concentration > 10^{19} /cm^3) thus presenting a low hole concentration typically around 10^{17} /cm^3 [296], [297] with low hole mobility due to scattering from the dopant atoms present in large concentrations. This is in particular not desirable for GaN trench power MOSFETs since the high concentration of dopant atoms in the p-GaN channel region scatters the electrons formed by inversion during normal ON-state operation, thereby degrading the channel mobility [254], [277], [298] and thus the output current. The low hole mobility of the p-GaN layers also affects the resistance of p-i-n diodes and results in ON-state losses.

Adoption of bulk GaN for commercialization is not only hindered by the high cost and the small size of these substrates but also by the huge initial investment needed for the setting up GaN specific fabs, which could shoot up the average selling price (ASP) of discrete devices slowing down further the adoption of these devices. Hence it is vital to make significant strides in the improvement of substrate size as well as cost of these bulk GaN substrates.

GaN-on-Si could offer an alternative to lower the device costs, but significant progress has to be made on the GaN quality with low defect density and on the thickness of the GaN layers grown on Si substrates, in order to enable larger voltage devices. The advent of CTE matched substrates available in large wafer diameters [299] may further push the development of vertical GaN power devices.

8 Charge-trapping processes in GaN transistors

The presence of deep-level traps [300]–[302] in GaN and its alloys and the effects of the associated charge capture/emission processes can rarely be neglected in GaN transistors under their typical operating conditions in power RF amplifiers and power switching converters. As will be detailed, figures of merit that are key to these applications and that can detrimentally be affected by trapping processes include output power (P_{out}) and power-added efficiency (PAE) in RF amplifiers, switching and conduction losses in power converters.

Spatial position of traps within the device (surface, barrier, buffer and, if present, gate dielectric), trap parameters [301], [302] (energy, capture cross sections, concentration, acceptor- or donor-like behavior), type of involved carriers (electrons or holes) and the associated charging/discharging path (contact injection/removal, carrier generation, internal redistribution) can all play a role, and their signatures on transistor operation should be known by the technologist for a proper device optimization.

The detrimental consequences of charge-trapping processes include several, widely studied dynamical effects, including: the current collapse [303]–[307], the increase in the dynamic on-state resistance (dynamic R_{ON} [308]–[311]), different forms of threshold-voltage (V_T) instabilities [312]–[318], and the kink effect [319], [320]. These phenomena are at the same time the incumbent burden of traps and the way the latter can be probed.

In addition, several trap measurement methods have been devised and extensively applied to GaN structures and transistors, in order to quantitatively characterize traps.

This section is organized as follows. First, the properties of the most common traps in GaN are reviewed, to help the reader understanding the complexity of the topic. Second, the most important trapping mechanisms affecting GaN transistors are elucidated by crossing the different trap locations with the corresponding possible charging/discharging paths. Then, the resulting trap effects and their relevance for applications are reviewed. Finally, methods that can be adopted for measuring trap parameters are reviewed.

8.1 Traps and deep levels in GaN

The properties of gallium nitride as a semiconductor material are determined by the specific periodicity of its crystalline structure. If this periodicity is lost, either due to incorporation of foreign atoms into the crystal or to a non-ideal arrangement of the host atoms during the growth of the material, a defect is locally generated. Defects are referred to as "impurity-related" in the former case, whereas they are defined as "native" in the latter. The presence of these defects locally perturbs the periodic potential of the lattice, therefore introducing allowed energy states within the forbidden bandgap of the material. These states, that can either act as carrier traps or recombination centers, can have a detrimental impact on both the performance and the reliability of GaN-based devices. It is therefore of primary importance to identify the properties and the physical origin that such states have in actual GaN devices. To this aim, a database of traps and deep-levels related to the GaN material system has been created by collecting and comparing the data of almost one hundred scientific publications (Table 7). The comparison of the 480+ records of traps experimentally detected in GaN by means of various techniques allowed us to correlate energy positioning, signature and trapping behavior of the levels accredited to the defects most commonly found in GaN. In the following paragraphs we report the outcome of the study of such defects based on energetic-positioning considerations.

Type of defect or impurity	**Physical origin**	**Reported E_a (eV)**	**Detected as**	**References**
NATIVE DEFECTS				
Nitrogen interstitial	N_I-related	1 to 0.76	EC -	[321]–[325], [326]*,&, [327]
		2.42	EV +	[328]
Nitrogen antisite	N_{Ga}-related	0.66 to 0.5	EC -	[322], [326], [329]–[338]
		2.48	EV +	[339]
Nitrogen vacancy	V_N-related	0.27 to 0.089	EC -	[323], [337], [340]–[342], [332]&, [343], [344], [331]&, [345], [346], [329]*, [347]&, [326], [327], [338], [342], [343], [348]–[351], [352]*
		0.4	EC -	[350]
		3.28	EV +	[328]

	V_N or Mg_{Ga}-V_N	3.18	EV +	[339]
	V_N complexes	0.35	EC -	[323]
	$(V_N)^{3+}$	0.53	EC -	[351]
	V_N clusters	0.613	EC -	[343]&
Gallium interstitial	Ga_I complexes	0.91	EC -	[353]&
	Ga_I-related	0.8	EC -	[327]*
Gallium vacancy	V_{Ga} or unspecified complexes (main band)	2.85 to 2.47	EC -	[346], [348], [354]–[358], [359]*
		1.02, 0.83 and 0.89, 0.9, 0.86	EV +	[324], [328], [327]*, [330]
	V_{Ga}-O	1.12, 0.64, 0.6	EC -	[335]
	V_{Ga}-related	0.62	EC -	[347]
		1.8	EV +	[339]
		0.25	EV +	[350]
	V_N-V_{Ga} complexes	0.24	EC -	[329]*
Extended defects	Many	1.118 to 0.24	EC -	[341]&, [335]*, &, [348]&, [333]&, [323]&, [360]&, [326]*,&, [361]&, [330]&, [352]&
IMPURITIES-RELATED DEFECTS				
Silicon	Si-related	0.59	EC -	[362]
		0.4	EC -	[341]
		0.37	EC -	[341]
Magnesium	Shallow acceptor level	0.16 to 0.24	EV +	[357]*, [346], [359], [363], [339]**
	Mg-H complexes	0.08	EV +	[364]*
		0.62	EC -	[357]
	Mg-related	0.355, 0.597	EC -	[340], [365]
	Mg-V_N complexes	0.44	EC -	[349]
Hydrogen	H-V_{Ga} complexes	2.62 to 2.47	EC -	[346], [356]
	C- or H-related	0.578, 0.49	EC -	[366]*, [367]*
Oxygen	O-V_{Ga} complexes or dislocations	1.118, 0.642, 0.599	EC -	[335]&
	O_N	0.44, 0.01	EC -	[368], [350]*
Iron	Fe-related	0.397, 0.5, 0.57, 0.66, 0.68, 0.72	EC -	[334], [354], [369], [370]
		2.5	EV +	[371]
	Fe^{2+} or Fe^{3+} related	0.34	EC -	[372]
		3	EV +	[371]
Carbon	$(C_N)^0$	3.31 to 3.22	EC -	[357]*, [346], [348], [356], [358], [373], [374], [353]*, [330], [375], [352]*

		0.29	EV +	[364], [376]
	$(C_N)^{-1}$	0.8 to 0.95	EV +	[329], [364], [375]*, [330], [376], [377]
	C_I	1.35 to 1.2	EC -	[346], [348], [357], [352]*
	C- or H-related	0.578, 0.49, 0.14	EC -	[366]*, [367]*, [367]*
	C_{Ga}	0.4	EC -	[329]*

Table 7 Database of traps detected in GaN- and AlGaN-based devices. References marked with * , & and ** indicate, respectively, tentative associations, traps related to extended defects and tentative grouping performed by the authors of this work. Activation energies and related references are reported in the same order.

Native defects

The position of the trap levels associated with native defects in GaN are reported in Figure 67. These levels are mainly related to nitrogen interstitial (N_I), nitrogen antisites (N_{Ga}), nitrogen vacancies (V_N), gallium interstitials (Ga_I), gallium vacancies (V_{Ga}), to clusters of the former or to unspecified extended defects (mostly dislocations).

Nitrogen interstitials have been reported to introduce trap states between E_C - 1.2 eV and E_C – 0.76 eV [321]–[328], with average preferential energy positioning at E_C – 1.02 eV, E_C – 0.89 eV and E_C - 0.79 eV. The former and the latter levels have also been tentatively associated with an extended defect in [326]. Among nitrogen-related native defects, nitrogen interstitials exhibit the highest activation energy, allowing them to act both as traps or recombination centers.

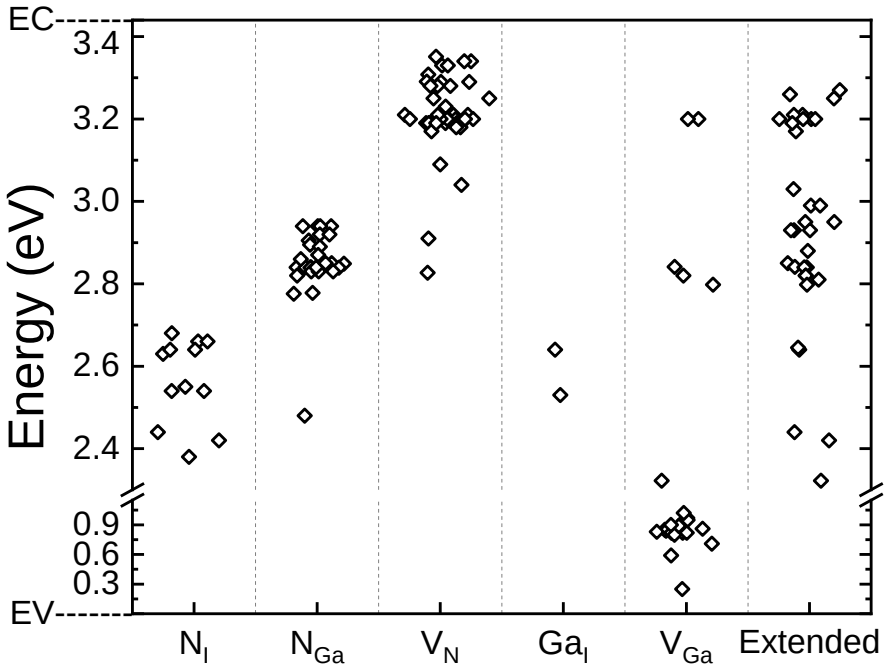


Figure 67 Energy states detected in GaN and associated to native or extended defects. The reference level, assumed to have an energy equal to 0, is related to the top of the valence band. The scatter-like representation highlights the preferential energy assignment of the detected traps with respect to a specific type of defects.

Nitrogen antisite defects are assumed to form a mini-band of levels between $E_C - 0.66$ eV and $E_C - 0.5$ eV [322], [326], [329]–[339]. None of the aforementioned reports suggests a direct correlation between the levels associated to nitrogen antisite defects and extended defects.

Nitrogen vacancies represent the most commonly observed type of native defect in GaN, with more than 40 records in 25 different scientific publications [322], [326], [329]–[339]. The associated trap states are preferentially positioned in the $E_C - 0.27$ eV to $E_C - 0.089$ eV range, with most of the occurrences belonging to the mini-band at $E_C - (0.24 \pm 0.003)$ eV identifying the typical level associated to nitrogen vacancies in GaN. The outliers of the aforementioned distribution are represented by the deeper $E_C - 0.35$ eV [323], $E_C - 0.4$ eV [350], $E_C - 0.53$ eV [351] and $E_C - 0.613$ eV [343] levels, respectively associated with V_N complexes, simple nitrogen

vacancies, triply ionized nitrogen vacancies and clusters of vacancies. Other V_{Ga}-related levels whose physical origin was found to be compatible with an extended defect are located at $E_C - 0.19$ eV [332], at $E_C - 0.23$ eV [331], [332] and at $E_C - 0.25$ eV [347]. The fact that trap levels with similar Arrhenius signatures, and therefore similar activation energy and cross-section, have been associated both with extended and point defects suggests that even if the capture rate of the defect is influenced by the electrostatic repulsion due to the close proximity to other ionized traps or to extended crystal defects, gallium vacancies tend to maintain their characteristics emission properties.

Gallium interstitials are reported as the physical origin of traps detected in GaN by only a couple of papers. In [353], an $E_C - 0.91$ eV level was associated with Ga_I complexes located along dislocations. In [327], a trap located at $E_C - 0.8$ eV was tentatively ascribed to gallium interstitials located in an unspecified layer of an AlGaN\GaN HEMT.

Gallium vacancies are often associated with deep levels responding in the $E_C - 2.42$ eV to $E_C - 2.85$ eV range, with most occurrences roughly located at $E_C - 2.6$ eV [324], [327], [328], [330], [346], [348], [354]–[359]. Some of these traps have been tentatively associated with oxygen- [324], [327] or hydrogen- [346], [356] related complexes formed with V_{Ga}. Also the $E_C - 1.12$ eV, the $E_C - 0.64$ eV and the $E_C - 0.6$ eV levels found in [335] have been referred to as V_{Ga}-O-related defects, whereas the other deep levels detected outside the band of reference for this particular type of native defect have been associated to V_N-V_{Ga} complexes (at $E_C - 0.24$ eV in [329]) or to simple gallium vacancies (at $E_C - 0.62$ eV in [347], at $E_C - 1.64$ eV in [339] and at $E_C - 3.19$ eV in [350]).

Trap states related to **extended defects** have been found to cover a wide and non-continuous portion of the upper part of the GaN bandgap, ranging from $E_C - 1.118$ eV to $E_C - 0.24$ eV [323], [326], [330], [333], [335], [341], [348], [352], [360], [361]. Interestingly, the upper group of levels, scattered from $E_C - 0.27$ eV to $E_C - 0.17$ eV, covers the same range of activation energies exhibited by V_N-related defects. Similarly, also a second mini-band of deep levels associated to extended defects, and scattered from $E_C - 0.641$ eV to $E_C - 0.41$ eV, finds a correspondence with the typical range of response of N_{Ga}-related defects. These considerations suggest that both nitrogen vacancies and nitrogen antisite defects can be found in proximity of other defects, and therefore behave as interacting defects. Interestingly, no defects with activation energies corresponding to the V_{Ga} band

were ascribed to extended defects, possibly suggesting that this type of native defect tends to predominantly behave as a non-interacting point defect, or does not form in highly defective device regions.

Impurity-related defects

Imperfections of the lattice structure may also arise from the inclusion of atomic species that nominally do not belong to the GaN crystal. Such atoms, or atom complexes, are referred to as impurities. These impurities can either be intentionally introduced into the material, as in the case of dopants, be originated as the byproduct of the chemical reactions occurring during crystal growth, or derive from unwanted contaminations. Si and Mg represent the main doping species for GaN. Similarly, Fe and C can be intentionally introduced in order to compensate for the intrinsic n-type conductivity of GaN, Others may act as unwanted contaminants, like residual O and H atoms. A more detailed description of the deep levels introduced by these impurities is provided in the following paragraphs.

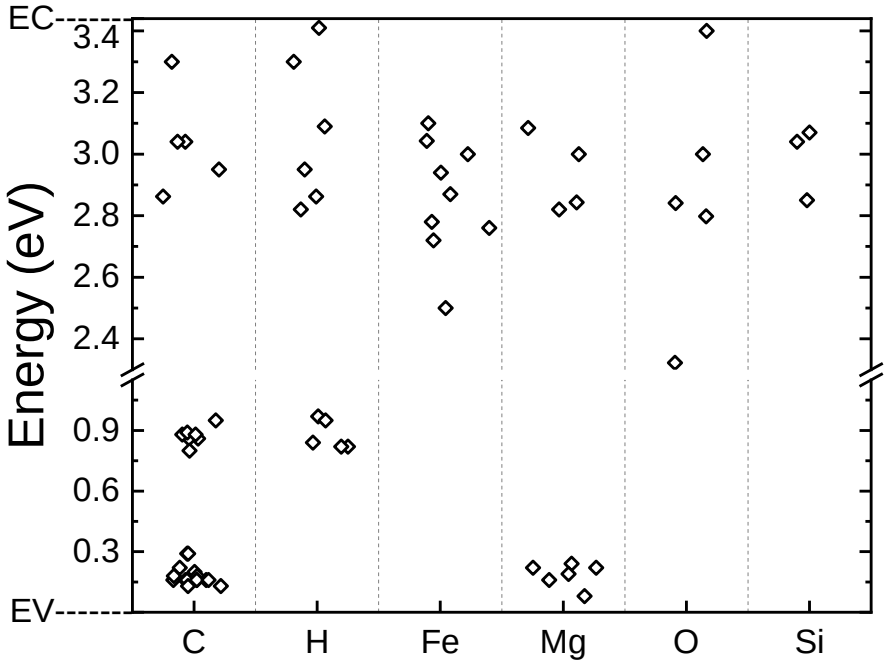


Figure 68 Energy states detected in GaN and associated to impurities-related defects. The reference level, assumed to have an energy equal to 0, is represented by the top of the valence band. The dispersion of the detected levels within the lower portion of the forbidden gap has been magnified with respect to Figure 67.

Aside from its shallow donor level, which has a typical activation energy ranging from $E_C - 0.011$ eV to $E_C - 0.028$ eV for moderately doped GaN layers [378]–[380], only few scientific reports attribute to **silicon** deeper allowed energy levels, respectively located at $E_C - 0.37$ eV [341], $E_C - 0.4$ eV [341], $E_C - 0.59$ eV [362].

Magnesium is employed in GaN devices in order to achieve p-type conductivity. Trap states detected near the valence band edge at $E_C - 3.2$ eV [363], $E_C - 3.22$ eV [346], [357], $E_C - 3.25$ eV [359] and $E_C - 3.28$ eV [339], even if nominally assigned to other physical origins, can reasonably be ascribed to the shallow level of the dopant, which is known to be typically located from 0.15 eV to 0.2 eV above the valence band edge [381], [382]. A shallower level at $E_C - 3.36$ eV [364] was tentatively ascribed to Mg-H complexes, and a similar origin was assigned to the $E_C - 0.62$ eV level in [357]. Additional levels at $E_C - 0.355$ eV [340] and at $E_C - 0.597$ eV [365] were ascribed to generic Mg-related defects, whereas the $E_C - 0.44$ eV level in [349] was associated with Mg-V_N complexes.

Due to its unpaired valence electron, **hydrogen** is prone to form complexes with other chemical species in addition to magnesium. Different authors ascribe deep levels located between $E_C - 2.62$ eV and $E_C - 2.47$ eV to complexes formed between hydrogen and gallium vacancies [346], [356], even if the similarity between this range and the preferential energy positioning of V_{Ga}-related defects indicates that those levels may be ascribed to the latter. Levels at $E_C - 0.49$ eV and $E_C - 0.578$ eV were tentatively assigned to carbon- and/or hydrogen-related defects, respectively in [367] and [366].

Due to its very-high electronegativity, also **oxygen** tends to bond with other impurities of native defects within the GaN crystal. One of the few literature reports investigating the formation of deep levels related to O in GaN associates the levels at $E_C - 1.118$ eV, $E_C - 0.642$ eV and $E_C - 0.599$ eV either to V_{Ga}-O complexes or to dislocations [335]. In [368] the $E_C - 0.44$ eV level was ascribed to O_N. The same interpretation was provided by the authors in [350] to tentatively explain

the shallow E_C – 0.04 eV donor level detected by means of PL measurements as part of a donor-acceptor pair.

Iron is often adopted in GaN-based transistors to intentionally reduce the intrinsic n-type conductivity of specific u.i.d. GaN layers. Several levels, ranging from E_C – 0.94 eV to E_C – 0.34 eV, have been detected and associated to Fe [334], [354], [369]–[372]. In particular, the authors in both [372] and [371] agree when associating shallower deep states, respectively detected at E_C – 0.34 eV and E_C – 0.44 eV, to transitions between, or related to, different charge states of the Fe atoms. Recent reports deeply investigated the signatures of Fe-related traps [111], [383], [384]; it was recently suggested that Fe_{Ga} sites are related to a trap located at E_C-0.58 eV, $\sigma=2x10^{-15}$ cm^2 [383].

Like iron, also **carbon** doping is used to compensate the intrinsic n-type conductivity of the GaN crystal. This effect is achieved when C atoms occupy a substitutional position on the nitrogen site (C_N). C_N is a deep acceptor, with the (0/-) transition level theoretically located at E_V+0.9 eV [385], and experimentally associated with a band of allowed states between E_C – 2.64 eV and E_C – 2.49 eV [329], [330], [364], [375]–[377]. Being a deep acceptor, the C_N level does not generate large free hole density and strong p-type conductivity; large concentrations of C_N can pin the Fermi level at E_V+0.9 eV, leading to semi-insulating layers. C_N may also induce the formation of shallow acceptor-like levels in the E_C – 3.31 eV to E_C – 3.15 eV band [330], [346], [348], [352], [353], [356]–[358], [364], [373]–[376]. On the other hand, if C occupies interstitial positions, the resulting C_I sites are believed to introduce a deep donor level in the upper part of the gap, with typical energies ranging from E_C – 1.35 eV to E_C – 1.2 eV [346], [348], [352], [357]. Other shallower levels at E_C – 0.14 eV [367], E_C – 0.4 eV [329], E_C – 0.49 eV [367] and E_C – 0.578 eV [366] have been tentatively ascribed to carbon- or hydrogen-related defects, with a speculative assignment of the E_C – 0.4 eV to C_{Ga} sites.

8.2 Trapping mechanisms

Traps influence the electrical behavior of transistors since they are characterized by relatively long capture/emission times [301] and thus they charge up or discharge following fast bias changes more slowly than device capacitances that govern the “prompt” device response.

Regardless of the nature of traps, i.e. whether they are associated to intrinsic crystallographic defects, unintentional or intentional impurities or defect-impurity complexes, only those traps that have a chance to change their charge state during the device functioning through capture or emission of mobile carriers can induce electrical effects of concern for the dynamic device performance. Based on these considerations, trapping mechanisms can be categorized as the combination of a *trap location* plus an associated *charging/discharging path* and *type of involved mobile carriers.*

Traps can virtually be located in any semiconductor or dielectric layer as well as at interfaces, but locations that have more frequently been associated with harmful effects for GaN transistors include the device surface and the passivation within the gate-drain access region, the barrier, the buffer (including the interface with the barrier layer), and, if present, the gate dielectric (including the interface with the underlying semiconductor). The reported charging/discharging paths include all leakage currents from the device terminals (gate, source, drain, substrate), the 2DEG at the barrier/buffer interface in HEMTs and unrecessed or partially-recessed MIS-HEMTs or the channel at the dielectric/GaN interface in fully-recessed MIS-HEMTs, charge redistribution processes within floating C-doped buffer, as well as high-field mechanisms like field-enhanced emission, trap impact ionization, and Zener trapping. One or more of these paths can be activated depending on the applied device bias.

Two general remarks that will apply to all effects described below, are as follows.

1) Since all GaN transistors relevant for applications are n-channel field-effect transistors, traps can induce a reduction in the source-to-drain channel conductivity and, through this, in the drain current, if the negative trapped charge increases or the positive one decreases. These changes can either be the result of electron capture or hole emission. On the other hand, an increase in the channel conductivity and drain current can be promoted by electron emission or hole capture.

2) Trapping effects that take place in the device portion under the gate directly influence V_T, whereas those occurring in the gate-drain access region impact the drain access resistance and the transconductance peak.

Table 8 lists the major trapping mechanisms that have been reported in the literature classified in terms of trap location and corresponding charging/discharging path and type of involved mobile carriers. The different trapping mechanisms resulting from this classification will be described in more detail in the following sections.

Table 8. Classification of major trapping mechanisms in terms of trap location, charging/discharging path and type of involved mobile carriers.

Mechanism label	**Trap location**	**Charging/discharging path (type of involved carriers)**
Su1	Surface in the G-D access region	Gate contact (electrons)
Su2	Surface in the G-D access region	2DEG (electrons)
Ba1	Barrier	Gate contact (electrons)
Ba2	Barrier	2DEG (electrons)
Ba3	Barrier	Field-enhanced ionization (electrons)
Ba4	p-GaN/AlGaN interface	p-GaN (holes)
Bu1	Buffer	Source contact (electrons)
Bu2	Buffer	Gate contact (electrons)
Bu3	Buffer	Substrate contact (electrons)
Bu4	Buffer	2DEG (electrons)
Bu5	Buffer	Zener trapping (valence-band electrons)
Bu6	Barrier/buffer interface	Zener trapping (valence-band electrons)
Bu7	Barrier/buffer interface	Trap impact ionization (electrons)
Bu8	C-doped buffer	“Leaky-dielectric” buffer

Bu9	C-doped buffer	C doping (holes)
Ox1	Gate dielectric	Gate contact (electrons)
Ox2	Dielectric/semiconductor interface	Channel/2DEG (electrons)
Ox3	Dielectric/semiconductor interface	C doping (holes)

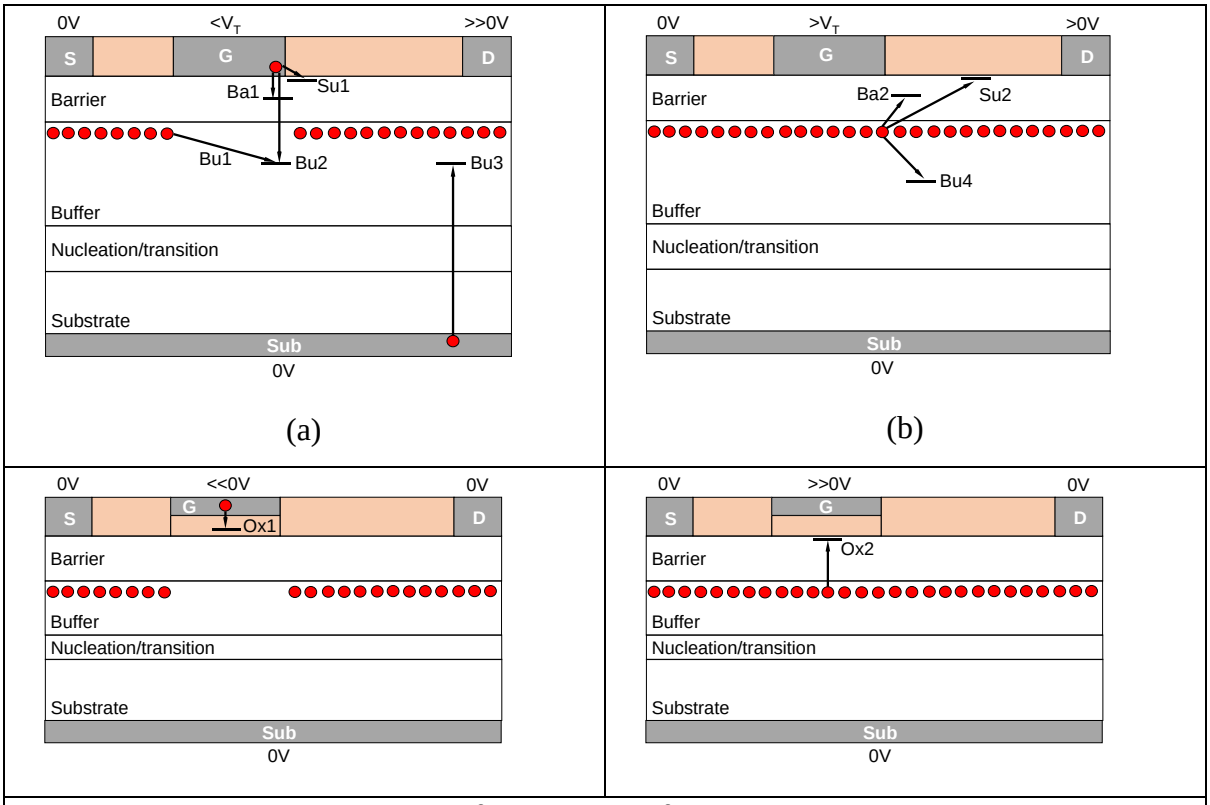


Figure 69. Schematic illustration of a selection of trapping mechanisms listed in Table 8, grouped according to bias conditions triggering the charging processes as follows: (a) off-state conditions at sub-threshold V_{GS} and large, positive V_{DS}; (b) semi-on or power-state conditions at above-threshold V_{GS} or large, positive V_{DS}, respectively; (c) negative gate bias; (d) positive gate bias. Red circles and small bars represent electrons and traps, respectively. Arrows illustrate the charging path (not direct electron transfer into traps).

8.3 Surface traps in the gate-drain access region

Surface traps in the gate-drain (G-D) access region (in following, simply, surface traps) can capture electrons injected by the gate contact in GaN HEMTs [mechanism Su1 in Table 8]. This occurs as

the device is biased under *off-state* conditions, i.e. when the gate is biased below threshold, and a large, positive V_{DS} is applied. Gate-injected electrons can leak across the passivation [303], [386]–[388] or propagate through surface traps by a hopping mechanism [389], [390]. Trapped electrons are then slowly emitted by traps following the device switching to *on-state* conditions, i.e. zero or positive V_{GS} with small, positive V_{DS}. To describe this mechanism, the "virtual gate" [303] concept has been used. In the early stage of the GaN HEMT development, this was the trapping process of major concern owing to the heavy limitation it could induce on the achievable RF output power and power-added efficiency. Passivation optimization [391], [392] and field-plate introduction [393], [394] were key to minimize it, thanks to a combination of surface defect density reduction (passivation optimization) and gate-drain electric field mitigation (field plates).

Another possible charging path for surface traps is through trapping of 2DEG electrons gaining sufficient energy to overcome the barrier due to the AlGaN/GaN conduction-band offset [159], [395]–[398] [mechanism Su2 in Table 8]. This process requires the presence of channel hot electrons (CHE) and therefore an accumulated device operation under *semi-on* or *power-state* conditions (i.e. simultaneously high V_{GS} or I_D and V_{DS}), like in RF power or hard-switching conditions.

As far as the physical nature of surface traps is concerned, dominant discrete levels [55] as well as distributed interface states [56], [399]–[401] or border traps [402] have been reported.

Finally, since these traps are located within the drain access region, their primary, detrimental effect is an increase in the drain access resistance and therefore a reduction in the transconductance peak.

8.4 Barrier traps

In GaN HEMTs barrier traps located under the gate can capture electrons injected by the gate contact following off-state biasing and slowly emit them as the device is turned to on-state conditions [mechanism Ba1 in Table 8]. Under power-state conditions, hot electrons from the 2DEG can instead be trapped by barrier traps located in the G-D access region [396] [mechanism Ba2 in Table 8]. The consequence is either a positive shift in V_T or an increase in the drain access resistance, depending on whether traps are located under the gate or in the G-D access region.

During drain voltage sweeps, donor-like barrier traps can be ionized by field-enhanced electron emission [403], [404] [mechanism Ba3 in Table 8], in this case inducing an increase in the output conductance sometimes termed “kink effect” (see Section 8.7.4).

In normally-off p-GaN HEMTs, hole trapping can take place at the p-GaN/AlGaN interface under positive gate bias [87] [mechanism Ba4 in Table 8].

8.5 Buffer traps

Buffer traps are probably the major source of trapping effects in present-days GaN transistors, following the already mentioned advancements in surface passivation and the introduction of field plates, which resulted in the effective minimization of surface trapping effects.

Buffer-trap effects have been associated with several different trapping mechanisms. The most straightforward charging path is through electrons originating, under off-state bias, from the source and/or gate contacts and forming the source-drain [405]–[407] [mechanism Bu1 in Table 8] and the gate-drain [307] [mechanism Bu2 in Table 8] leakage currents, respectively. At very large drain voltages (always under off-state conditions), the substrate leakage current come also into play, contributing to electron trapping into buffer traps mainly within the G-D access region under the drain contact [408] [mechanism Bu3 in Table 8]. Under semi-on and power-state bias conditions, on the other hand, energetic 2DEG electrons can be injected deeply into the buffer and get thereby trapped, mainly in the G-D access region [398], [409] [mechanism Bu4 in Table 8].

Other buffer trapping mechanisms that have been invoked include the capture of valence-band electrons through Zener processes involving traps in the buffer region under the gate edges [410] [mechanism Bu5 in Table 1], and at the barrier/buffer interface [411] [mechanism Bu6 in Table 8]. Moreover, trap impact ionization by channel electrons has been proposed as a mechanism that can discharge traps at the barrier/buffer interface as the drain bias is increased above some critical voltage and resulting in the so-called “kink effect” in the device output characteristics [319] [mechanism Bu7 in Table 8].

With relevance to power transistors with C-doped buffer, peculiar trapping effects taking place in the weakly p-type buffer characterizing these devices have been explained by the so-called “leaky-

dielectric" model [412] to describe charge injection into the buffer region [mechanism Bu8 in Table 8] or by hole redistribution within the buffer itself [413] [mechanism Bu9 in Table 8].

As far as the physical origin of buffer traps is concerned, either GaN intrinsic defects [407], [414], [415] or intentional impurities have been correlated with the observed trapping effects. The latter are acceptor-like traps purposely introduced to suppress the n-type conductivity of GaN. Fe and C are the two species that are more commonly adopted.

Fe is generally adopted for RF transistors [407], [416]. The dominant deep level introduced in the GaN bandgap by Fe doping is generally assumed to be energetically located at 0.5-0.6 eV from E_C [334], [369]. As a result, the Fe-related level behaves as an acceptor-like electron trap.

C is typically used for power devices [67] and can be incorporated (i) by tuning growth parameters to control the decomposition rate of TMGa and the incorporation of C from methyl group (autodoping [100], [417]), or (ii) by adding a C precursor (propane, methane, ethylene) [418] to CVD gas mixture (extrinsic doping). Early DLTS/DLOS measurements [419] and correlation with DFT calculations based on LDA approximation [420] suggested two deep levels related to C doping being the C_N (acceptor) and C_{Ga} (donor) centers, respectively located at E_V+0.14 eV (or equivalently E_C-3.28 eV) and E_C-0.11 eV. More accurate and recent hybrid-functional DFT calculations yielded C_N at E_V+0.9 eV and C_{Ga} above E_C, along with other C-related centers inside the bandgap like interstitial C_I center at E_C-0.4 eV (acceptor) and the C_{Ga}-V_N complex at E_C-0.1 eV (donor [385], [421], [422]). While there is nowadays a rather general consensus that trapping effects in C-doped GaN transistors are mainly related to the dominant C_N traps, many simulation-based works [112], [413], [423]–[428] suggest that some degree of auto-compensation between these acceptors and C-related donor traps must take place, reducing the effective acceptor density below the level of the introduced C concentration (especially in case of extrinsic C doping). On the other hand, higher donor concentration in GaN:C compared with donor density in undoped samples has been confirmed also experimentally [429]. The (E_V+0.9 eV) level is anyway able to induce the compensation of the buffer region, for suitable concentrations. As mentioned above, this may lead to peculiar trapping effects, which are still subject of investigation in the literature [424], [430]–[433].

Regardless of whether they are related to intrinsic defects or intentional impurities, buffer traps are essential to compensate the unintentional n-type conductivity (related to V_N, Si, O) of nitrides,

therefore allowing for an abrupt channel pinch-off, reducing the source-drain leakage current and increasing the off-state breakdown voltage. Owing to this, buffer optimization requires a trade-off between trapping effects and breakdown voltage. In the case of doped buffers, this is typically achieved by switching off the impurity flow during growth at a designed distance from the channel at the barrier/buffer interface [406], [434].

Similarly to barrier traps, buffer electron traps can lead to a positive shift in V_T or an increase in the drain access resistance and R_{ON} depending on whether involved traps are located under the gate or in the G-D access region. Positive charge can also be accumulated in the buffer, leading to a decrease in R_{ON}, under specific conditions [412], [435].

8.6 Gate-dielectric traps

In transistors with an insulated-gate structure, like AlGaN/GaN MIS-HEMTs, also the gate oxide bulk and its interface with the underlying semiconducting region can act as trapping sites.

As far as bulk oxide traps are concerned, the main charging/discharging path is through the gate electrode [mechanism Ox1 in Table 8], which can inject electrons into the gate dielectric at large and negative V_{GS} [436], [437] and remove trapped electrons out of the device under positive V_{GS} [438].

For interface and border traps, the main charging path is through electron injection from the device channel at the AlGaN/GaN interface (in MIS-HEMTs) or the GaN surface (in MOSFETs) [mechanism Ox2 in Table 8. Classification of major trapping mechanisms in terms of trap location, charging/discharging path and type of involved mobile carriers. Table 8], that can be triggered at positive V_{GS} (forward-gate bias [313]). These traps can instead emit electrons at negative V_{GS} [317].

Another reported mechanism, specific to devices with a C-doped buffer, consists of hole capture into interface traps, where holes are provided by C-related acceptors in the buffer and not necessarily by a high-field electron-hole generation mechanism [mechanism Ox3 in Table 1 [428]].

Both bulk and interface dielectric traps affect the device performance through V_T, by inducing instabilities on this crucial parameter [439]. These effects will be described in more detail in Section 8.7.3.

8.7 Trapping effects

In this section the major charge trapping effects observed in GaN transistors are reviewed and associated to the mechanism(s) put into evidence in the previous section. The correlation between trapping effects and related mechanisms is summarized in Table 9.

Table 9. Major trapping effects in GaN transistors with associated, responsible mechanism(s) (labelled according to Table 1).

Trapping effect	**Trapping mechanism(s)**
RF current collapse	Su1, Su2, Ba1, Ba2, Bu1, Bu2, Bu4
Dynamic R_{ON}	Su1, Su2, Ba1, Ba2, Bu1, Bu2, Bu3, Bu4, Bu5, Bu6, Bu8, Bu9
Negative-gate-bias V_T instabilities	Ox1, Ox2, Ox3, Bu5, Bu8
Positive-gate-bias V_T instabilities	Ox1, Ox2
Kink effect	Ba3, Bu7, Bu8

8.7.1 RF current collapse

Considering RF amplification, the most harmful trap-related effect is the so-called *RF current collapse* [303], [304] resulting in a reduction in the maximum drain current and simultaneous increase in the minimum drain-source voltage explorable by the operating point during the RF sweep. The increase in the minimum drain-source voltage is also referred as *knee-voltage walk-out* [303], [440]. The overall result is a compression in the RF output power and a degradation of the power added efficiency compared to the theoretical limits achievable by the given transistor that can be calculated from the DC output characteristics.

Responsible mechanisms are related to electron trapping taking place under off-state or semi-on bias. Channel conductivity is weakened by this and can not promptly be restored as the dynamic operating point moves to ON-state. Electrons can be provided by the gate through tunneling

injection at large drain-gate voltage, by the source via source-drain leakage current due to the large drain-source voltage, or by the 2DEG channel under semi-on conditions. Gate electrons can reach surface, barrier, as well as buffer traps, whereas source electrons can only get trapped into buffer traps. Channel hot electrons can be trapped by buffer, barrier or surface traps. Either V_T or the drain access resistance or both parameters can in principle be increased, depending on whether electron trapping takes place under the gate, in the gate-drain access region or both. A major impact is typically associated to electron trapping within the gate-drain access region. Optimization of surface passivation [391], [392] and introduction of field plates [393], [394] have comparatively decreased the role of surface and barrier traps as promoters of the RF current collapse, thanks to the mitigation of the electric field at the drain-end edge of the gate, leaving buffer electron trapping as the major responsible mechanisms, especially in technologies where compensating impurities (like Fe) are used in the buffer to increase the breakdown voltage [407], [441].

These effects are illustrated in Figure 70, showing the dispersion of the pulsed output characteristics from a Fe-doped AlGaN/GaN HEMT.

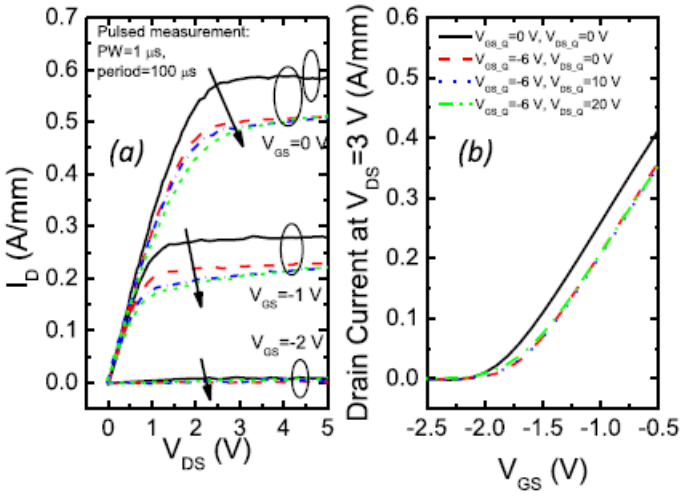


Figure 70. (a) Pulsed ID–VD curves measured starting from different quiescent bias points, in the OFF-state, on a sample of wafer D (highest Fe content). (b) Pulsed ID–VG curves measured starting from different quiescent bias points, in the OFF-state [same sample as in (a)] [111].

8.7.2 Dynamic R_{ON} increase

When GaN transistors are used in power switching converters, the most detrimental trap-related effect is the increase in the dynamic R_{ON} compared to its DC value, resulting in an undesirable increment in power losses [310], [442].

Possible underlying mechanisms include all the electron trapping processes already described for RF current collapse, taking also place during the off-state phase of the switch-mode operation or during hard switching when large V_{DS} and I_D can temporarily co-exist. Channel conductivity, that is reduced by this increase in negative trapped charge, can not be restored promptly as the device is driven to on-state, thus leading to the dynamic R_{ON} increase.

In addition to these mechanisms, there are additional trapping processes leading to dynamic R_{ON} increase that are specific to power transistors. These include the electron trapping into buffer traps within the gate-drain access region induced by the substrate leakage current [310], [443]. The latter becomes comparable with gate and source leakage currents only at the very high drain voltages that are typically achieved in GaN power transistors only.

Carbon doping is commonly adopted in the buffer region of power transistors to increase the blocking voltage. When this is the case, the carbon doped buffer can be the site for peculiar trapping mechanisms, that are mainly governed by the C_N acceptor state at E_V+0.9 eV [100], [415], [419]. Holes are emitted by these traps within the gate-drain access region when the device is in the OFF state, leading to an increase in the density of negatively-ionized C_N acceptors, and therefore to a dynamic increase in the channel conductivity and R_{ON} [413], [424]. It has been shown that both R_{ON} increasing transients under off-state bias stress and subsequent R_{ON} recovery transients may be thermally activated with the same activation energy of 0.9 eV [444], [445]. This has been explained as the result of a thermally activated electron capture process [310], [443] or, alternatively, by means of a hole redistribution model [413], [446]. Recently, it was demonstrated that discharging and charging events in carbon-doped GaN layers (GaN:C) can be governed by transport properties of GaN:C (details can be found in [433]).

Recent works have shown that the dynamic R_{ON} can exhibit a non-monotonic dependence on the off-state drain voltage [447]–[449], recovering to smaller values after reaching a maximum. This behavior has been explained by means of a “leaky dielectric” buffer model: at high off-state bias, band-to-band tunneling through the uid channel layer may promote the generation of holes, that

can be pushed to the bottom of the buffer, partially compensating the effect of the negatively-ionized carbon acceptors [450]. A similar behavior was also attributed to holes generated by impact-ionization, discharging the ionized C_N traps and thus attenuating the dynamic R_{ON} increase mechanism [427].

Some of the above effects are illustrated by Figure 71, showing the dynamic R_{ON} variation measured on GaN-based power HEMTs and a schematic representation of the related processes [451].

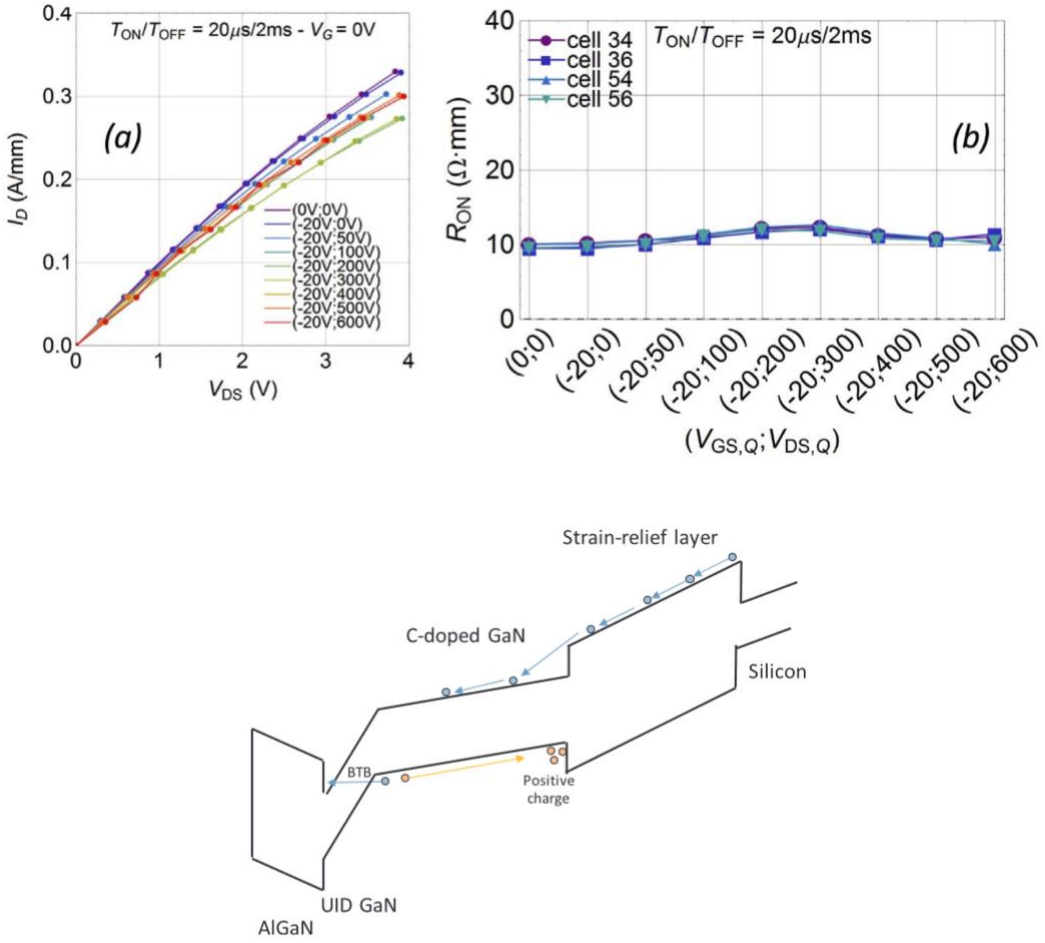


Figure *71*. (a) Pulsed-IV curves measured at room temperature on a GaN-based power HEMT. (b) Dependence of on-resistance on the applied trapping bias (the four lines refer to four devices sitting on different locations on the wafer) [451]. Schematic representation of the mechanisms responsible for non-monotonic dynamic-Ron as a function of trapping voltage

8.7.3 Threshold-voltage instabilities in isolated-gate and p-GaN transistors

To suppress the gate current, which is a requirement especially for power transistors, isolated-gate AlGaN/GaN MIS-HEMTs have been proposed and developed [67], [452]. These include both unrecessed or partially-recessed MIS-HEMTs, in which the gate dielectric is deposited onto the AlGaN barrier, and fully-recessed MIS-HEMTs, where the AlGaN barrier is completely removed under the gate region so that the gate dielectric is formed onto the GaN buffer region (while the 2DEG at the AlGaN/GaN interface survives in the two access regions).

In these transistor types, also the gate dielectric bulk and its interface with the underlying semiconductor can act as trapping sites. The most serious effects for device performance are the V_T instabilities adding up to other trapping effects like dynamic R_{ON}. These instabilities are typically analyzed by applying either negative gate bias (NGB) or positive gate bias (PGB) stress voltages with zero drain-source voltage, with the aim of isolating V_T effects from the drain access-resistance ones [453].

For normally-on devices with negative threshold voltages of several volts, V_T stability under NGB is, in particular, a critical aspect that needs careful evaluation during technology development. In normally-off devices, V_T stability under PGB is instead of major concern. In the latter devices, assessing the V_T stability under NGB can be important as well, since a negative gate voltage can be applied to switch off the transistor, in order to prevent false turn-on and ensure safe operation against voltage spikes on the gate [454]. Moreover, NGB measurements are in any case a proxy for the off state operation, as similar, large values of drain-gate voltage can be achieved with both biasing conditions.

As far as NGB effects are concerned, V_T shifts of either negative (i.e. V_T becoming more negative [317], [318], [455]) or positive (i.e. V_T becoming more negative [436], [454], [456]) sign, as well as of both signs depending [410], [437] on applied bias, temperature, and stress time have been reported. The trapping mechanisms that have been held responsible for the negative V_T shifts are: (a) electron emission from interface and/or border traps [317], [318], [437]; (b) decrease in the negatively ionized C-related acceptors in the buffer region under the gate [455], (c) hole capture into interface traps, where holes are provided by C-related acceptors and not necessarily by a high-field electron-hole generation mechanism [428]. Positive V_T shifts have instead been attributed to: (d) electron injection from the gate and consequent electron capture into gate dielectric traps [436],

[437]; (e) hole-induced defect generation in the gate insulator [454], [456], [457] or interface state generation [410]; (f) Zener electron trapping into GaN traps localized under the gate edges [410]; (g) the recombination of holes provided by the C doping (and attracted to the device surface) with electrons injected from the gate [428].

Also PGB experiments can produce V_T instabilities of both signs. More commonly, positive V_T shifts are observed [318], [458], [459]. These are attributed to channel electron injection into interface or border traps [313], [458], [459]. Negative V_T shifts under PGB have instead been explained as the result of electron removal from dielectric traps through the gate.

V_T stability of devices with p-GaN gate after PGB stress is of a great concern because of the normally-off operation [460]. By focusing on trap-related instabilities, electron injection from the 2DEG into pre-existing defects in the AlGaN barrier (also occurring in HEMT and MIS-HEMT structures) has been reported to cause V_T to shift positively. On the other hand, negative V_T shifts have been attributed to trapping of holes at the p-GaN/AlGaN interface.

Some of the above effects are illustrated by Figure 72, showing V_T instabilities effects induced by NGB (up [317]) and PGB (bottom [461]).

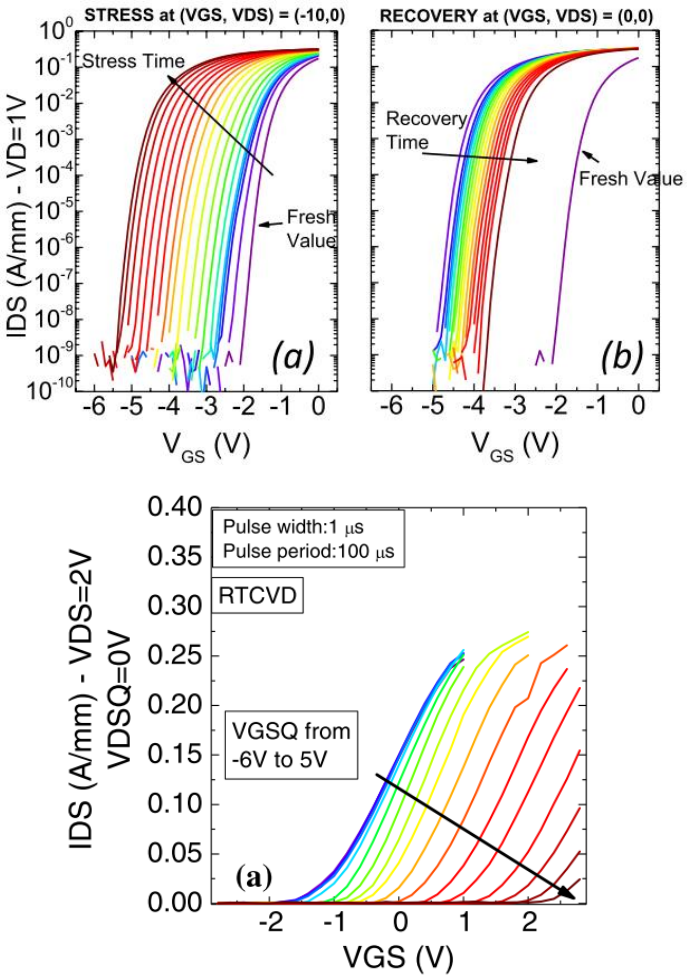


Figure 72. V_T instabilities effects induced by NGB (up [317]) and PGB (bottom [461]).

8.7.4 "Kink" effect

The "kink" effect is an operational instability emerging during a V_{DS} sweep, by which the drain current in the saturation region is initially compressed and then increases, over a relatively narrow voltage range, to a higher value [320], [404], [462]. This behavior is detrimental especially in transistors for RF amplifiers because it can result in transconductance compression and output conductance increase [319], [463], [464].

Most recent works on this issue proposed that the kink effect can be caused by (i) impact ionization of traps in the channel or the barrier, with consequent emission of electrons [319], [465], [466] (ii) trapping of holes generated by trap-assisted tunneling into C-related traps [432], [467], (iii) field-

enhanced ionization of AlGaN barrier traps under the gate and near the GaN/AlGaN interface [404].

8.8 Traps characterization techniques

Within this section an overview of different techniques adopted for the characterization of trapping phenomena will be provided. Pulsed IV characterization will initially be introduced. Even if it does not provide a quantitative characterization of traps activation energies, it is a widely used tool to highlight the presence of trapping phenomena. Deep-Level Transient Spectroscopy and Deep-Level Optical Spectroscopy will then be discussed. Their combination provides the characterization of trap levels located within the full gap of GaN. Nevertheless, specific test structures are needed, making them difficult to apply directly on actual transistors. Characterization techniques based on the monitoring of device drain current evolution will then be introduced and the different methods will be commented. Monitoring of drain current for emission process characterization supposes that the emission process takes place when the device is biased in on-state. If traps experience said emission when the device is biased in off-state, it would be thus impossible to properly characterize them. On-the-fly characterization overcome this issue, allowing for the characterization of traps experiencing charge emission during off-state operation. Interface states can be characterized by specific measurement based on capacitance-voltage (C-V) and conductance-voltage (G-V). Finally, photoluminescence (PL) measurement technique will be briefly described.

8.8.1 Pulsed IV

As previously introduced, trap characterization can be carried out by means of several techniques. The most important measurement adopted to quickly identify the presence of trapping phenomena is pulsed-IV (PIV) characterization. The concept of this measurement is rather simple. The device is hold into a quiescent bias point (QBP), also called baseline, with its source terminal grounded. Synchronous and short voltage pulses, typically in the 100 ns-10 us range with a duty-cycle in the 0.1 %-1 % range, are applied to the gate and drain terminals to evaluate the device I-V characteristics. The basic idea is that traps are not able to reach their equilibrium condition during the short duration of the pulses. Therefore, the measurement yields the I-V characteristics of the device obtained with the traps filled at the condition set by the quiescent bias point. Since trap

filling condition strongly depend on the applied voltages, comparing pulsed I-V obtained at different quiescent bias points quickly allows to evaluate the presence and in some way the amount of trapping phenomena. A typical set of pulsed I-V is performed by comparing at least three or more different quiescent bias points [390], [468], [469]: (i) the V_{GS}=0 V,V_{DS}=0 V QBP, which sets also the reference of the "fresh" device conditions; (ii) gate-lag effect is then evaluated with a QBP where V_{GS} is held below the device threshold voltage and V_{DS}=0 V; (iii) drain-lag effect is finally evaluated by a QBP with the device in off-state conditions and large V_{DS}. Obviously, many other combinations can be considered by the three reported are the most used for device characterization. PIV characterization quickly offers an overview on device operation and a qualitative evaluation of the reduced device performance due to trapping phenomena. Some information on trap spatial localization might also be obtained by comparing results from different QBPs. If the device experiences a threshold voltage shift, trapping phenomena are likely to be confined within the device buffer layer and/or the barrier or insulator layer under the gate terminal [445]. On the other hand, a decrease in its transconductance might be related to an increase in access region resistance which might be induced by surface, barrier, or buffer traps [390].

8.8.2 DLTS/DLOS

Trap investigation has been an important topic since the beginning of the semiconductor device development. Capacitance transients are used to obtain information about an impurity level in the depletion region of a Schottky barrier or p-n junction. The measurement consists in observing the capacitance transient associated with the return to thermal equilibrium of the occupation of the level, following an initial nonequilibrium condition [470], [471] [Williams_JAP_1966, Sah_SolidState_1970]. One can thus measure the time constant of this capacitance transient as a function of temperature and obtain the activation energy for the level. An alternative method named deep-level transient spectroscopy (DLTS) was introduced in [472] (see Figure 73). DLTS is still based on capacitance transients but it allows a faster characterization. The essential feature of DLTS is the ability to set an emission rate window such that the measurement apparatus only responds when it sees a transient with a rate within this window. Thus, if the emission rate of a trap is varied by varying the sample temperature, the instrument will show a response peak at the temperature where the trap emission rate is within the window. These emission rates are thermally activated and by the principle of detailed balance can be given as:

$$e_1 = (\sigma_1 v_1 N_{D1}/g_1)\, exp(-\Delta E/kT)$$

where σ_1 is the minority-carrier capture cross section, v_1 is the mean thermal velocity of minority carriers, $N_{D1}$is the effective density of states in the minority-carrier band, $g_1$is the degeneracy of the trap level and ΔE is the energy separation between the trap level and the minority-carrier band.

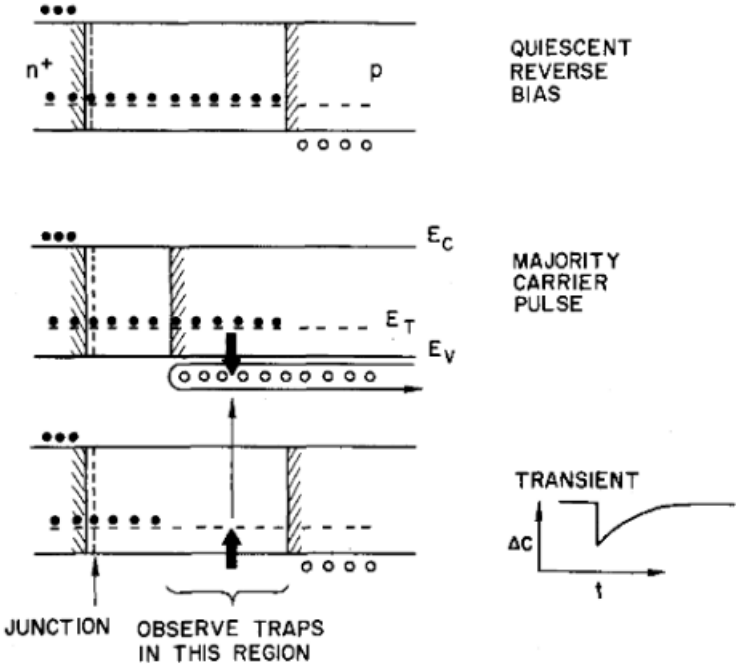


Figure 73: Majority-carrier pulse sequence which is used to produce a capacitance transient for a majority-carrier trap. The energy-vs-distance diagrams (with band bending omitted for simplicity) show the p+n junction depletion region (edges denoted by shaded lines) as well as the capture and emission processes and trap occupation before, during, and after a majority-carrier pulse [472]

While DLTS is still one of the most used techniques, it also shows some limitations. Impurity levels with a large activation energy result in a low emission rate, leading to transients with large, time constants whose evaluation could be masked by slow drifts [473]. A novel methodology was thus introduced in [474] with the name of deep-level optical spectroscopy (DLOS). DLOS is based on photostimulated capacitance transients measurements after electrical, thermal, or optical excitation of the sample. By increasing the energy of the photons impinging on the device, the optical cross section for the transition between the deep level and the conduction and valence band can be extracted. DLOS can provide information not only about the ionization energies of the levels, but also about the electron-phonon interaction and temperature dependence of the levels, i.e., about their relations with each band [474].

Due to its wide band-gap, the characterization of GaN material has typically carried out by combining both DLTS and DLOS measurements. DLTS is adopted for evaluating levels with activation energies below approximately 1 eV, while deeper levels are typically investigated by means of DLOS [419], [475], [476]. The combination of the two measurement techniques allows a full investigation of the trap level within the whole GaN band-gap.

8.8.3 Current transients

DLTS and DLOS techniques are typically applied to large area diodes, in order to have a well measurable capacitance value. When three terminal devices are tested, these techniques suffer from the low device capacitance (typically in the pF range), making them less appealing for trap characterization. Furthermore, the electric field distribution in actual transistors in normal bias conditions can be significantly different from that in large area diodes. Consequently, while DLTS and DLOS can definitely provide useful information on crystal impurities, they might not be able to provide a clear indication on the effects of said impurities on actual device dynamic operation. Trapping sensing in DLTS and DLOS is provided by evaluating capacitance transients induced by depletion region variations linked to the emission of trapped charge. On an actual device, the effect of charge emission can be monitored by evaluating the drain current evolution as the emission process takes place. In fact, an emission of trapped electrons will lead to a decrease in the fixed negative charge within the device, leading to an increase in its 2DEG concentration [477], and, therefore, an increase in its drain current. Drain current transients (DCTs) are typically evaluated by monitoring the device current in on-state, after applying for a certain time a different bias condition typically in off-state condition (corresponding to the application of a V_{GS} below device V_{TH} and large V_{DS}). It should be stressed though that this is only one of the possible biasing conditions. Generally speaking, any variation in the device bias point can in principle lead to a variation in traps occupancy and thus cause during the emission process the observation of a DCTs. On the practical side, traps characterization based on device current variations can be performed by means of drain current DLTS (ID-DLTS) [478], [479], constant drain-current DLTS/DLOS (CID-DLTS/DLOS) [373], [480] or multiple DCTs measurements carried out at different temperatures [390], [481]. Pulsed drain-current methodologies have also been proposed, to characterize the de-trapping processes in absence of applied bias [482].

8.8.3.1 ID-DLTS

ID-DLTS [478], [479] is typically performed by applying a constant V_{DS} voltage, to have a readable drain current. The gate terminal is periodically pulsed between a filling condition and a sensing condition (see Figure 74). The sensing condition is typically slightly above device threshold voltage, with the aim of obtaining a readable current level while at the same time reducing device self-heating effects. Monitoring the current transient over a certain temperature range allows to obtain a plot of the DLTS signal vs. temperature. The detection of peaks in DLTS spectra corresponds to the presence of a trap level, whose activation energy can be extracted by means of an Arrhenius plot [478], [479].

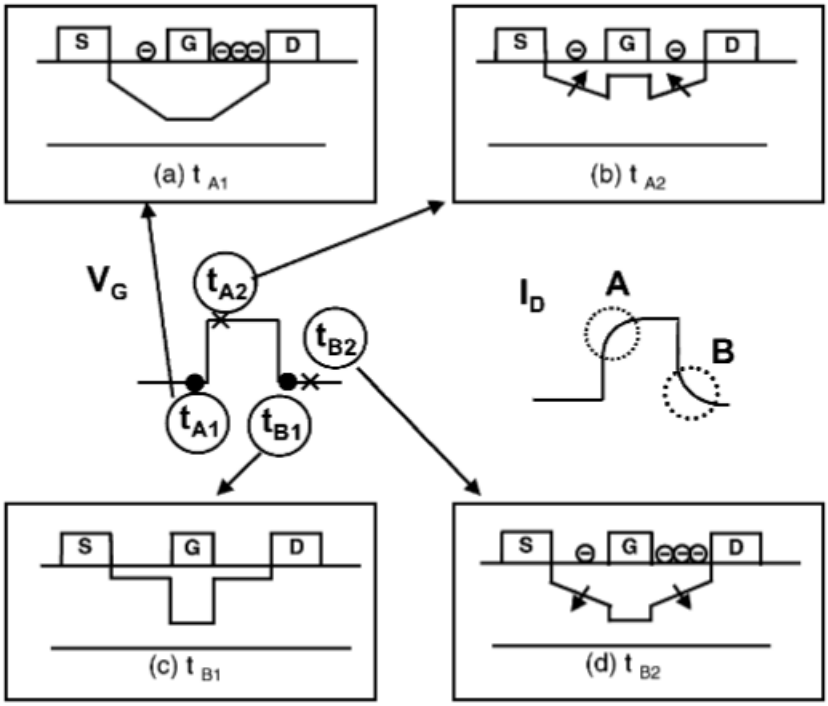


Figure 74: Schematic illustration of response of the depletion layers: (a)–(d)represent the response of the depletion layer at the timing of t_{A1}, t_{A2}, t_{B1}, and t_{B2} on the gate bias pulse, respectively [479]

8.8.3.2 CID-DLTS/DLOS

The CID-DLTS/DLOS [373], [480] technique is based on a dynamic control of either the device gate or drain voltages with the aim of maintaining a fixed drain current in response to a thermally and optically stimulated trap emission. For a gate-controlled method, a constant and large enough

V_{DS} is applied to the device to have it working in its saturation region. The gate terminal is pulsed to the on-state to induce trap filling, and then lowered near pinch-off conditions. The dynamic control on V_{GS} for maintaining a constant I_{DS} will thus give rise to a V_{GS} transient, that will thus be recorded. This condition is sensitive for trap levels located beneath the gate contact and affecting device V_{TH}. For a drain-controlled method the device is biased in its linear region with low V_{DS} and a V_{GS} large enough to have a negligible forward transconductance g_m. Filling condition is here obtained by biasing the device in pinch-off conditions with large V_{DS}. The subsequent change in device resistance $\Delta R_D=\Delta V_{DS}/I_{DS}$ is then recorded. This condition is particularly sensitive to traps located in the device access regions. The detection of peaks in either the temperature or optical spectra corresponds to the presence of a trap level, whose activation energy can be extracted by means of an Arrhenius plot [373], [480].

8.8.3.3 Multiple DCTs

Multiple DCTs measurements provide an important advantage in reducing the number of measurements to be carried out, since DCTs are typically evaluated at some (5-10) temperature levels. On one hand this technique is rather simple and can easily applied to actual transistors. Voltage pulse generators or a load-line drain biasing network are required to switch the device between a filling and a sensing condition [483] (see Figure 75). Multiple DCTs however can yield results that might be strongly dependent from the device bias conditions used, and the method adopted for the analysis of DCTs required for Arrhenius plot extraction [481]. Additional comments on bias conditions and the DCTs analysis will be provided in the following subsections.

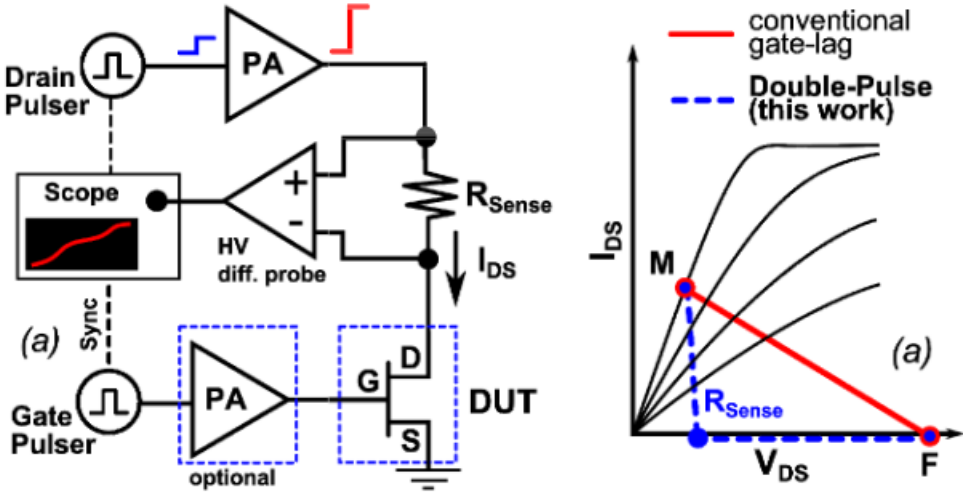


Figure 75: (left) schematic representation of a system to switch the device between a filling and a sensing condition and (right) switching trajectories for device analysis [483]

8.8.3.4 Bias conditions

DCTs can be recorded with a sensing condition lying in the linear [368], [484], [485] or in the saturation region [390], [486], [487]. Significantly different results might be obtained when comparing results obtained in the linear and saturation region [481]. Nevertheless, an accurate evaluation of the different DCTs response might be useful for spatially localize traps as suggested by [480]: a sensing condition in the linear region of the device with reasonably high V_{GS} should highlight the effect of traps located within the device access regions. On the other hand, sensing in saturation near the pinch-off voltage, i.e. at low current level so that the effect of device access region can be minimized, should be more sensitive to the effect of traps located beneath the gate contact. Other phenomena that might significantly affect the results of DCTs analysis could be the presence of mechanisms affecting the DCTs time constants, i.e. device self-heating and electric field enhanced emission mechanisms. Self-heating by raising the local device temperatures enhances carrier emission process leading thus to an erroneous evaluation of the emission process. In other words, the de-trapping appears faster than it should be at the applied base-plate temperature [488]. Similarly field enhanced emission mechanisms such as Poole-Frenkel phenomena [489] will lead to an error like that introduced by device self-heating. Therefore, DCTs results needs to be carefully reviewed to avoid an erroneous estimation of the activation energy associated with the trap level causing the observed DCTs. Based on the comments and issues reported in this section, the authors would like to suggest that, to have an accurate estimation of the trap activation energy, V_{DS} voltages applied during the sensing condition should be as low as possible, in order to reduce self-heating and electric field related enhanced emission. The use of pulsed-drain current transient (P-DCT) methodologies can also be effective to this aim, since the device is kept at zero bias during recovery, and short voltage pulses are used to sense the on-resistance during the de-trapping phase [482].

8.8.3.5 Analysis of DCTs for time constant extraction

The extraction of time constants at different temperatures is the process leading to the construction of the Arrhenius plot from which the trap activation energy is obtained. Several techniques can be

used to this aim. A *multi-exponential* approach [484] can be adopted by least-square fitting the experimental data with the sum of several exponential functions, typically in the amount of few hundreds, with different amplitudes and time constants as described in the following equation

$$I_{fitted} = \sum_{i=1}^{n} a_i exp(-t/\tau_i) + I_\infty$$

By plotting the amplitude coefficients a_i vs the time constants τ_i, the traps associated time constants can be inferred by looking at the peaks of the spectra obtained, see for example Figure 76.

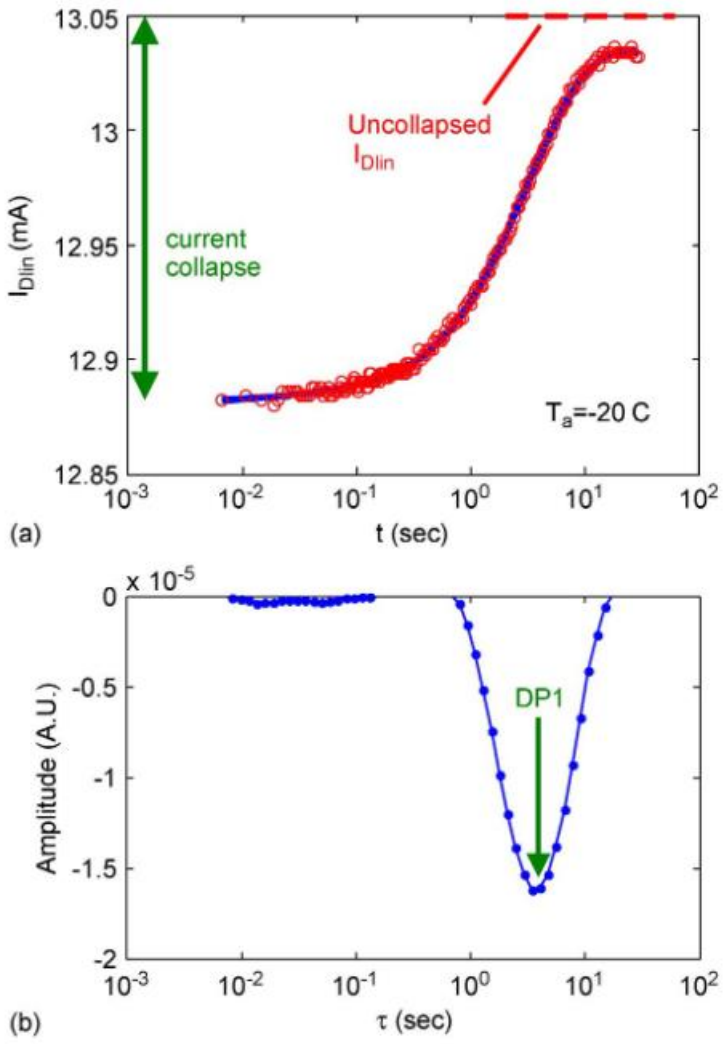


Figure 76: (a) Recovery transient of I_{Dlin} and (b) corresponding time-constant spectrum at−20◦C after applying a 1 s V_{DS}=0 and V_{GS}=−10 V trapping pulses [484]

A different approach relies on the so called stretched exponential fitting [303], [390]. This method least-square fits the experimental data by means of stretched exponential functions, one for each of the low-pass or high-pass transitions observed in DCTs according to the equation:

$$I_{fitted} = \sum_{i=1}^{n} a_i exp(-t/\tau_i)^{\beta_i} + I_\infty$$

where n here is corresponds to the number of transitions observed in DCTs which typically ranges between 1 and 3. Note that each exponential function corresponds to potentially a different charge emission/capture process. The Arrhenius plot of each of the i-th process is then built using the τ_i values obtained at different temperatures.

An alternative approach widely used is the analysis of the derivative of the DCT by the logarithm of time [368], [485]. Peaks in the derived spectra are used to locate the characteristic time constants of different traps and used to derive the emission energies.

8.8.4 On-the-fly characterization

The trap characterization methods based on the sensing of device drain current assume that the emission process takes place when the device is biased in on-state. Only in this way it is possible to observe current variations linked to charge emission processes. If said emission process would take place instead in off-state conditions, it would be impossible to perform a proper characterization. An example of a trap level behaving in such manner as been proposed in [424], where it has been suggested that carbon-doping might introduce a hole-trap whose emission process takes place during the biasing in off-state condition. The analysis of such a trap level can be performed then by means of the so called on-the-fly characterization [311], [490]. Basically, the device is biased in a condition promoting the charge emission process and it is periodically turned-on to sample within a short time interval the drain current evolution. This allows to obtain a drain current evolution like that of DCTs and consequently extract traps activation energies using the methods previously described.

8.8.5 Interface trap characterization by means of C-V and G-V measurements

Surface states at metal-insulator-semiconductor interfaces are typically characterized by means of capacitance-voltage (C-V) and conductance-voltage (G-V). C-V measurement were proposed as a

tool for evaluating surface-states density and energy distribution [491], [492]. The combination of both C-V and G-V measurements [493] can also be used to calculate the interface state density NSS, whose most accurate calculation can be obtained by means of the Nicollian-Goetzberger theory [494]. Said method presents some issue related to the need of an extensive data acquisition. An alternative method based on single-frequency approximation can also be used [495] which allows to estimate the NSS from the equation:

$$N_{ss} = \frac{2}{q\,A}\frac{G_{m,max}/\omega}{\left(\frac{G_{m,max}}{\omega\,C_{ox}}\right)^2 + \left(1 - \frac{C_m}{C_{ox}}\right)^2}$$

where q is the electronic charge, A is the area of the capacitor, $G_{m,max}$ is the peak value of conductance, $\omega = 2\pi f$ where f is the measurement frequency, C_{ox} is the capacitance in accumulation region and C_m is the capacitance corresponding to $G_{m,max}$. This method has been successfully applied to the characterization of GaN based devices [496], [497], in which the G-V measurement [494] relies upon the assumption that energy losses and leakage currents in dielectrics are negligibly small [498]. To this end, quasi-static capacitance–voltage (QSCV) measurement [499] is rarely used in AlGaN/GaN HEMTs, because of the high leakage current associated with the Schottky gate [312]. To overcome the oxide leakage problem in GaN-based structures, high frequency C-V measurements (HFCV) are typically adopted [500]–[502]. Nevertheless, standard HFCV measurements performed at room temperature (RT) may not be adequate to characterize wide bandgap GaN and AlGaN interfaces [503] because of the extremely long time constants of deep interface traps. In fact, said deep levels are frozen at RT, thus requiring elevated temperature C-V measurement to accurately characterize the interfaces quality [496]. Recent papers pointed out that the conductance method may show limitations on AlGaN/GaN metal-insulator-semiconductor capacitors, and discussed the related implications [504] Other papers [505] proposed methodologies to analyze the interface state density of dielectric/GaN MIS devices. The wide bandgap of GaN limits hole generation at room temperature, allowing measurements in deep depletion. By a photoassisted high-frequency capacitance-voltage characterization, it is possible to measure the total interface state density throughout the bandgap, by using an above bandgap light source.

8.8.6 Photoluminescence (PL)

Photoluminescence spectroscopy (PL) is a commonly used technique for studying optical properties, measuring band-gap energy, determining phonon modes and identify energy levels due to impurities or defects [506], [507]. During PL measurements, a light with fixed energy above the energy-gap of the material being characterized is directed on the sample under test. Luminescence is then detected at different wavelengths and peaks can be observed in correspondence of allowed (radiative) transitions within the energy-gap of the semiconductor. One of the most famous result obtained by PL on GaN layer has been the so called yellow-band YL [508], [509]. PL is a relatively fast, contactless, and nondestructive technique and can provide very high spatial resolution. It thus offers the possibility to evaluate material properties from samples of various sizes (from microns to centimeters) without having to undergo a complex sample preparation [510].

9 Degradation processes in GaN devices

The possible device types and structures based on gallium nitride have a huge variety, as well as many applications, and therefore a high number of possible degradation and failure modes may take place. In this section, we will review the most relevant ones, with reference to lateral and vertical devices. The discussion will be organized based on the operating conditions that lead to the detected effects. In the first part, the ON-state and OFF-state bias conditions will be discussed, since they are the most relevant ones for a power device. Then, the transition between the two phases will be considered, leading to additional degradation in the SEMI-ON-state. Finally, reliability in realistic environment will be analyzed, including the study of electrostatic discharge (ESD) and electrical overstress (EOS) events, and radiation hardness.

9.1 ON-state

The on-state bias condition can be heavily stressful for several reasons. A large gate overdrive is usually desired, in order to increase the channel carrier density and, therefore, the maximum current levels, but this leads to a high voltage drop and electric field across the gate stack. Moreover, although the desired voltage drop on the device should be zero in on-state, to ensure maximum power transfer and no power loss, real devices may have voltage drops in the range of hundreds of millivolts. At the high operating current levels, this may cause a significant power dissipation and self-heating, that can be detrimental for long-term operation.

9.1.1 Extrinsic degradation: the role of dielectrics

A high gate overdrive can be dangerous for insulated gate devices, where the electric field in the gate dielectric has to be engineered in order not to exceed the breakdown value.[511]

Even when this design rule is correctly achieved, the insulator can still show some degradation in its performance over time, due to a physical process called time-dependent dielectric breakdown (TDDB) and usually linked to defect percolation.[512] As shown in Figure 77 (a), before stress some defects are already present in the bulk of the oxide. When the device is stressed (Figure 77 (b)), additional defects can be created by the high electric field or by the current flowing through the insulator. The spatial distribution of these defects is, in principle, random, but the presence of a pre-existing defect can alter the local energy configuration, leading to a higher electric field and, therefore, to a larger defect creation probability. Once enough defects are created and link up in a complete conduction path, as shown in Figure 77 (c), a large current can flow through the oxide, leading to a loss in isolation and to the possible catastrophic failure of the oxide if the power dissipation is too high.

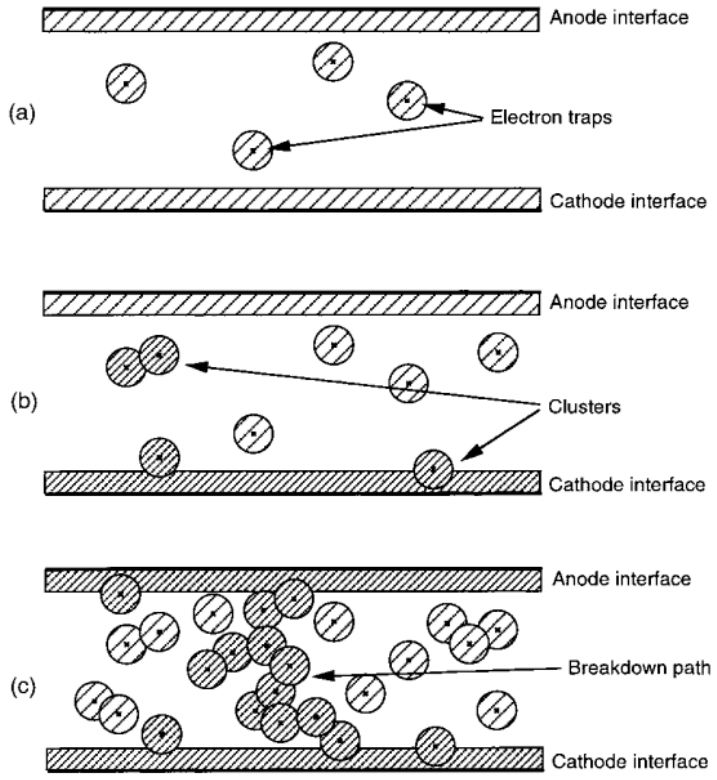


Figure 77: sketch of time-dependent dielectric breakdown caused by defect percolation. [512]

Since the defect-creation process is field-assisted, operation of a device at a larger gate overdrive causes a faster degradation, as commonly observed; in reliability tests a β parameter of the Weibull distribution larger than 1 may be extrapolated, consistently with a degradation related to intrinsic causes.[513], [514] Before catastrophic failure occurs, detected effects on the device performance include increase in the gate leakage current due to the creation and destruction of the metastable conduction paths (see Figure 78) [515] and the increase in gate leakage absolute value,[516] but the effects on the device performance in terms of threshold voltage and drain current are minor.[516] The possible presence of hole trapping in the oxide, originated by impact ionization under the high electric field, has also been speculated.[514]

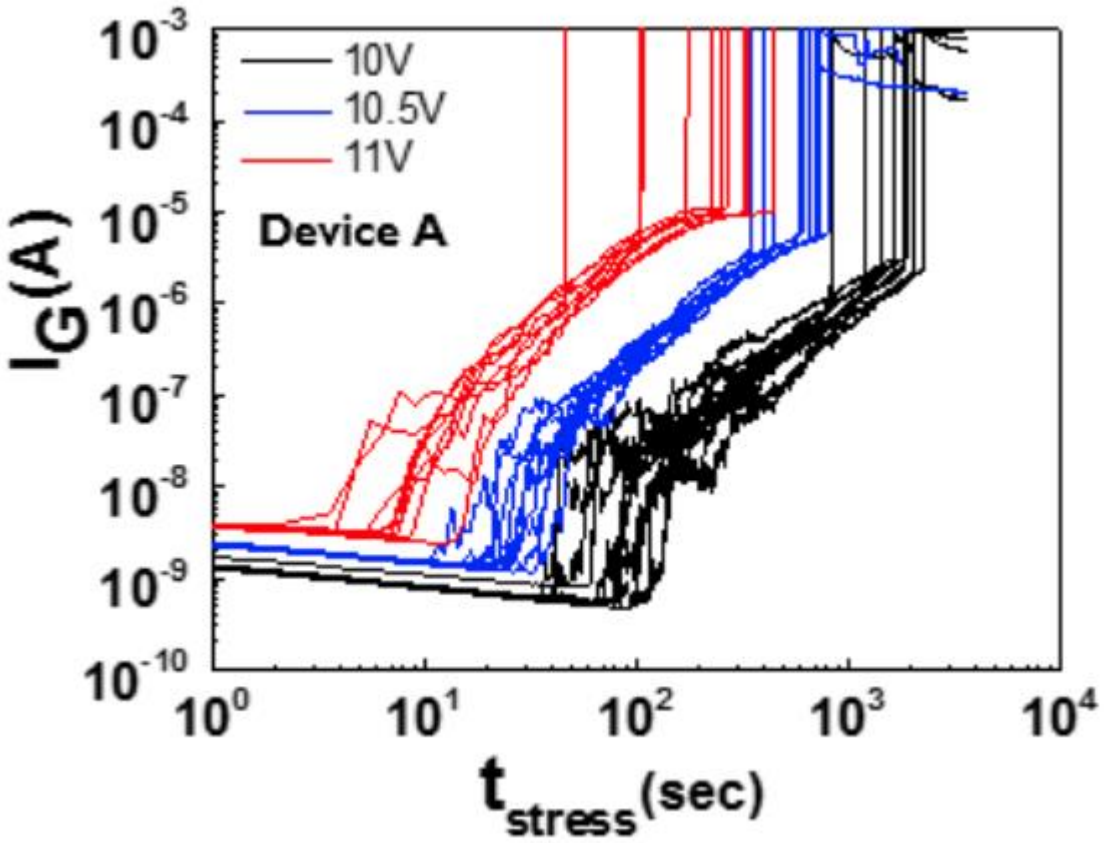
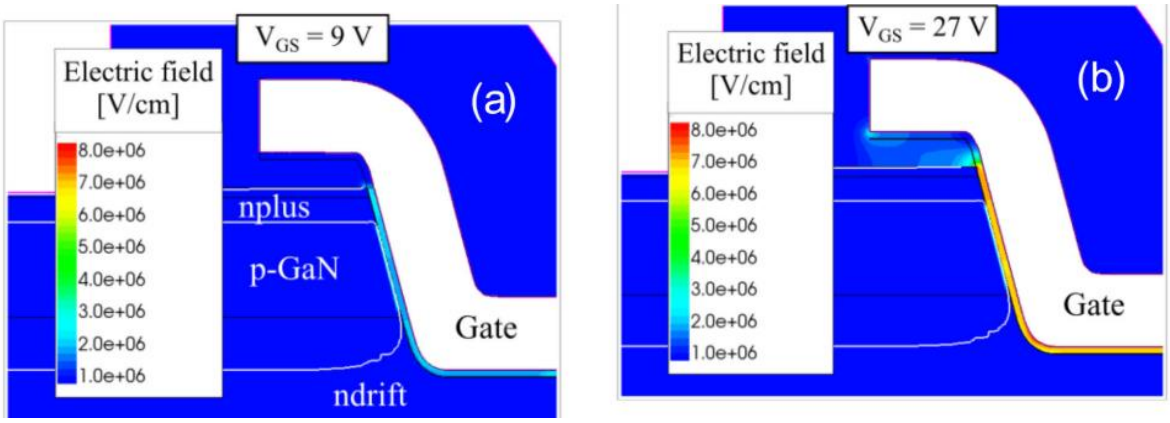


Figure 78: Increase in gate leakage and metastable behavior caused by ON-state stress in a MIS-HEMT. [515]

The TDDB can affect not only lateral devices but also vertical ones, such as trench MOSFETs[284], [517] and FinFETs.[518] The results quoted above demonstrate the possibility of using electroluminescence measurements to pinpoint the location of the failure spots in the device, and of limiting the current during the catastrophic failure to avoid extensive damage to the sample, leaving a failure analysis feasible on the detected spot. Additionally, a careful design of the insulator composition and bilayer structure can significantly improve robustness and lifetime.[517] In the case of trench transistors, numerical simulations show electric field crowding at the trench edges,[284] whereas in the FinFETs it is located at the corner of the dielectric, at the foot of the fin [518] (Figure 79).



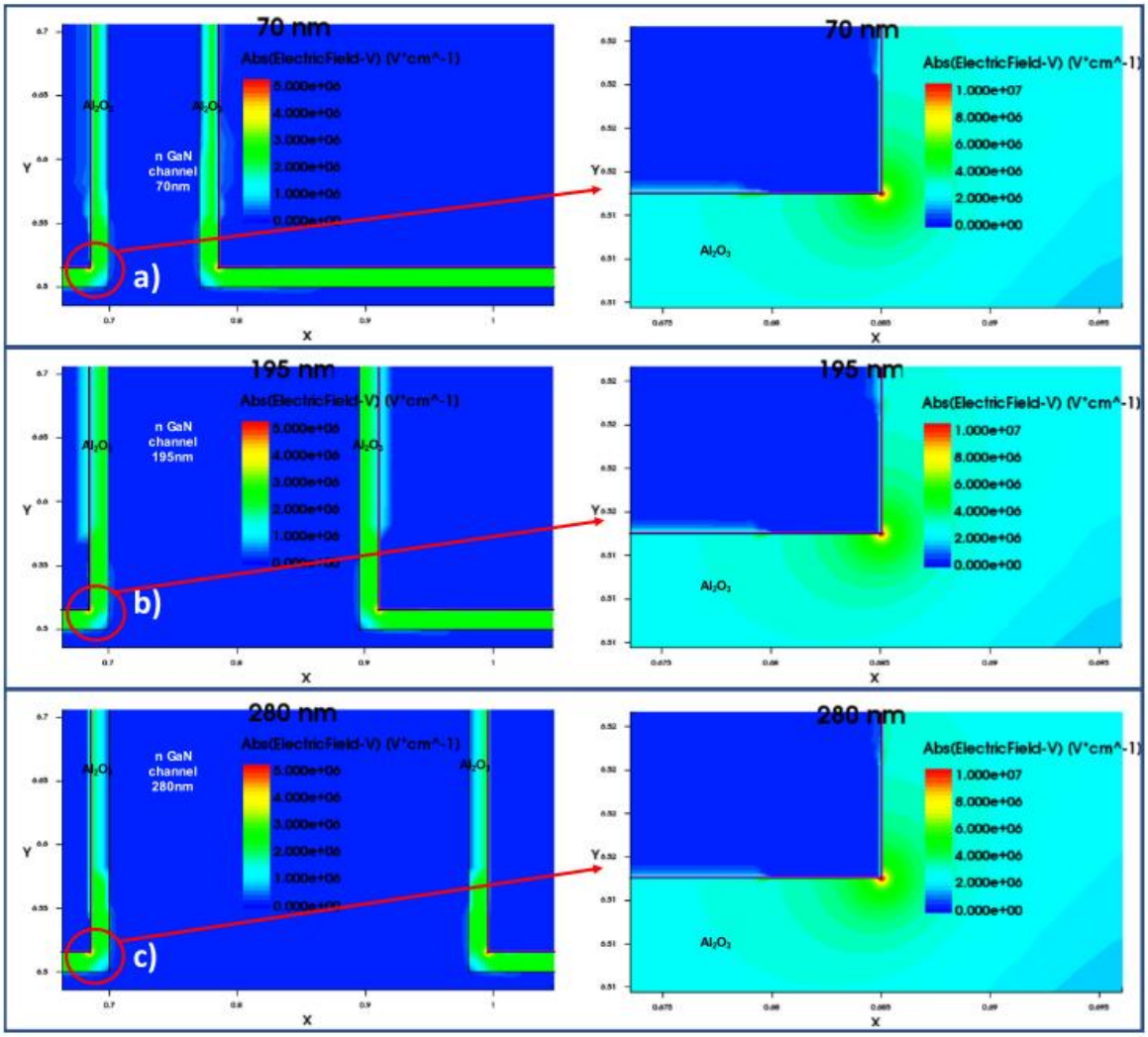


Figure 79: numerical simulations of the electric field in (top) trench MOSFETs and (bottom) FinFETs. [284], [518]

9.1.2 Degradation of p-GaN gate stacks

In order to achieve normally-off operation, the most common approach is to use a p-GaN gate layer, as discussed in Section 6.2.4. Under the strong gate overdrive of typical operating conditions and with the channel formed, a large voltage drop and electric field is present in the thin p-GaN layer, leading to possible reliability issues.

When a stress below the catastrophic failure is applied, a time-dependent degradation process might still be present, leading to sudden jumps and a larger noise in the gate current level.[519] The jumps are associated to the appearance of additional electroluminescence spots at the gate edge, suggesting that conductive paths are created in the gate stack due to a defect generation and percolation process, similar to what was found in the case of dielectrics in the previous section.[520] Early reports suggested that the traps are created due to impact ionization of electrons injected from the channel into the p-GaN region and accelerated by the high electric field.[521] This idea still needs to be supported by spectral electroluminescence measurements; so far, no band-to-band recombination and only bremsstrahlung and yellow luminescence,[520] or other sub-bandgap wavelengths have been detected.[522]

An additional similarity with the dielectric degradation is the exponential dependence of the time-to-failure on the stress voltage, which is also found to be Weibull-distributed. The shape parameter β has been reported to be lower than 1, suggesting an extrinsic breakdown mechanism,[520], [523], and greater than 1, as in recent reports.[522], [524] The degradation should happen at the edge of the gate, as suggested by the aforementioned EL measurements and by tests of devices with different gate width and gate length.[525] This is supported by results of numerical simulations (Figure 80), showing that the electric field value is maximum at the edge of the p-GaN, lower in the center of the p-GaN and furthermore reduced in the AlGaN barrier, which should therefore not cause any reliability issues.[520]

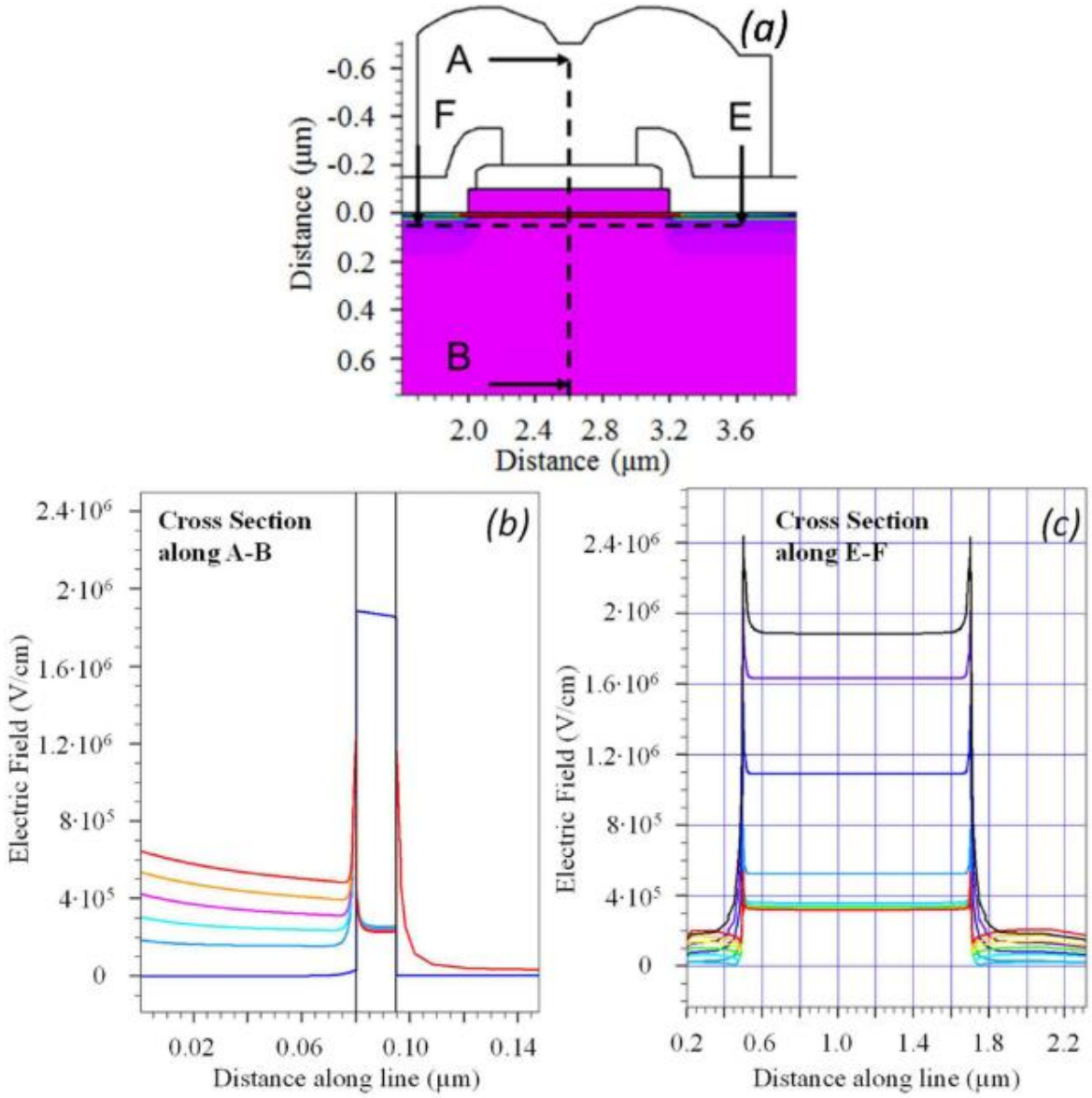


Figure 80: Numerical simulations of the electric field distribution in the p-GaN and AlGaN barrier during high gate bias stress. [520]

Even though the degradation is found to be faster at higher temperature,[525] a different behavior can be seen in case of more complex degradation processes.[526], [527] In [526], the degradation is supposed to be enhanced by the accumulation of positive charges at the p-GaN/AlGaN interface, which promotes the injection of electrons from the channel into the p-GaN, with consequent degradation. Higher temperature leads to more hole release, therefore improving the reliability.

The presence of the hole trapping is confirmed by the fact that the gate current decreases during stress, due to the electrostatic repulsion between the injected and trapped holes. This degradation process is sketched in Figure 81, which also shows the electroluminescence distribution and the correlation between the electroluminescence intensity and the gate current. It is worth mentioning that carrier acceleration and impact ionization are also less prominent at high temperatures, due to the increased scattering, and this can also contribute to the positive temperature coefficient.

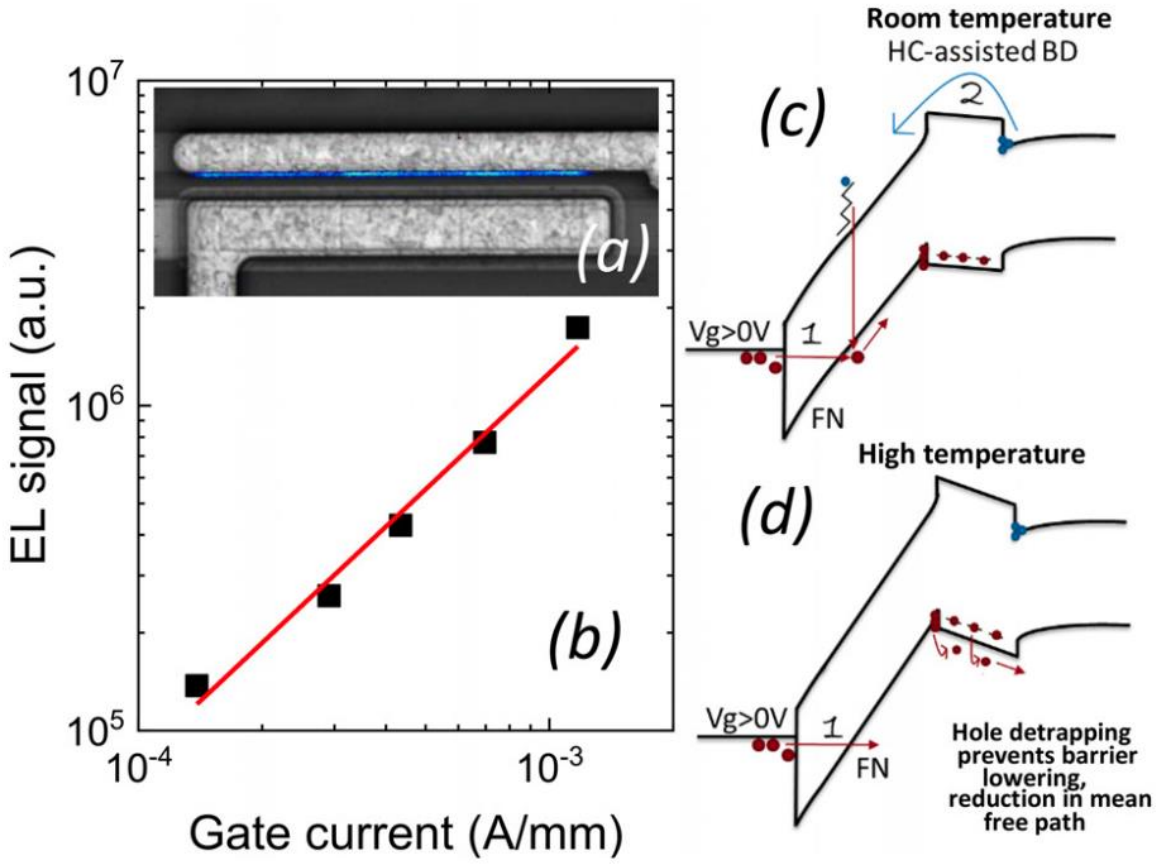


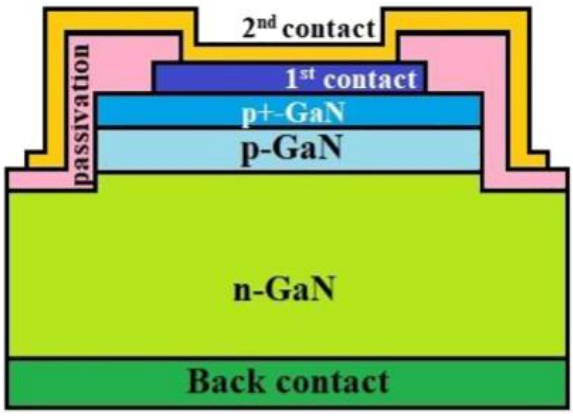
Figure 81: (a) spatial distribution of the electroluminescence and (b) its correlation with the gate current. (c-d) sketch of the degradation process leading to a higher robustness at high temperature in p-GaN gate devices. [526]

9.1.3 Vertical devices

Some results on the degradation of vertical devices were already discussed in section 9.1.1, since they were related to dielectric degradation, but other processes are exclusive to vertical structures and will be discussed in this section.

In the case of vertical p-n$^-$-n diodes and vertical junction field-effect transistors, most of the failures in common reliability tests (HTRB, HTOL, THB, TC) are related to the substrate quality, the substrate miscut angle and the morphology of the surface after the epitaxial growth.[528]

More detailed studies on pn vertical diodes show that forward bias stress induces an increase in series resistance, in turn-on voltage and in forward and reverse leakage current, as well as a reduction in the optical power emitted by diode due to band-to-band recombination in forward bias.[529] The variation in series resistance and optical power are well correlated, and their variation has a square root dependence on time, as shown in Figure 82. All the experimental results can be explained according to the following model. During stress, the flow of carriers, aided by the temperature, can break the residual Mg-H bonds that are still present after the Mg activation phase done during growth. Hydrogen interstitials can then diffuse following the concentration gradient towards the n-type material. The diffusing hydrogen can passivate Mg atoms closer to the p-n interface, decreasing the hole concentration. This causes an increase in the turn-on voltage and the reduction in the amount of holes available for radiative recombination. The dependence on the square root of stress time is a common signature of diffusion-related degradation, being originated from the solution of Fick's second law of diffusion in one dimension.[530]



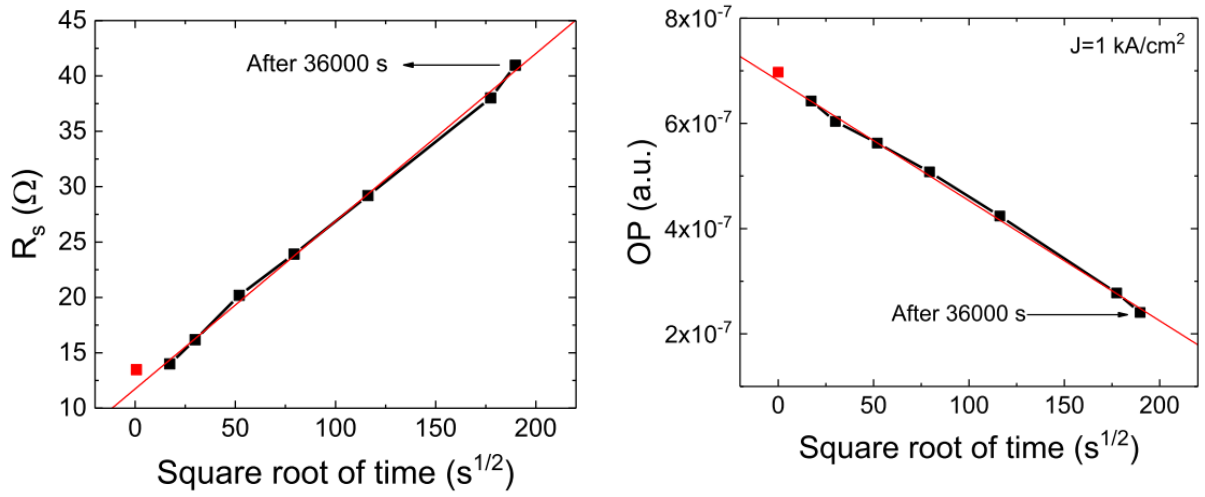


Figure 82: (top) Schematic cross-section of the vertical GaN pn diode; (bottom) Dependence of the increase in the series resistance and of the decrease in electroluminescence intensity on the square root of stress time. [529]

9.1.4 RF stress

Operation in radiofrequency (RF) conditions is not relevant for power devices but only for amplifiers, but a useful conclusion can be drawn by the analysis of the difference in degradation between DC and RF conditions.

In the case of RF devices, a common degradation cause is the presence of hot electrons in near pinch-off conditions, especially when short channel effects and poor carrier confinement play a role due to the reduced gate length. Since the process is influenced by the source-drain leakage, a correct compensation of the buffer conductivity can significantly improve the reliability of the devices, with Fe and C co-doping leading to the best results.[531] The degradation mechanism is field-driven, as suggested by tests on devices with and without field-plates.[532] A RF stress usually induces small variations in the DC performance of state-of-the art devices, mainly a lowering of the saturation current and a decrease in gate leakage,[533] but the generation of defects causes an increase in the dynamic current collapse.[534] A negative[535] or positive[536] shift in

threshold voltage is also observed sometimes, due to the presence of traps in the cap and barrier layer.[535]

The important conclusion comes from the comparison between devices stressed in DC and RF conditions, showing different degradation modes and a stronger degradation in the RF case.[535] This suggests that, even for power devices, it may be important to test the degradation not only in ON-state, OFF-state and SEMI-ON-state separately, but to test it also in the real switching pattern, to take into account the interplay between the different mechanisms and time dependence occurring in the various bias points of the switching locus.[537]

9.2 OFF-state

The OFF-state bias condition can be highly stressful for a power device, due to the high electric field present, on average, in the blocking region and peaking in critical device regions, such as the sharp corners and the gate edge. The electric field can cause damage to materials that are part of the device without being the semiconductor itself, such as the insulators for passivation and gate isolation. Other processes may involve the breakdown of gallium nitride itself. In addition, interaction with the external atmosphere may promote field-assisted chemical reactions. In some cases, the high electric field can also be present together with a high current density, such as during avalanche conduction. In the following, we will discuss all these possibilities.

9.2.1 Extrinsic degradation: the role of dielectrics

As discussed in section 9.1.1, degradation of the dielectrics is usually present in ON-state stress conditions, since the voltage drop across the gate insulator is the highest, whereas in OFF-state stress the large voltage drop in the depleted semiconductor mitigates the electric field across the gate stack. Therefore, some of the results already presented in section 9.1.1 still hold, even when a larger bias is applied: the better reliability of engineered bilayer insulators,[284], [517] the

location of weak spots corresponding to electric field peaks[518], and the negative[511] or positive[538] threshold voltage shift related to defect generation, which may also cause worse dynamic performance.[511]

Nevertheless, additional dielectrics are present in the complex structure of a state-of-the-art GaN power devices, such as the ones used for passivation and isolation of the field-plates. Their degradation results in an increase in gate leakage level and noise, eventually leading to catastrophic failure even significantly below the breakdown voltage of the device; dielectric degradation is typically characterized by an exponential dependence of the average time to failure on the stress voltage.[539] In this case, the shape parameter β of the Weibull distribution is lower than 1, suggesting that reliability is limited by extrinsic factors. A possible origin for this experimental behavior is the degradation of the silicon nitride used for the passivation and field plate isolation. As can be seen through numerical simulations (Figure 83 (a)), in the case described in [539], in off-state conditions the peak of the electric field is located in the silicon nitride, in proximity of the edge of the gate overhang on the drain side, and the value is ~6 MV/cm, comparable with the theoretical breakdown electric field (~ 6 MV/cm). [539] The electric field in the AlGaN barrier is lower than 3 MV/cm, therefore degradation in this layer is unlikely. This hypothesis can be confirmed by locating the failure spot by means of electroluminescence measurements (Figure 83 (c)) and performing cross-sectional transmission electron microscope (TEM) failure analysis on it.[540] As can be seen in Figure 83 (b), the damaged region starts at the edge of the gate region and extends into the channel region.

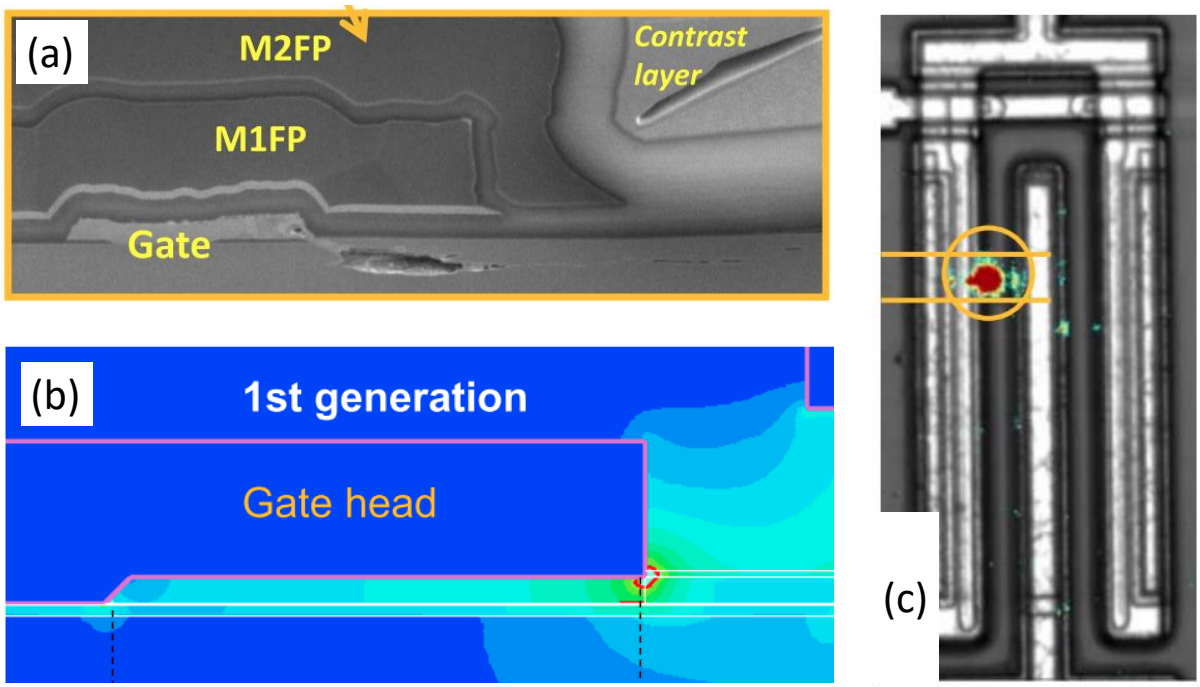


Figure 83: (a) TEM cross-section analysis is able to identify the degradation caused by (b) the peak in electric field at the edge of the gate head (as obtained by numerical simulations), located by means of (c) electroluminescence measurements. [539], [540]

The mechanism can be further confirmed and solved by changing the vertical conductivity in the epilayer, leading to a different grounding of the floating buffer and, therefore, to a larger 2DEG retraction in the case of the improved devices, as shown in the numerical simulations in Figure 84 (d).[539] This leads to a significantly lower electric field in the silicon nitride for the second generation of devices (Figure 84 (a-c)) and to an improvement in the time-to-failure of more than three orders of magnitude, as shown in Figure 84 (e).

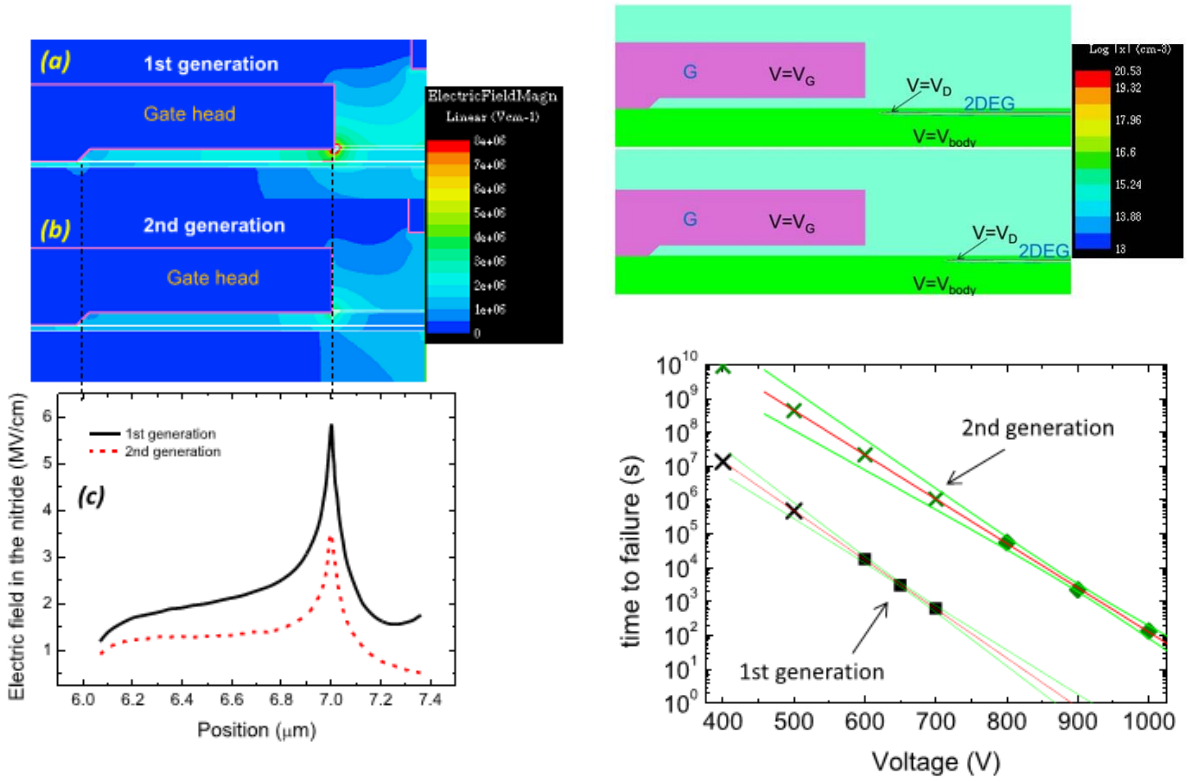


Figure 84: (a-c) improved devices with different grounding of the floating buffer have a lower electric field due to (d) the larger 2DEG retraction. (e) this change leads to an increase in time-to-failure by more than three orders of magnitude. [539]

A second possible solution is to change the length of the gate head at the drain side, limiting the peak electric field, or to add an extra SiN layer under the gate head.[540][541]

9.2.2 Degradation of GaN stacks

9.2.2.1 Converse piezoelectric effect

As discussed in Section 4, gallium nitride is a polar material. Any polar material, when submitted to a compressive or tensile mechanical stress, builds a potential across itself, and this behavior is called direct piezoelectric effect. In polar materials the opposite is also true. An external voltage

applied in the direction of the polarization vector may cause an expansion or a contraction of the material: this is called the converse (or inverse) piezoelectric effect. A sketch of all the processes is shown in Figure 85.

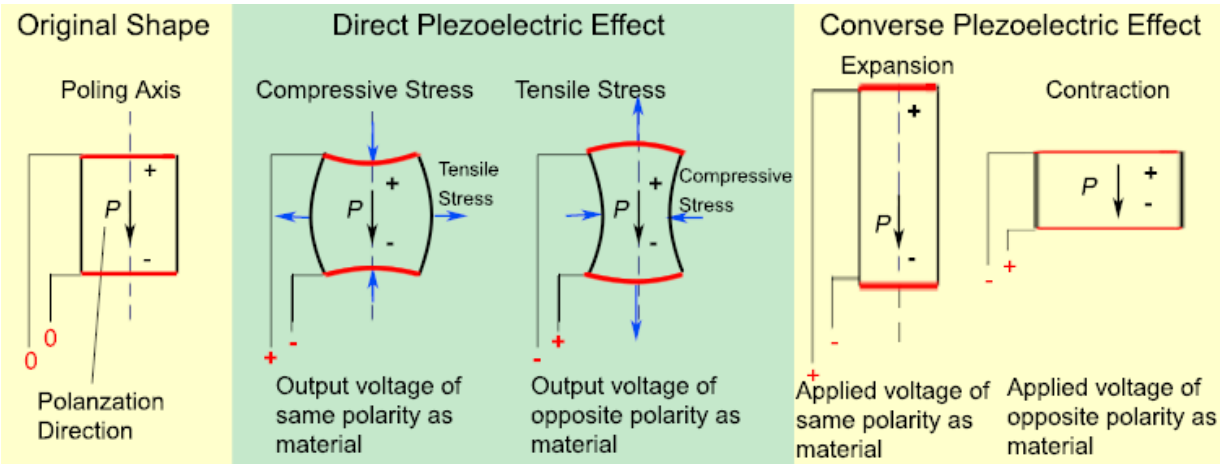


Figure 85: sketch of the direct and converse piezoelectric effect in polar materials. http://resources.edb.hkedcity.net/physics/articleIE/smartmaterials/SmartMaterials_e.htm

This behavior is not only theoretical, but can be experimentally measured by means of interferometric techniques on GaN crystals.[542] The amount of displacement caused by different voltages applied to a 2.5 μm thick single crystal [0001] GaN film is shown in Figure 86, and corresponds to a displacement of 0.05 nm at an electric field of 64 000 V/cm, i.e. to a displacement of 1.56 nm at an electric field of 2 MV/cm. The electric field peak found close to the gate edge at the drain side in common HEMT devices is close or can even exceed this value, even in presence of multiple field plates, in common high power operation. Therefore, one may wonder if this level of displacement (without considering the different value of the piezoelectric coefficients between the reported GaN film and the AlGaN of the barrier) can cause damage to the device and limit its reliability. Of course, a localized electric field would not be enough to produce a displacement, since the lattice would build up strain to accommodate for the expected local displacement, but the levels of piezoelectric stress originated by the expected variation can be very high, in the order of hundreds of MPa.[543], [544]

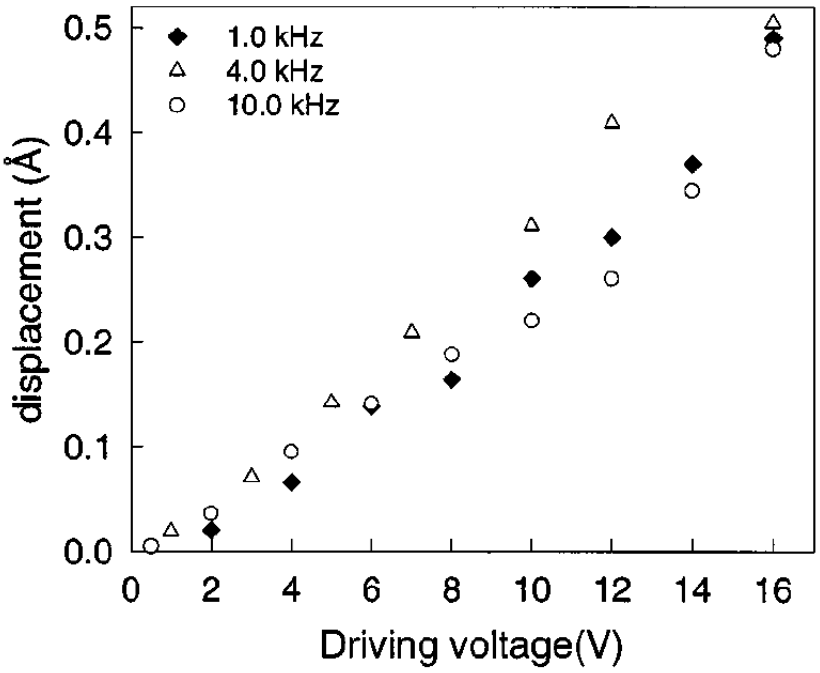


Figure 86: GaN displacement measured at various applied voltages. [542]

This idea was proposed for the first time in 2006,[545] and a lot of work has been done to identify this mechanism in the following years. Specific tests have found the presence of a critical gate or drain voltage for the degradation, consistent with the build-up of a critical amount of strain in the structure before relaxation and formation of defects takes place.[545] When stressed above the critical voltage, an increase in charge trapping inside the AlGaN barrier takes place, consistently with the generation of defects in that region, whereas the trapping in the buffer remains unaffected.[546] By means of stresses at different gate voltages and current levels it was possible to exclude any effect of the hot electrons in the process, since the stress current was found to have no impact on the critical voltage value.[547] The generation of cracks only at the drain side of the gate taking place above the critical voltage, without any impact in the degradation of temperature or hot electrons, was reported by TEM measurements.[548]

The generation of indentations, pits and grooves at the drain side of the gate edge was confirmed also by atomic force microscope (AFM) and scanning electron microscope (SEM) testing of

stressed devices after chemical etching of the gate metal, as shown in Figure 87. At least some of the new pits form without the presence of any pre-existing defects, consistently with the inverse piezoelectric effect. The defects act as gate leakage paths, may reduce the maximum drain current and favor the charge trapping in the device.

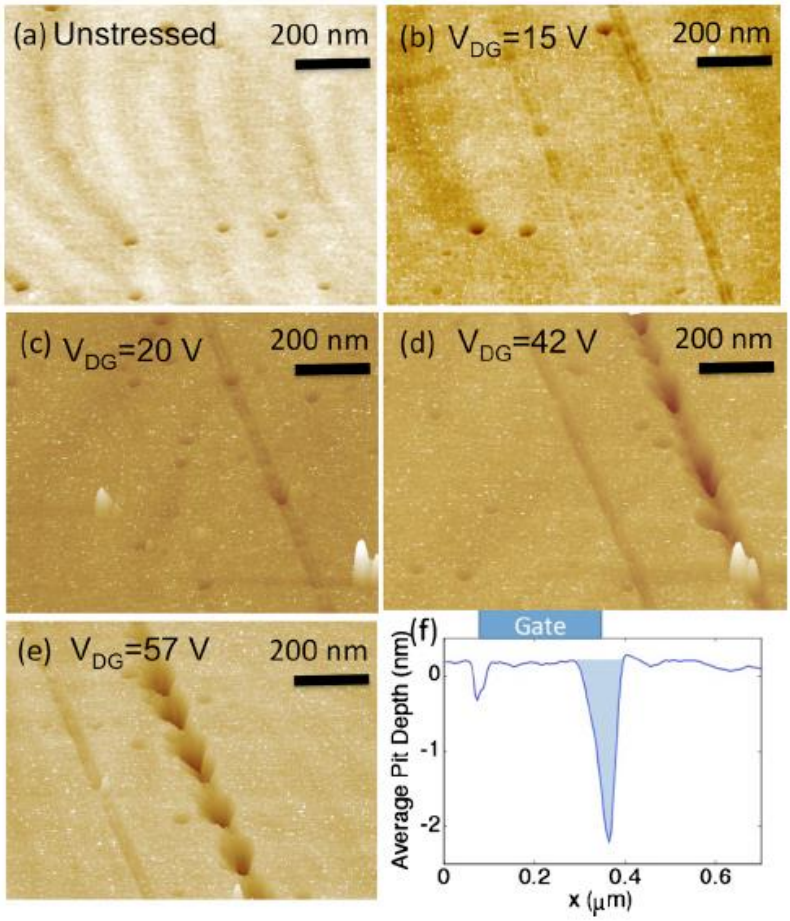


Figure 87: formation of grooves and pits in devices stressed at increasing drain-gate voltage. [549]

9.2.2.2 Electrochemical degradation

The formation of localized damage at the edge of the gate can be visible even below the critical voltage, due to other processes involving chemical reactions.

When devices are stressed in reverse gate bias conditions, particles and stringers appear along the gate edge, both at the source and the drain side, as shown in Figure 88 (a-c).[550] Their chemical composition can be determined by Auger electron spectroscopy (AES), reported in Figure 88 (d), highlighting an oxygen-rich composition and the presence of gallium. The quantitative analysis is compatible with the formation of Ga_2O_3 and Al_2O_3. After metal removal, the presence of large pits below each oxide particle is clearly visible (Figure 88 (e)). By changing the polarity of the stress bias on the gate-source and gate-drain diodes, it is possible to demonstrate that the oxide forms where the electric field is the highest. By testing devices in vacuum it was possible to demonstrate that the oxide only forms when oxygen is present in the atmosphere, and it is supposed that oxygen diffuses through the passivation layer and locally oxidizes the AlGaN/GaN layers.

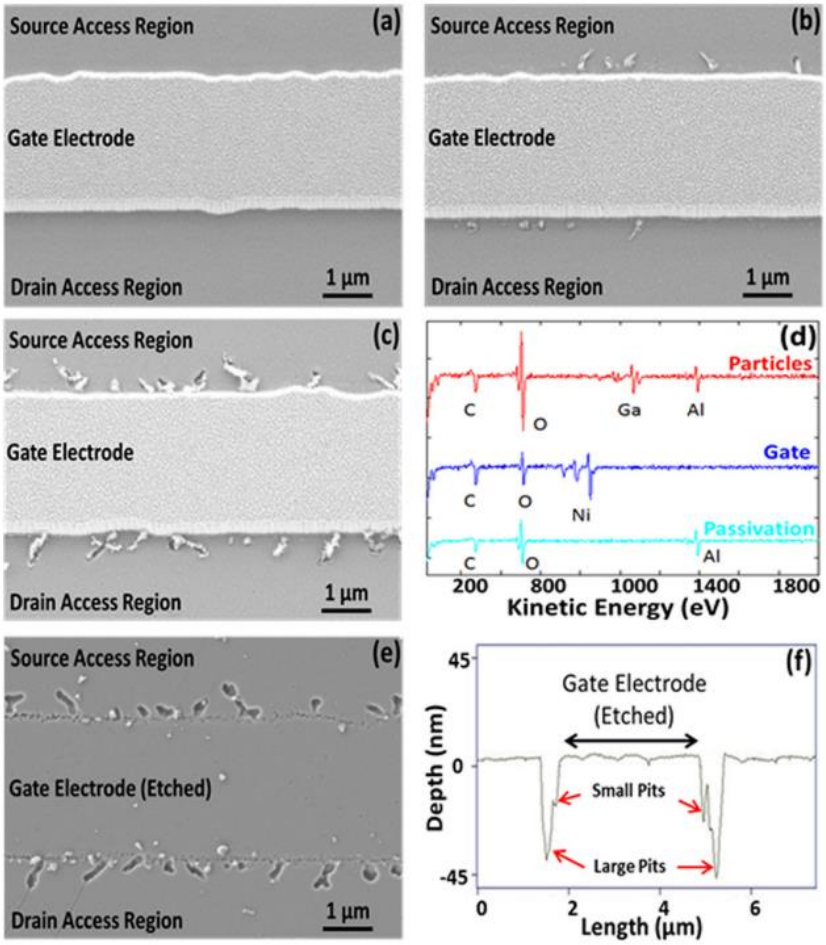


Figure 88: (a-c) top view SEM images of an HEMT stressed at reverse gate bias for increasing periods of time. The chemical composition of the stringers is shown in (d), and (e) shows the pits that form below them. [550]

Similar effects can be produced by reaction with hydroxyl groups (OH^-) or water.[551] In this case, the degradation happens due to anodic oxidation of the AlGaN layer in the electrochemical cell composed of the gate metal, the passivation layer and the barrier, aided by water and by the presence of holes. The main effects are a degradation in drain current and dynamic performance, whereas in this case the increase in gate leakage is not caused by the presence of the pits.

It is also suggested that an exclusion zone can appear around the pits, where no additional degradation spots can be formed, as the result of the consumption of mobile species in the electrochemical reaction.[552]

9.2.2.3 Time-dependent breakdown of GaN epitaxial stacks

The results presented in section 9.1.2 for the p-GaN degradation show trends comparable to the ones reported in section 9.1.1 for the time-dependent dielectric breakdown degradation, namely the Weibull distribution of the failure time and its exponential dependence on the stress voltage. One can then wonder if gallium nitride itself, when deeply depleted, can behave as a dielectric and experience a TDDB-like degradation process. In general, detecting a TDDB process in a full GaN power device can be complex, due to the large number of parts and materials it is composed of, each of them possibly contributing to the degradation as discussed in this Section 9. Moreover, if a device is not fully vertical, both a lateral and a vertical electric field are present, further complicating the analysis. Therefore, even though the presence of GaN TDDB was suggested in the past, no demonstration excluding other possible causes was provided.[553], [554] For this reason, the first conclusive demonstration of time-dependent dielectric breakdown in the gallium nitride itself was done on optoelectronic devices.[555] LEDs have an intrinsic vertical structure, no complex parts such as field plates, gate with various geometries, blocking dielectrics or engineered passivation, and are already at a high technology readiness level, allowing for testing of stable and reliable devices with no reliability and behavioral issues, which is not the case for fully-vertical power devices. The experimental tests, carried out in reverse bias condition, confirm that gallium nitride behaves as a leaky dielectric when deeply depleted, that the time-to-failure has an exponential dependence on the stress electric field, and that it is Weibull distributed.[555] The extrapolated shape parameter β is 4.43, confirming that the devices under test show an intrinsic failure behavior. Consistent results were obtained also on GaN-on-Si stacks used for the fabrication of GaN transistors. It was demonstrated that when submitted to drain-to-substrate (2 terminal) stress, AlGaN/GaN transistors can show a time-dependent degradation, which is Weibull distributed, significantly field-dependent and weakly thermally activated (Ea=0.25 eV). Degradation was ascribed to a percolation process, leading to the generation of localized shunt paths between drain and substrate. [556]

9.2.2.4 Buffer decomposition experiments

When a lateral power device is biased in the off-state, a large voltage drop is present in all the layers from drain to substrate, which usually include the AlN nucleation layer, an AlGaN buffer and a carbon-doped GaN buffer. Understanding which of these layers has the strongest impact on the vertical breakdown voltage and on device reliability is a critical task for improving the final behavior. This can be done by testing separate structures, where the growth has been stopped after each of the single layers above the silicon substrate, to form AlN/Si, AlGaN/AlN/Si, and C:GaN/AlGaN/AlN/Si stacks.[557] [558] This way, the variation in reliability (and charge trapping) induced by each layer can be analyzed independently. In order to do this, a mandatory technical requirement is the processing of good ohmic contacts on top of each layer, a non-trivial task on low-conductivity and wide-bandgap materials.

The analysis of AlN layers directly grown on a silicon substrate indicated a breakdown field of 3.25 MV/cm, which is significantly lower than that of high-quality crystalline AlN. The difference is ascribed to the presence (and high density) of vertical leakage paths, involving V-pits and threading dislocations. This value further decreases with temperature (see Figure 89) [558]. To explain this temperature dependence, the failure voltage was plotted against the leakage current. Samples with higher leakage showed a lower breakdown voltage, and a lower breakdown field, of the AlN nucleation layers. The flow of current at localized defects may lead to premature breakdown. This argument was used to explain why the breakdown field of AlN grown on silicon (3.25 MV/cm) is much lower than that of high quality crystalline AlN (up to 12 MV/cm).

In addition, it was demonstrated that the AlN/Si structures show trapping of negative charge, which has been ascribed to the injection of electrons from the silicon substrate towards deep traps located in the AlN. By adding an AlGaN layer on top of the AlN, it is possible to significantly reduce the density of defects, and this results in a more uniform sample-to-sample leakage current. A strong increase in the breakdown voltage can be reached by adding a C:GaN layer on top of the stack. In this case, the structures analyzed in [558] showed breakdown voltages larger than 800 V. It is worth noticing that the presence of a C:GaN layer can result in positive charge trapping. This is ascribed to the presence of holes from C:GaN, that are trapped at the GaN/AlGaN interface, leading to the storage of positive charge in the buffer.

In the case of the AlN/Si stacks under analysis, the leakage current originates, as confirmed by numerical simulations, from the series connection of equivalent AlN/n^+-Si and n^+-Si/p-Si junctions, due to the presence of an inversion layer at the interface.[559] The limiting factors are the p-doping level of the silicon substrate and the electric field at the interface, since both of them control the tunneling injection from the silicon substrate into the AlN layer.

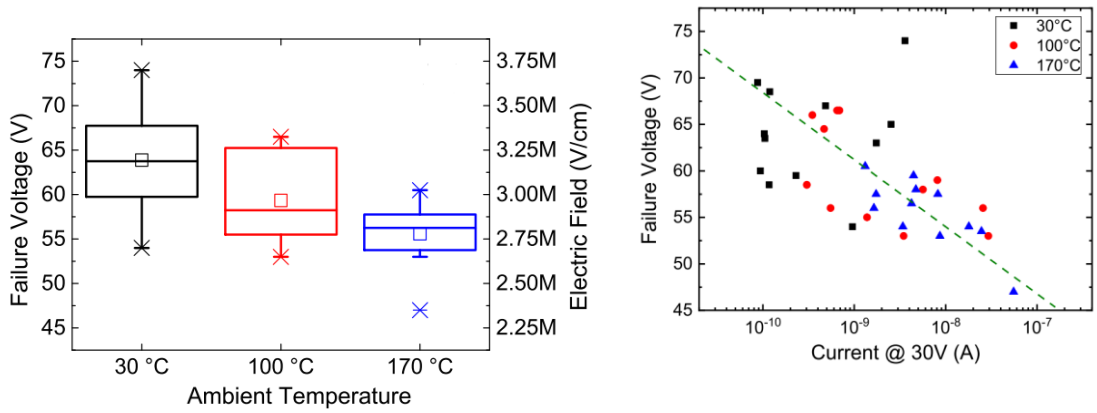


Figure 89: Dependence on temperature of the failure voltage of AlN/Si layers, and its correlation with the leakage level. [558]

9.2.2.5 Avalanche operation and walkout (in vertical devices)

All the processes discussed above can affect also vertical devices, but a degradation mechanism exclusive to them exists. Vertical power devices are built in order to withstand high voltage levels, as discussed in section 7, and the high electric field and long drift region makes them capable of avalanche current conduction. This is not an unwanted side-effect but a desired feature, especially in power diodes, since it allows them to withstand surge events.

However, one needs to consider that if the structure is not optimized, operation in avalanche mode may be detrimental for the reliability of the devices, due to the high electric field and to the

presence of a large number of highly-energetic carriers. The former can cause failure due to non-optimal termination and electric field peak at the bevel surface,[560] whereas the latter can create significant lattice damage.[561]

The actual defect species responding during avalanche operation is not yet clear, but a possible hypothesis is that carbon in nitrogen substitutional position (C_N) may be involved. These defects create a wide range of effects, including an increase in series resistance and leakage current, a variation in the turn-on voltage, an increase in avalanche breakdown voltage (avalanche walkout [562]) and a worsening of the dynamic performance. The analysis is made more complex by the large variations in vertical electric field in the lateral direction, as summarized in Figure 90. In the high-field region, the avalanche condition and the high current conduction causes damage creation and trapping of a part of the flowing charges, whereas in the medium field region no avalanche is present, only a negligible amount of current is flowing and therefore the main effect is field-assisted de-trapping of native charge. When the device is moved to measure bias condition, the trapped carriers cause the increase in avalanche breakdown voltage, the de-trapped ones modify the turn-on voltage, and the lattice damage impacts on the leakage current and the series resistance.[561]

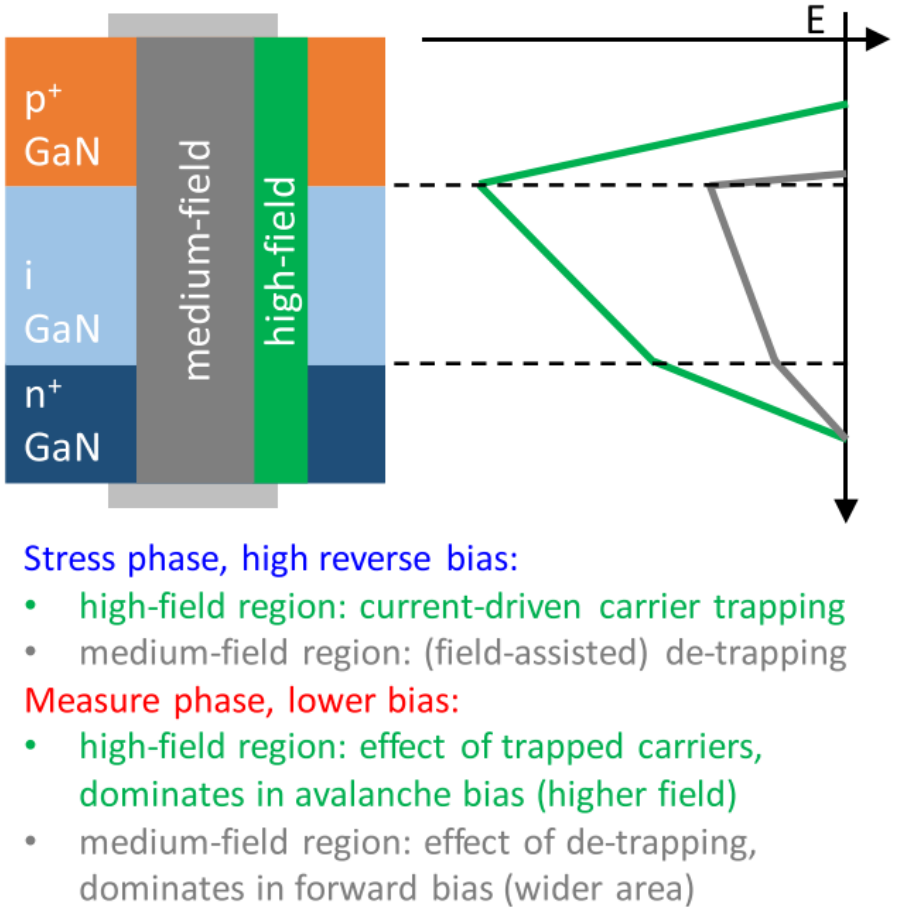


Figure 90: summary of the possible effects taking place in a vertical GaN power diode during stress in avalanche conduction. [173]

9.3 SEMI-ON-state

In real operating conditions, a power switch is not limited only to ON-state and OFF-state bias points. During the turn-ON and turn-OFF transitions, the presence of the internal and parasitic capacitances prevents an instantaneous variation of the voltage at the terminals of the device, therefore a relatively high voltage at the drain can still be present when the gate voltage is already close to the threshold value. This bias condition is called SEMI-ON-state, because the conductive channel is partially formed. Depending on the residual drain voltage during the transition, in SEMI-

ON-state state a relatively large amount of electrons in the channel can be accelerated by a large electric field, causing the flow of highly-energetic (hot) carriers in the device that can be detrimental for its reliability.

The main effects a SEMI-ON-state stress can cause on a transistor include a worsening of the isolation properties of the gate diode, threshold voltage shifts, increase in ON-resistance, decrease in transconductance peak value, change in peak electric field, knee walkout and increase in drain-lag transient amplitude [563], [564]. These changes may be ascribed to the increase in defect concentration close to the channel region, shown in Figure 91, caused by the energy exchange between the hot electrons and the crystal lattice, as can be detected by several deep level characterization techniques applied during stress [564]. The specific microscopic configuration of the deep level causing the detected variations can change depending on the device growth conditions, structure and processing. Recent papers investigated the effect of hot electrons on the dynamic on-resistance of AlGaN/GaN high-electron mobility transistors subject to semi-on stress. The additional dynamic-Ron detected in semi-on state was ascribed to hot-electron trapping at the passivation/AlGaN interface [565].

Specific circuits [398], [566]–[568] can be used to test the degradation of GaN HEMTs induced by hot-electrons. A promising approach was proposed in [568], [569], based on the use of switching setups capable of monitoring on-wafer the effects of semi-on stress. By tuning the capacitance at the drain node, it is possible to control the amount of energy/charge released during hard switching events, and to evaluate the effect of stress on the devices. The comparison of results obtained via different techniques [482], indicated that hot-electron trapping is a very fast process, that takes place in few nanoseconds. The developed methodologies allowed to assess the trajectory of the switching locus, the power dissipated during the turn-on transitions, and the dynamic on-resistance of the devices (see an example in Figure 92). The kinetics of hot-electron trapping were modeled analytically in a recent publication, based on rate equations [570].

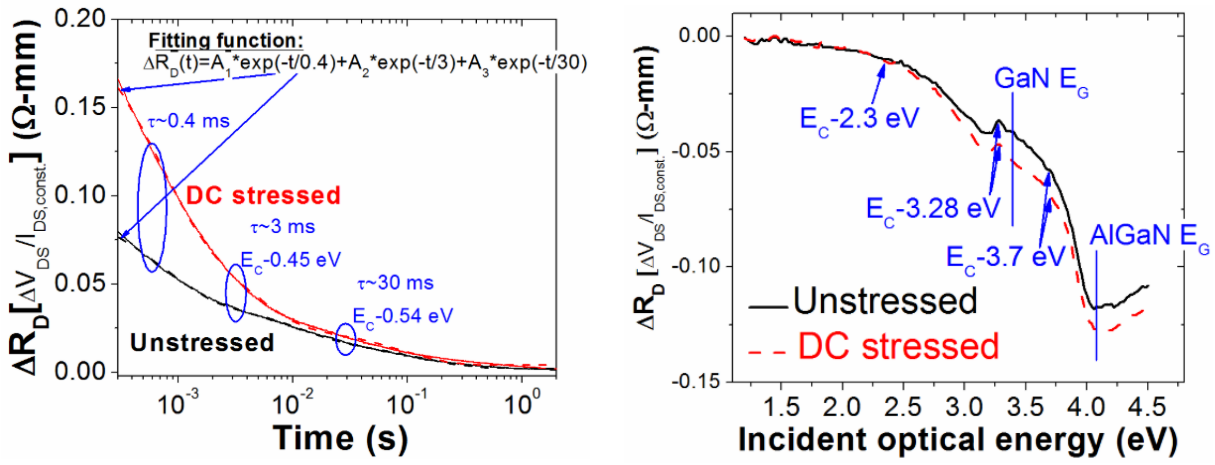


Figure 91: increase in amplitude of the drain-lag transient caused by SEMI-ON-stress, and corresponding increase in defect density detected by CI_D-DLOS. [373]

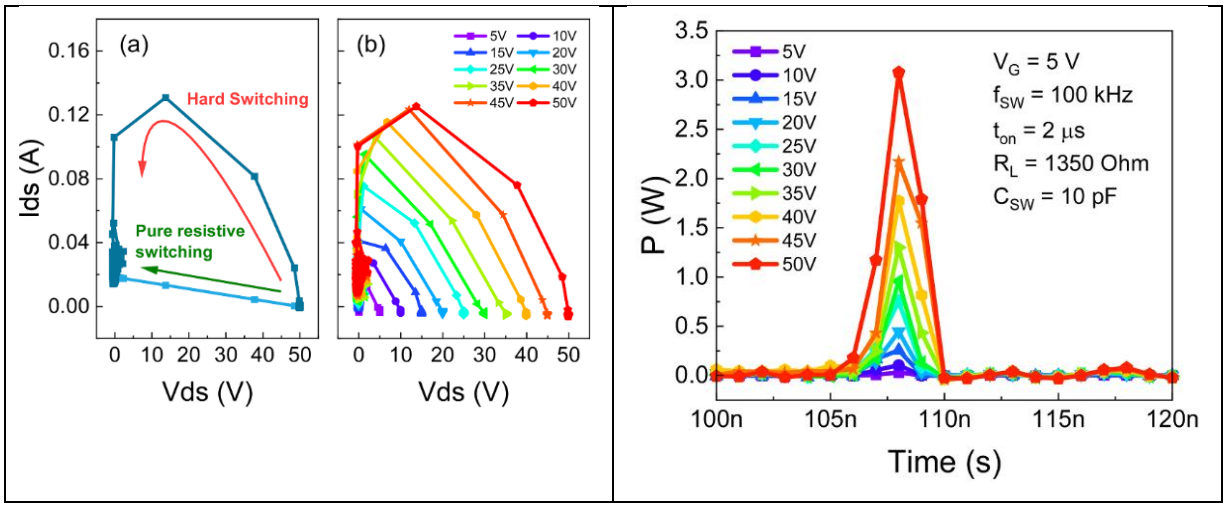


Figure 92: (left) Switching locus curve (a) comparing purely resistive switching and hard switching (b) applying different stress voltages (V_{DD}). The trajectory confirms the hard switching condition during the turn-on transition. (right) Power dissipated during the turn-on transition. The power peak increases with increasing the stress voltage V_{DD} [482](PERMISSION FROM https://iopscience.iop.org/article/10.1088/1361-6641/abc456/pdf)

In the specific case of gate injection transistors (GITs), a destructive positive feedback loop initiated by the hot electrons created during SEMI-ON-stress can lead to a rapid increase in the

electric field at the drain side and to the failure of the device. [537][571] This issue can be solved by using hybrid drain gate injection transistors (HD-GITs) device configuration, since the hole injection from the p-GaN at the drain partially reduces the amount of trapped charge caused by the hot electrons and the electric field peak.[537]

9.4 Electrostatic discharges and electrical overstress

Dangerous bias points for the reliability of a device can originate not only from the expected behavior during operation, but also from external unwanted stimuli. A frequent example is the application of short voltage or current pulses to one of the terminals, nanoseconds to seconds long, as a consequence of the interaction with users, the ambient conditions, or machinery during fabrication, assembly and handling. Collectively, these phenomena are called electrostatic discharges (ESD) and electrical overstress (EOS).

Under such high power dissipation conditions, several parts of the device can show degradation. One of them is the ohmic contacts at the source and the drain, as can be evaluated by tracking their specific resistance without any contribution by the channel resistance [572]. At increasing current stress levels in floating gate condition, the values of the contact resistance can significantly increase, up to a factor of ≈ 30. Backside infrared camera measurements, reported in Figure 93, show the creation of dark spots, attributed to electromigration leading to current filamentation. The spots are always present on the grounded contact, suggesting that not only the high power dissipation but also the current flow or electric field direction plays a role in the degradation. In this case, no variation in material parameters, charge density or electron mobility is observed.

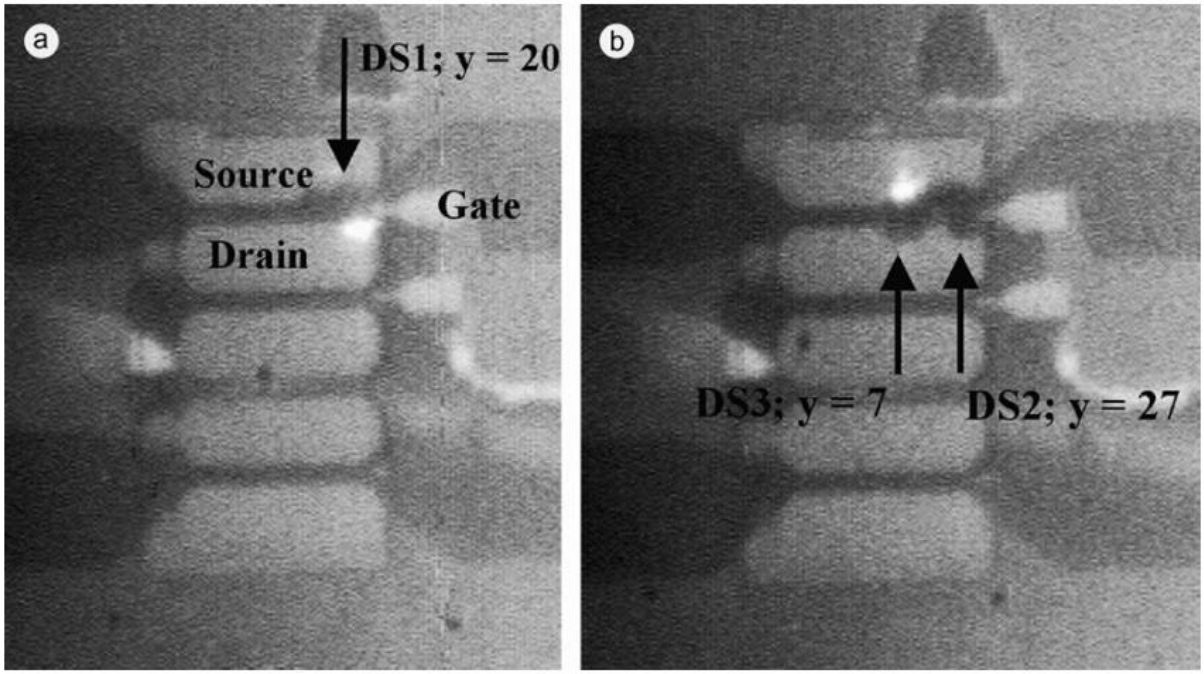


Figure 93: backside infrared camera measurements, showing the appearance of dark spots on the contact (source in part a, drain in part b) grounded during the ESD event. [572]

In general, issues related to contacts can be solved by an improvement in device processing, leaving other parts as the causes of degradation and failure. The substrate is no exception, especially if semiconductors with worse breakdown fields, such as silicon, are used in order to lower the cost and increase wafer size. This can easily be evaluated by testing lateral Schottky diodes, since additional structures can be tested to gain more information, as will be described in the following [573]. Schottky diodes tested in reverse conduction mode show no dependence of the failure voltage on diode length after a critical length, suggesting that the breakdown is not related to the lateral direction anymore. In order to investigate if the vertical electric field is causing the issue, specific buffer isolation structures can be fabricated, without and with silicon substrate removal, composed of isolated ohmic contacts connected only through the substrate. The structures with silicon substrate are found to fail at significantly lower voltage, confirming that the vertical electric field and the silicon breakdown field define the ESD robustness. If the ESD testing is carried out in forward conduction mode, the limiting factor is the high local power dissipation.

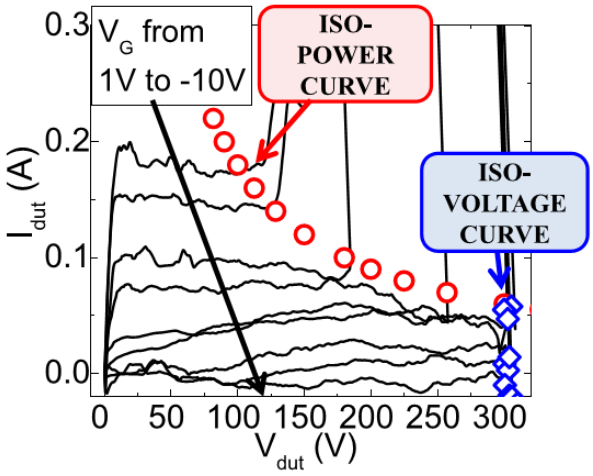
In a state-of-the-art transistor, the list of the possible effects caused by an ESD/EOS event extends beyond contact and substrate damage, depending on device structure and test conditions [574]. In normally-ON devices and gate grounded testing configuration, the melting of the gate metal and the formation of cracks from source to drain can be observed. In the case of shorter events (< 10 ns), the heating of the device is not high enough to lead to metal melting and catastrophic failure. Instead, several damaged regions can be found at the drain side of the gate edge, attributed to the converse piezoelectric effect caused by the high electric field during the event. Another possible failure mode is the breakdown of the parasitic diode between the gate finger and the drain and source contacts at the mesa edge.

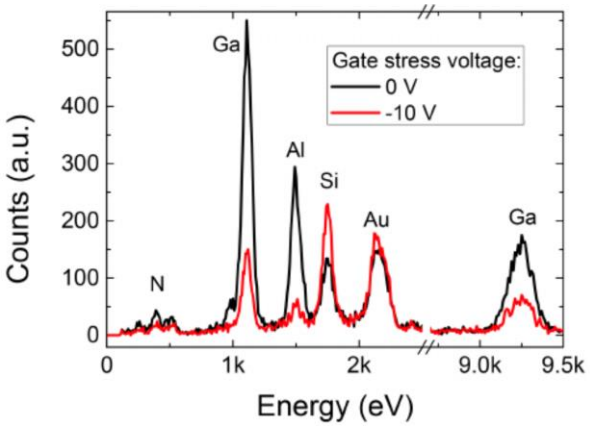
If the gate reliability is not the main goal of the analysis, it is possible to test devices without the gate metal [574]. If a mesa-type isolation is not present, the migration of the contact metal from drain to source, leading to a drain-source short, is a relevant process, especially at the corners of the contacts, where the electric field is the highest. The process is started by the melting of the metal at the high power dissipation condition, which is expected to happen at temperatures 1.5x to 4x lower than the GaN one. If a mesa isolation is present, the short-circuit instead forms along the channel, due to the presence of surface states that act as low-energy paths for the metal migration.

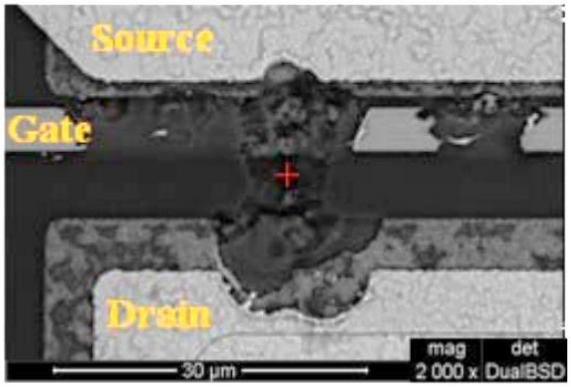
One of the main shortcomings with ESD/EOS testing on transistors is the fact that a single pulse is applied to the device under test, whereas it was demonstrated that GaN-based devices suffer from cumulative effects [574]. Another problem is that the protocol is usually based only on gate-floating and gate-grounded configurations. Unfortunately, in the real application the gate voltage will sweep the entire operating range, and there is no way to guarantee that the ESD event will happen only when the device is biased in one of the two tested configurations. For this reason, in a three-terminal device it is important to analyze the dependence of the robustness on the applied gate voltage [575].

As shown in Figure 94 (a), when the ESD event is applied in OFF-state and SEMI-ON-state, the catastrophic failure of the device always takes place at the same voltage on the device under test. This finding is consistent with a failure related to reaching the breakdown electric field of the material, which always happens at the same drain-source voltage regardless of the applied gate voltage. When the ESD event is applied in ON-state, the detected robustness is lower, and the failure voltage and current points closely follow an iso-power curve. This behavior confirms that,

in the on-state, the reliability is limited by the power dissipation that the device can withstand. These assumptions are confirmed by the results of a scanning electron microscope (SEM) inspection (Figure 94 (c), for a device failed after testing in ON-state, and Figure 94 (d), for a device tested in OFF-state). The energy-dispersive X-ray spectroscopy (EDX) analysis in correspondence of the failure points (red crosses in Figure 94 (c-d)) is reported in Figure 94 (b). The failed region of the device tested in ON-state has a high gallium and aluminum content, possibly originated by the melting of the barrier and channel layers. The crack in the device tested in OFF-state has a lower gallium ad aluminum concentration, since the GaN-based layers are separated side-by-side, and a high silicon signal, because the electron beam is able to reach a larger part of the silicon substrate through the crack [575], [576].







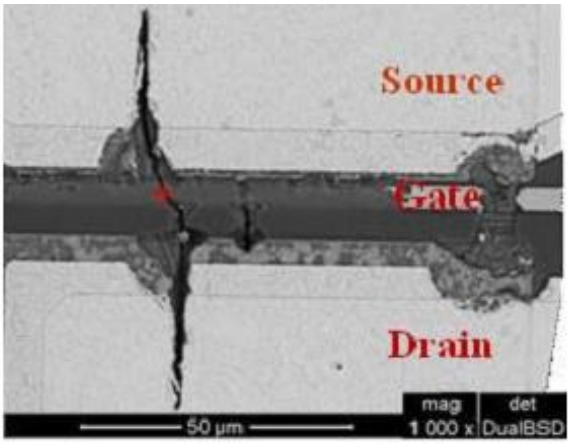


Figure 94: (a) failure caused by critical electric field and power dissipation in a device submitted to drain ESD discharges at various gate voltages. EDX measurements in (b) of the failed region in a device failed due to (c) power dissipation and (d) electric field confirm the driving force of the failure. [575], [576]

9.5 Radiation hardness

Owing to their very high operating limits and reliability, GaN-based devices are attractive for a wide range of special uses in extreme ambient conditions, such as space applications. In order to be a viable option, their robustness against radiation doses has to be analyzed and confirmed. Different types of irradiation can lead to different effects, therefore in the following we will analyze each of them separately. For an interested reader, an extensive discussion can be found in recent reviews [577]–[579].

9.5.1 Proton irradiation

The irradiation with protons can cause a wide range of effects in GaN-based devices, which can be related to the creation of new defects (or to the increase in concentration of pre-existing ones) caused by the interaction between the crystal lattice and the energetic protons.

The increase in defect concentration leads to a lowering of the mobility of the material, due to the scattering between the carriers and the defects, and to a reduction in carrier density, caused by the charge trapping in the defects and by the corresponding electrostatic effects. On the final devices, this corresponds to an increase in on-resistance, a positive shift in the threshold voltage, a reduction in the saturation current and in the peak transconductance value. The larger defect concentration causes a worsening of the dynamic behavior, due to increased density of states available for the trapping of charge.

In some cases, the dynamic R_{ON} is found to be decreased rather than increased by the proton irradiation [580]: on irradiated devices an increase in off-state leakage is observed, indicating an increase in the unintentionally-doped GaN layer conductivity. This conductivity increase leads to an increased deionization rate, thus reducing the dynamic on-resistance.[580]

The level of damage depends on the energy of the protons, and it is found to be higher for lower energy [581], [582]. This behavior may seem unexpected, but is related to the larger non-ionizing energy loss of the lower energy particles in the barrier and channel region, whereas higher energy protons cause damage deeper in the device structure. Concerning the number of irradiated protons, a typical threshold value (at 1.8 MeV) for the variation in device performance is a fluence of 10^{12}-10^{13} p^+/cm^2 at 1.8 MeV[583]–[585], 5×10^9 p^+/cm^2 at 40 MeV[586]. Based on the energy dependence discussed above, the lower threshold fluence at higher energy is unexpected, and may be related to different device structure and quality in the various papers. It is worth pointing out that values for variation in dynamic performance may be lower than the ones reported for variation in DC characteristics[587].

Specific defects created by proton irradiation include both deep donor and deep acceptor levels, as well as de-hydrogenation and reconfiguration of O_N-H complexes.[588], [589]

Most of the degradation caused by proton irradiation is related to displacement damage and is recoverable by high temperature annealing.[590], [591]

9.5.2 Neutron irradiation

Neutron irradiation produces two main effects: an increase in threshold voltage and a decrease in the material mobility. The threshold voltage variation originates from the increase in concentration of pre-existing acceptor states in the barrier, and the amount of variation increases linearly with the neutron fluence. [577]–[579] The cause of the lower material mobility is attributed to barrier acceptors too, which cause local threshold voltage and channel density variations and, therefore, additional scattering.

In general, neutrons are found to be less damaging than protons, both in terms of ON-resistance and breakdown voltage,[588] but cause extended damage rather than the creation of point defects found by other irradiation species.[577]

9.5.3 Electron irradiation

The main effect of electron irradiation is to cause a negative threshold voltage shift at lower fluence, which becomes positive at higher fluence, originated by the generation of traps with different charge states. Additionally, a monotonic decrease in channel mobility has been reported. The defects responsible for these variations have been extensively studied, and include nitrogen vacancies and additional traps with 0.3 eV, 0.45 eV, 0.55 eV and 0.8 eV activation energy.[578]

9.5.4 Gamma ray irradiation

The irradiation with gamma rays is less tested, but some information is available from the literature. Reported effects include increase in ON-resistance, negative shift in threshold voltage, increased saturation current, decreased gate current and increased reverse breakdown voltage[592]. The generated defects are supposed to be nitrogen vacancies (V_N), which act as donors in gallium nitride. Conflicting results have been reported, indicating instead a reduction in current[593], [594]. The difference may originate from different device structure and quality, or from the impact of different dose levels, showing improvements at lower dose and damage at high dose.[595]

9.5.5 Other ionizing species

Additional ionizing species have been tested on gallium nitride devices, including helium and carbon.[596] Effects include increase in ON-resistance, positive shift in threshold voltage and

reduction in saturation current, linearly proportional to the fluence, with no influence of the particle mass or energy. No variation in gate leakage was found.

10 Conclusions

In summary, with this tutorial paper we reviewed the properties and advantages of gallium nitride, and the characteristics, technology and reliability of GaN-based transistors. These devices are expected to play a significant role in next-generation power converters: competition with silicon and silicon carbide is expected to become stronger and stronger in the coming years. A substantial improvement in device technology will be possible through extensive research, both at academic and industrial levels.

If on one hand current GaN transistors can significantly improve the performance and reliability of switching mode power converters, next-generation scaled devices will enable monolithic integration, thus paving the way for the fabrication of miniaturized and MHz-range power converters. Further competition with silicon and SiC will come from the development of vertical GaN transistors, which have a great potential for high power/high voltage applications, and can be fabricated on inexpensive and large substrates.

A deep understanding of material and device properties will allow to further extend the operating ranges of the devices, thus enabling robust kV-range operation (for large-size devices) and sub-microsecond switching (for scaled transistors). Finally, a deep knowledge of trapping and reliability-limiting processes will allow to push the devices to the limits, thus fully exploiting the competitive advantage of GaN, as a ground-breaking semiconductor for power electronics.

This paper provides a comprehensive overview on the properties of GaN and related devices, and can be used as a reference for researchers willing to enter this interesting and complex field, or looking for an update on the most recent advancements on device technology.

11 Acknowledgments

…

12 Reference

[1] T. Morita et al., “99.3% Efficiency of three-phase inverter for motor drive using GaN-based Gate Injection Transistors,” in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2011, 481–484, DOI: 10.1109/APEC.2011.5744640.

[2] D. Han et al., “Efficiency characterization and thermal study of GaN based 1 kW inverter,” in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, 2344–2350, DOI: 10.1109/APEC.2014.6803631.

[3] W. Zhang et al., “Evaluation and comparison of silicon and gallium nitride power transistors in LLC resonant converter,” in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, 1362–1366, DOI: 10.1109/ECCE.2012.6342657.

[4] E. Gurpinar et al., “Ultra-low inductance design for a GaN HEMT based 3L-ANPC inverter,” in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, 1–8, DOI: 10.1109/ECCE.2016.7855540.

[5] E. Gurpinar et al., “600 V normally-off p-gate GaN HEMT based 3-level inverter,” in *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, 2017, 621–626, DOI: 10.1109/IFEEC.2017.7992110.

[6] M.-X. He et al., “A 1-MHz GaN Converter with 4X Voltage Range *,” in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, 2349–2355, DOI: 10.1109/APEC.2019.8722186.

[7] “High-Efficiency, 1.6-kW High-Density GaN-Based 1-MHz CrM Totem-Pole PFC Converter Reference Design.” [Online]. Available: https://www.ti.com/lit/ug/tidudt3b/tidudt3b.pdf?ts=1598363960865&ref_url=https%253A%252F%252Fwww.google.com%252F.

[8] E. Aklimi et al., *IEEE J. Solid-State Circuits*, 52, 6, 1618–1627, 2017, DOI: 10.1109/JSSC.2017.2672986.

[9] A. Villarruel-Parra et al., “75 MHz discrete GaN based multi-level buck converter for

envelope tracking applications," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, 1553–1560, DOI: 10.1109/APEC.2019.8721823.

[10] X. Li et al., "GaN-on-SOI: Monolithically Integrated All-GaN ICs for Power Conversion," in *2019 IEEE International Electron Devices Meeting (IEDM)*, 2019, 4.4.1-4.4.4, DOI: 10.1109/IEDM19573.2019.8993572.

[11] Y. Yamashita et al., "Monolithically Integrated E-mode GaN-on-SOI Gate Driver with Power GaN-HEMT for MHz-Switching," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2018, 231–236, DOI: 10.1109/WiPDA.2018.8569057.

[12] X. Ding et al., *CES Trans. Electr. Mach. Syst.*, 3, 1, 54–64, 2019, DOI: 10.30941/CESTEMS.2019.00008.

[13] W. S. Tan et al., *Solid. State. Electron.*, 50, 3, 511–513, 2006, DOI: 10.1016/j.sse.2006.02.008.

[14] R. Cuerdo et al., *Phys. Status Solidi (c)*, 5, 6, 1971–1973, 2008, DOI: 10.1002/pssc.200778555.

[15] D. Maier et al., *IEEE Trans. Device Mater. Reliab.*, 10, 4, 427–436, 2010, DOI: 10.1109/TDMR.2010.2072507.

[16] "EPC2023 - Enhancement Mode Power Transistor." [Online]. Available: https://epc-co.com/epc/Products/eGaNFETsandICs/EPC2023.aspx.

[17] "EPC2012C - Enhancement Mode Power Transistor." [Online]. Available: https://epc-co.com/epc/Products/eGaNFETsandICs/EPC2012C.aspx.

[18] "EPC2108 - Enhancement Mode GaN Power Transistor Half Bridge with Integrated Synchronous Bootstrap." [Online]. Available: https://epc-co.com/epc/Products/eGaNFETsandICs/EPC2108.aspx.

[19] "650V SuperGaN® FET in TO-247 (source tab)." [Online]. Available: https://www.transphormusa.com/en/document/datasheet-tp65h035g4ws-650v-gan-fet/.

[20] "650V SuperGaN® FET in PQFN (source tab)." [Online]. Available:

https://www.transphormusa.com/en/document/datasheet-tp65h300g4lsg-2/.

[21] "IGT40R070D1 E8220 400V CoolGaN™ enhancement-mode Power Transistor." [Online]. Available: https://www.infineon.com/dgdl/Infineon-IGT40R070D1 E8220-DataSheet-v02_01-EN.pdf?fileId=5546d4626afcd350016b269dd8f34ec4.

[22] "IGT60R070D1 600V CoolGaN™ enhancement-mode Power Transistor." [Online]. Available: https://www.infineon.com/dgdl/Infineon-IGT60R070D1-DataSheet-v02_12-EN.pdf?fileId=5546d46265f064ff016686028dd56526.

[23] "Panasonic PGA26E06BA product standard." [Online]. Available: https://industrial.panasonic.com/content/data/SC/ds/ds4/PGA26E06BA_E.pdf.

[24] I. Hwang et al., "1.6kV, 2.9 mΩ cm2 normally-off p-GaN HEMT device," in *2012 24th International Symposium on Power Semiconductor Devices and ICs*, 2012, 41–44, DOI: 10.1109/ISPSD.2012.6229018.

[25] E. Dogmus et al., *Appl. Phys. Express*, 11, 3, 034102, 2018, DOI: 10.7567/APEX.11.034102.

[26] N. Herbecq et al., *Phys. Status Solidi (a)*, 213, 4, 873–877, 2016, DOI: 10.1002/pssa.201532572.

[27] S. Q. Zhou et al., *Appl. Phys. Lett.*, 86, 8, 081912, 2005, DOI: 10.1063/1.1868870.

[28] A. Dadgar et al., *New J. Phys.*, 9, 10, 389–389, 2007, DOI: 10.1088/1367-2630/9/10/389.

[29] D. Zhao et al., *J. Semicond.*, 39, 3, 033006, 2018, DOI: 10.1088/1674-4926/39/3/033006.

[30] Y. Cai et al., *Materials (Basel).*, 11, 10, 1968, 2018, DOI: 10.3390/ma11101968.

[31] H. Morkoc, "General Properties of Nitrides," 2008, ch. 1, 1–61.

[32] S. Keller et al., *Semicond. Sci. Technol.*, 29, 11, 113001, 2014, DOI: 10.1088/0268-1242/29/11/113001.

[33] J. L. Hudgins et al., *IEEE Trans. Power Electron.*, 18, 3, 907–914, 2003, DOI: 10.1109/TPEL.2003.810840.

[34] R. L. Coffie, "High Power High Frequency Transistors: A Material's Perspective," Springer

International Publishing, Cham, 2020, 5–41.

[35] D. Ueda, “Properties and Advantages of Gallium Nitride,” 2017, 1–26.

[36] B. J. Baliga, *IEEE Electron Device Lett.*, 10, 10, 455–457, 1989, DOI: 10.1109/55.43098.

[37] B. J. Baliga, *J. Appl. Phys.*, 53, 3, 1759–1764, 1982, DOI: 10.1063/1.331646.

[38] P. Murugapandiyan et al., *J. Sci. Adv. Mater. Devices*, 2, 4, 515–522, 2017, DOI: 10.1016/j.jsamd.2017.08.004.

[39] F. Yun et al., *J. Appl. Phys.*, 92, 8, 4837–4839, 2002, DOI: 10.1063/1.1508420.

[40] S. Kasap et al., Eds., *Springer Handbook of Electronic and Photonic Materials*. Cham: Springer International Publishing, 2017.

[41] I. Vurgaftman et al., *J. Appl. Phys.*, 89, 11, 5815–5875, 2001, DOI: 10.1063/1.1368156.

[42] Q. Guo et al., *Jpn. J. Appl. Phys.*, 33, Part 1, No. 5A, 2453–2456, 1994, DOI: 10.1143/JJAP.33.2453.

[43] W. Walukiewicz et al., *J. Cryst. Growth*, 269, 1, 119–127, 2004, DOI: 10.1016/j.jcrysgro.2004.05.041.

[44] F. Bernardini et al., *Phys. Rev. B*, 56, 16, R10024–R10027, 1997, DOI: 10.1103/PhysRevB.56.R10024.

[45] J. F. Nye, *Physical Properties of Crystals*. Oxford University Press, 1985.

[46] M. Posternak et al., *Phys. Rev. Lett.*, 64, 15, 1777–1780, 1990, DOI: 10.1103/PhysRevLett.64.1777.

[47] *Semiconductor Device Physics and Design*. Dordrecht: Springer Netherlands, 2007.

[48] O. Ambacher et al., *J. Appl. Phys.*, 87, 1, 334–344, 2000, DOI: 10.1063/1.371866.

[49] *Gallium Nitride Electronics*, 96. Berlin, Heidelberg: Springer Berlin Heidelberg, 2008.

[50] E. T. Yu et al., *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, 17, 4, 1742, 1999, DOI: 10.1116/1.590818.

[51] I. Vurgaftman et al., *J. Appl. Phys.*, 94, 6, 3675–3696, 2003, DOI: 10.1063/1.1600519.

[52] H. Morkoc et al., “Polarization in GaN Based Heterostructures and Heterojunction Field Effect Transistors (HFETs),” Springer US, Boston, MA, 2008, 373–466.

[53] G. D. O’Clock et al., *Appl. Phys. Lett.*, 23, 2, 55–56, 1973, DOI: 10.1063/1.1654804.

[54] O. Ambacher et al., *J. Appl. Phys.*, 85, 6, 3222–3233, 1999, DOI: 10.1063/1.369664.

[55] J. P. Ibbetson et al., *Appl. Phys. Lett.*, 77, 2, 250–252, 2000, DOI: 10.1063/1.126940.

[56] L. Gordon et al., *J. Phys. D. Appl. Phys.*, 43, 50, 505501, 2010, DOI: 10.1088/0022-3727/43/50/505501.

[57] T. Zhu et al., *Phys. Chem. Chem. Phys.*, 14, 27, 9558, 2012, DOI: 10.1039/c2cp40998d.

[58] H. Amano et al., *J. Lumin.*, 40–41, 121–122, 1988, DOI: 10.1016/0022-2313(88)90117-2.

[59] Y. Cao, “Epitaxial growth of III-nitride electronic devices,” 2019, 41–113.

[60] S. Khandelwal et al., *Solid. State. Electron.*, 76, 60–66, 2012, DOI: 10.1016/j.sse.2012.05.054.

[61] S. Kola et al., *IEEE Electron Device Lett.*, 9, 3, 136–138, 1988, DOI: 10.1109/55.2067.

[62] D. Delagebeaudeuf et al., *IEEE Trans. Electron Devices*, 29, 6, 955–960, 1982, DOI: 10.1109/T-ED.1982.20813.

[63] J. H. Davies, *The Physics of Low-dimensional Semiconductors*. Cambridge University Press, 1997.

[64] “Power MOSFET Basics.” [Online]. Available: https://www.infineon.com/dgdl/mosfet.pdf?fileId=5546d462533600a4015357444e913f4f.

[65] “Design considerations of GaN devices for improving powerconverter efficiency and density.” [Online]. Available: https://www.ti.com/lit/wp/slyy124/slyy124.pdf?ts=1598362572806&ref_url=https%253A%252F%252Fwww.google.com%252F.

[66] T. Heckel et al., “Characterization and application of 600 V normally-off GaN transistors in hard switching DC/DC converters,” in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC’s (ISPSD)*, 2014, 63–66, DOI:

10.1109/ISPSD.2014.6855976.

[67] K. J. Chen et al., *IEEE Trans. Electron Devices*, 64, 3, 779–795, 2017, DOI: 10.1109/TED.2017.2657579.

[68] X.-G. He et al., *Chinese Phys. B*, 24, 6, 067301, 2015, DOI: 10.1088/1674-1056/24/6/067301.

[69] A. Tanaka et al., *AIP Adv.*, 9, 9, 095002, 2019, DOI: 10.1063/1.5114866.

[70] M. Haeberlen et al., *J. Phys. Conf. Ser.*, 209, 012017, 2010, DOI: 10.1088/1742-6596/209/1/012017.

[71] D. Christy et al., *AIP Adv.*, 4, 10, 107104, 2014, DOI: 10.1063/1.4897338.

[72] L. Liu et al., *Mater. Sci. Eng. R Reports*, 37, 3, 61–127, 2002, DOI: 10.1016/S0927-796X(02)00008-6.

[73] R. Liu et al., *Appl. Phys. Lett.*, 83, 5, 860–862, 2003, DOI: 10.1063/1.1597749.

[74] A. Tajalli et al., *Materials (Basel).*, 13, 19, 4271, 2020, DOI: 10.3390/ma13194271.

[75] S. M. Cho et al., "AlGaN/GaN HFET grown on 6-inch diameter Si(111) substrates by MOCVD," in *Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials*, 2011, DOI: 10.7567/SSDM.2011.AL-7-3.

[76] A. Asgari et al., *Mater. Sci. Eng. C*, 26, 5–7, 898–901, 2006, DOI: 10.1016/j.msec.2005.09.002.

[77] X. Huang et al., "Evaluation and application of 600V GaN HEMT in cascode structure," in *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, 1279–1286, DOI: 10.1109/APEC.2013.6520464.

[78] X. Huang et al., *IEEE Trans. Power Electron.*, 29, 5, 2208–2219, 2014, DOI: 10.1109/TPEL.2013.2267804.

[79] G. Sorrentino et al., "GaN HEMT devices: Experimental results on normally-on, normally-off and cascode configuration," in *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, 2013, 816–821, DOI: 10.1109/IECON.2013.6699239.

[80] K. J. Chen et al., “Physics of fluorine plasma ion implantation for GaN normally-off HEMT technology,” in *2011 International Electron Devices Meeting*, 2011, 19.4.1-19.4.4, DOI: 10.1109/IEDM.2011.6131585.

[81] Z. Zhang et al., *IEEE Electron Device Lett.*, 36, 11, 1128–1131, 2015, DOI: 10.1109/LED.2015.2483760.

[82] C.-H. Wu et al., *IEEE J. Electron Devices Soc.*, 6, 893–899, 2018, DOI: 10.1109/JEDS.2018.2859769.

[83] W. Saito et al., *IEEE Trans. Electron Devices*, 53, 2, 356–362, 2006, DOI: 10.1109/TED.2005.862708.

[84] S. D. Burnham et al., *Phys. Status Solidi (c)*, 7, 7–8, 2010–2012, 2010, DOI: 10.1002/pssc.200983644.

[85] T. Oka et al., *IEEE Electron Device Lett.*, 29, 7, 668–670, 2008, DOI: 10.1109/LED.2008.2000607.

[86] O. Hilt et al., “Normally-off high-voltage p-GaN gate GaN HFET with carbon-doped buffer,” in *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, 2011, 239–242, DOI: 10.1109/ISPSD.2011.5890835.

[87] M. Meneghini et al., *Energies*, 10, 2, 153, 2017, DOI: 10.3390/en10020153.

[88] P. Fiorenza et al., *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, 35, 1, 01A101, 2017, DOI: 10.1116/1.4967306.

[89] G. Greco et al., *Nanoscale Res. Lett.*, 6, 1, 132, 2011, DOI: 10.1186/1556-276X-6-132.

[90] S. C. Kang et al., *Nanomaterials*, 10, 11, 2116, 2020, DOI: 10.3390/nano10112116.

[91] D. Bisi et al., “Influence of fluorine-based dry etching on electrical parameters of AlGaN/GaN-on-Si High Electron Mobility Transistors,” in *2013 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, 2013, 61–64, DOI: 10.1109/ESSDERC.2013.6818819.

[92] G. Greco et al., *Mater. Sci. Semicond. Process.*, 78, 96–106, 2018, DOI: 10.1016/j.mssp.2017.09.027.

[93] A. Lorenz et al., *Phys. Status Solidi (c)*, 6, S2, S996–S998, 2009, DOI: 10.1002/pssc.200880838.

[94] K. J. Chen et al., *Phys. Status Solidi (a)*, 208, 2, 434–438, 2011, DOI: 10.1002/pssa.201000631.

[95] M. Meneghini et al., *Electronics*, 5, 4, 14, 2016, DOI: 10.3390/electronics5020014.

[96] T. Fujii et al., *Jpn. J. Appl. Phys.*, 46, 1, 115–118, 2007, DOI: 10.1143/JJAP.46.115.

[97] T. Mori et al., *Appl. Phys. Lett.*, 69, 23, 3537–3539, 1996, DOI: 10.1063/1.117237.

[98] S. R. Bahl et al., "A New Approach to Validate GaN FET Reliability to Power-Line Surges Under Use-Conditions," in *2019 IEEE International Reliability Physics Symposium (IRPS)*, 2019, 1–4, DOI: 10.1109/IRPS.2019.8720479.

[99] Z. H. Liu et al., *Appl. Phys. Lett.*, 98, 11, 113506, 2011, DOI: 10.1063/1.3567927.

[100] S. Kato et al., *J. Cryst. Growth*, 298, 831–834, 2007, DOI: 10.1016/j.jcrysgro.2006.10.192.

[101] Y. C. Choi et al., *Semicond. Sci. Technol.*, 22, 5, 517–521, 2007, DOI: 10.1088/0268-1242/22/5/010.

[102] Y. C. Choi et al., "Effects of an Fe-doped GaN Buffer in AlGaN/GaN Power HEMTs on Si Substrate," in *2006 European Solid-State Device Research Conference*, 2006, 282–285, DOI: 10.1109/ESSDER.2006.307693.

[103] F. Medjdoub et al., *Appl. Phys. Express*, 4, 12, 124101, 2011, DOI: 10.1143/APEX.4.124101.

[104] I. Abid et al., *Micromachines*, 10, 10, 690, 2019, DOI: 10.3390/mi10100690.

[105] J.-H. Lee et al., *IEEE J. Electron Devices Soc.*, 6, 1179–1186, 2018, DOI: 10.1109/JEDS.2018.2872975.

[106] Xinhua Wang et al., *IEEE Trans. Electron Devices*, 61, 5, 1341–1346, 2014, DOI: 10.1109/TED.2014.2312232.

[107] X.-H. Ma et al., *Chinese Phys. B*, 24, 2, 027101, 2015, DOI: 10.1088/1674-1056/24/2/027101.

[108] S. Besendörfer et al., *J. Appl. Phys.*, 127, 1, 015701, 2020, DOI: 10.1063/1.5129248.

[109] G. Meneghesso et al., *Jpn. J. Appl. Phys.*, 53, 10, 100211, 2014, DOI: 10.7567/JJAP.53.100211.

[110] Y. C. Choi et al., *IEEE Trans. Electron Devices*, 53, 12, 2926–2931, 2006, DOI: 10.1109/TED.2006.885679.

[111] M. Meneghini et al., *IEEE Trans. Electron Devices*, 61, 12, 4070–4077, 2014, DOI: 10.1109/TED.2014.2364855.

[112] G. Verzellesi et al., *IEEE Electron Device Lett.*, 35, 4, 443–445, 2014, DOI: 10.1109/LED.2014.2304680.

[113] R. Kabouche et al., *Phys. Status Solidi (a)*, 217, 7, 1900687, 2020, DOI: 10.1002/pssa.201900687.

[114] P. Srivastava et al., *IEEE Electron Device Lett.*, 31, 8, 851–853, 2010, DOI: 10.1109/LED.2010.2050673.

[115] N. Herbecq et al., *Electron. Lett.*, 51, 19, 1532–1534, 2015, DOI: 10.1049/el.2015.1684.

[116] G. Pavlidis et al., *IEEE Electron Device Lett.*, 40, 7, 1060–1063, 2019, DOI: 10.1109/LED.2019.2915984.

[117] G. Pavlidis et al., "The thermal effects of substrate removal on GaN HEMTs using Raman Thermometry," in *Proceedings of the 15th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, ITherm 2016*, 2016, 1255–1260, DOI: 10.1109/ITHERM.2016.7517691.

[118] A. G. Baca et al., *J. Vac. Sci. Technol. A*, 38, 2, 020803, 2020, DOI: 10.1116/1.5129803.

[119] R. J. Kaplar et al., "III-Nitride ultra-wide-bandgap electronic devices," Academic Press Inc., 2019, 397–416.

[120] T. Razzak et al., *Int. J. High Speed Electron. Syst.*, 28, 1–2, 2019, DOI: 10.1142/S0129156419400093.

[121] I. Abid et al., "Remarkable Breakdown Voltage on AlN/AlGaN/AlN double

heterostructure," in *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, 2020, 2020-September, 310–312, DOI: 10.1109/ISPSD46842.2020.9170170.

[122] E. A. Douglas et al., *Phys. Status Solidi (a)*, 214, 8, 1600842, 2017, DOI: 10.1002/pssa.201600842.

[123] N. Yafune et al., *Jpn. J. Appl. Phys.*, 50, 10 PART 1, 100202, 2011, DOI: 10.1143/JJAP.50.100202.

[124] J. Y. Tsao et al., Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges.

[125] S. Bajaj et al., *Appl. Phys. Lett.*, 109, 13, 133508, 2016, DOI: 10.1063/1.4963860.

[126] L. Nela et al., *Nat. Electron.*, 4, 4, 284–290, 2021, DOI: 10.1038/s41928-021-00550-8.

[127] B. J. Baliga, *Semicond. Sci. Technol.*, 28, 7, 074011, 2013, DOI: 10.1088/0268-1242/28/7/074011.

[128] Y. Cao et al., *J. Cryst. Growth*, 323, 1, 529–533, 2011, DOI: 10.1016/j.jcrysgro.2010.12.047.

[129] S. Heikman et al., *J. Appl. Phys.*, 94, 8, 5321, 2003, DOI: 10.1063/1.1610244.

[130] T. Palacios et al., *IEEE Trans. Electron Devices*, 53, 3, 562–565, 2006, DOI: 10.1109/TED.2005.863767.

[131] J. Lei et al., *IEEE Electron Device Lett.*, 39, 2, 260–263, 2018, DOI: 10.1109/LED.2017.2783908.

[132] R. S. Howell et al., "The Super-Lattice Castellated Field Effect Transistor (SLCFET): A novel high performance Transistor topology ideal for RF switching," in *2014 IEEE International Electron Devices Meeting*, 2014, 11.5.1-11.5.4, DOI: 10.1109/IEDM.2014.7047033.

[133] K. Shinohara et al., "GaN-Based Multi-Channel Transistors with Lateral Gate for Linear and Efficient Millimeter-Wave Power Amplifiers," in *2019 IEEE MTT-S International Microwave Symposium (IMS)*, 2019, 1133–1135, DOI: 10.1109/MWSYM.2019.8700845.

[134] J. Chang et al., *IEEE Electron Device Lett.*, 40, 7, 1048–1051, 2019, DOI: 10.1109/LED.2019.2917285.

[135] C. Erine et al., *IEEE Electron Device Lett.*, 41, 3, 321–324, 2020, DOI: 10.1109/LED.2020.2967458.

[136] J. Ma et al., *Appl. Phys. Lett.*, 113, 24, 242102, 2018, DOI: 10.1063/1.5064407.

[137] J. Ma et al., *IEEE Electron Device Lett.*, 40, 2, 275–278, 2019, DOI: 10.1109/LED.2018.2887199.

[138] J. Ma et al., "1200 V Multi-Channel Power Devices with 2.8 Ω•mm ON-Resistance," in *2019 IEEE International Electron Devices Meeting (IEDM)*, 2019, 4.1.1-4.1.4, DOI: 10.1109/IEDM19573.2019.8993536.

[139] M. Xiao et al., *IEEE Electron Device Lett.*, 41, 8, 1177–1180, 2020, DOI: 10.1109/LED.2020.3005934.

[140] L. Nela et al., *IEEE Electron Device Lett.*, 42, 1, 86–89, 2021, DOI: 10.1109/LED.2020.3038808.

[141] H. Kawai et al., *Phys. Status Solidi (a)*, 214, 8, 1600834, 2017, DOI: 10.1002/pssa.201600834.

[142] T. Fujihira, *Jpn. J. Appl. Phys.*, 36, Part 1, No. 10, 6254–6262, 1997, DOI: 10.1143/JJAP.36.6254.

[143] F. Udrea et al., *IEEE Trans. Electron Devices*, 64, 3, 713–727, 2017, DOI: 10.1109/TED.2017.2658344.

[144] X. Zhou et al., *Appl. Phys. Lett.*, 115, 11, 112104, 2019, DOI: 10.1063/1.5109389.

[145] H. Huang et al., *Appl. Phys. Lett.*, 116, 10, 102103, 2020, DOI: 10.1063/1.5142855.

[146] Z. Li et al., *IEEE Trans. Electron Devices*, 60, 10, 3230–3237, 2013, DOI: 10.1109/TED.2013.2266544.

[147] H. Ishida et al., *IEEE Electron Device Lett.*, 29, 10, 1087–1089, 2008, DOI: 10.1109/LED.2008.2002753.

[148] H. Ishida et al., “GaN-based natural super junction diodes with multi-channel structures,” in *2008 IEEE International Electron Devices Meeting*, 2008, 1–4, DOI: 10.1109/IEDM.2008.4796636.

[149] A. Nakajima et al., *IEEE Electron Device Lett.*, 32, 4, 542–544, 2011, DOI: 10.1109/LED.2011.2105242.

[150] B. Song et al., “Design and optimization of GaN lateral polarization-doped super-junction (LPSJ): An analytical study,” in *2015 IEEE 27th International Symposium on Power Semiconductor Devices & IC’s (ISPSD)*, 2015, 273–276, DOI: 10.1109/ISPSD.2015.7123442.

[151] S.-W. Han et al., *IEEE Trans. Electron Devices*, 67, 1, 69–74, 2020, DOI: 10.1109/TED.2019.2953843.

[152] S.-W. Han et al., *IEEE Electron Device Lett.*, 41, 12, 1758–1761, 2020, DOI: 10.1109/LED.2020.3029619.

[153] “GaN HEMT – Gallium Nitride Transistor.” [Online]. Available: https://www.infineon.com/cms/en/product/power/gan-hemt-gallium-nitride-transistor/.

[154] “GS-065-150-1-D.” [Online]. Available: https://gansystems.com/gan-transistors/gs-065-150-1-d/.

[155] “Product Selector Guide for eGaN® FETs and ICs.” [Online]. Available: https://epc-co.com/epc/Products/eGaNFETsandICs.aspx.

[156] J. A. del Alamo et al., *Microelectron. Reliab.*, 49, 9–11, 1200–1206, 2009, DOI: 10.1016/j.microrel.2009.07.003.

[157] T. Ohki et al., “Reliability of GaN HEMTs: current status and future technology,” in *2009 IEEE International Reliability Physics Symposium*, 2009, 61–70, DOI: 10.1109/IRPS.2009.5173225.

[158] W. Saito, “Reliability of GaN-HEMTs for high-voltage switching applications,” in *2011 International Reliability Physics Symposium*, 2011, 4E.1.1-4E.1.5, DOI: 10.1109/IRPS.2011.5784510.

[159] G. Meneghesso et al., *IEEE Trans. Device Mater. Reliab.*, 8, 2, 332–343, 2008, DOI: 10.1109/TDMR.2008.923743.

[160] W. Zhang et al., "Evaluation of 600 V cascode GaN HEMT in device characterization and all-GaN-based LLC resonant converter," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, 3571–3578, DOI: 10.1109/ECCE.2013.6647171.

[161] X. Huang et al., *IEEE Trans. Power Electron.*, 29, 5, 2453–2461, 2014, DOI: 10.1109/TPEL.2013.2276127.

[162] Z. Liu et al., *IEEE Trans. Power Electron.*, 29, 4, 1977–1985, 2014, DOI: 10.1109/TPEL.2013.2264941.

[163] Yong Cai et al., *IEEE Electron Device Lett.*, 26, 7, 435–437, 2005, DOI: 10.1109/LED.2005.851122.

[164] B. Lu et al., *IEEE Electron Device Lett.*, 33, 3, 360–362, 2012, DOI: 10.1109/LED.2011.2179971.

[165] J. Ma et al., *IEEE Electron Device Lett.*, 38, 9, 1305–1308, 2017, DOI: 10.1109/LED.2017.2731799.

[166] J. Ma et al., *IEEE Electron Device Lett.*, 38, 3, 367–370, 2017, DOI: 10.1109/LED.2017.2661755.

[167] L. Nela et al., *IEEE Electron Device Lett.*, 40, 3, 439–442, 2019, DOI: 10.1109/LED.2019.2896359.

[168] "Semiconductors." [Online]. Available: https://www.hitachiabb-powergrids.com/offering/product-and-system/semiconductors.

[169] Y. Zhang et al., *Appl. Phys. Lett.*, 111, 16, 163506, 2017, DOI: 10.1063/1.4989599.

[170] K. Mochizuki et al., *Jpn. J. Appl. Phys.*, 52, 8S, 08JN22, 2013, DOI: 10.7567/JJAP.52.08JN22.

[171] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*. Boston, MA: Springer US, 2008.

[172] I. C. Kizilyalli et al., *IEEE Trans. Electron Devices*, 60, 10, 3067–3070, 2013, DOI: 10.1109/TED.2013.2266664.

[173] C. De Santi et al., *IEEE Electron Device Lett.*, 41, 9, 1300–1303, 2020, DOI: 10.1109/LED.2020.3009649.

[174] T. Maeda et al., *IEEE Electron Device Lett.*, 40, 6, 941–944, 2019, DOI: 10.1109/LED.2019.2912395.

[175] R. Kucharski et al., *J. Appl. Phys.*, 128, 5, 050902, 2020, DOI: 10.1063/5.0009900.

[176] S. T. Kim et al., *J. Cryst. Growth*, 194, 1, 37–42, 1998, DOI: 10.1016/S0022-0248(98)00551-X.

[177] H. Yamane et al., *Chem. Mater.*, 9, 2, 413–416, 1997, DOI: 10.1021/cm960494s.

[178] H. Yamane et al., *J. Cryst. Growth*, 186, 1–2, 8–12, 1998, DOI: 10.1016/S0022-0248(97)00480-6.

[179] R. Dwiliński et al., *J. Cryst. Growth*, 311, 10, 3015–3018, 2009, DOI: 10.1016/j.jcrysgro.2009.01.052.

[180] R. Dwiliński et al., *J. Cryst. Growth*, 310, 17, 3911–3916, 2008, DOI: 10.1016/j.jcrysgro.2008.06.036.

[181] H. Ohta et al., *Jpn. J. Appl. Phys.*, 57, 4S, 04FG09, 2018, DOI: 10.7567/JJAP.57.04FG09.

[182] H. Ohta et al., *IEEE Electron Device Lett.*, 36, 11, 1180–1182, 2015, DOI: 10.1109/LED.2015.2478907.

[183] Y. Zhang et al., *J. Phys. D. Appl. Phys.*, 51, 27, 273001, 2018, DOI: 10.1088/1361-6463/aac8aa.

[184] K. Grabianska et al., *Electronics*, 9, 9, 1342, 2020, DOI: 10.3390/electronics9091342.

[185] “Bulk GaN: from technology to market.” [Online]. Available: http://www.yole.fr/BulkGaN_Applications_Players.aspx#.X7z6MYhKhaQ.

[186] “12 Inch Silicon Wafers for Research & Development.” [Online]. Available: https://www.universitywafer.com/12-inch-silicon-wafers.html.

[187] “Silicon Wafer.” [Online]. Available: http://www.semiwafer.com/silicon-wafer.html.

[188] S. Raghavan et al., *J. Appl. Phys.*, 98, 2, 023514, 2005, DOI: 10.1063/1.1978991.

[189] M. Miyoshi et al., *Semicond. Sci. Technol.*, 31, 10, 105016, 2016, DOI: 10.1088/0268-1242/31/10/105016.

[190] S. Chowdhury, “GaN-on-GaN power device design and fabrication,” Elsevier, 2019, 209–248.

[191] I. C. Kizilyalli et al., *Microelectron. Reliab.*, 55, 9–10, 1654–1661, 2015, DOI: 10.1016/j.microrel.2015.07.012.

[192] I. C. Kizilyalli et al., *IEEE Trans. Electron Devices*, 62, 2, 414–422, 2015, DOI: 10.1109/TED.2014.2360861.

[193] Y. Hatakeyama et al., *IEEE Electron Device Lett.*, 32, 12, 1674–1676, 2011, DOI: 10.1109/LED.2011.2167125.

[194] J.-I. Chyi et al., *Solid. State. Electron.*, 44, 4, 613–617, 2000, DOI: 10.1016/S0038-1101(99)00183-5.

[195] A. . Zhang et al., *Solid. State. Electron.*, 44, 7, 1157–1161, 2000, DOI: 10.1016/S0038-1101(00)00059-9.

[196] X. A. Cao et al., *Appl. Phys. Lett.*, 87, 5, 053503, 2005, DOI: 10.1063/1.2001738.

[197] K. Nomoto et al., *Phys. Status Solidi (a)*, 208, 7, 1535–1537, 2011, DOI: 10.1002/pssa.201000976.

[198] I. C. Kizilyalli et al., *IEEE Electron Device Lett.*, 35, 2, 247–249, 2014, DOI: 10.1109/LED.2013.2294175.

[199] Y. Hatakeyama et al., *Jpn. J. Appl. Phys.*, 52, 2R, 028007, 2013, DOI: 10.7567/JJAP.52.028007.

[200] K. Fu et al., *Appl. Phys. Lett.*, 113, 23, 233502, 2018, DOI: 10.1063/1.5052479.

[201] H. Xing et al., *J. Appl. Phys.*, 97, 11, 113703, 2005, DOI: 10.1063/1.1914952.

[202] C. Matthews et al., “Switching characterization of vertical GaN PiN diodes,” in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2016, 135–138, DOI: 10.1109/WiPDA.2016.7799924.

[203] “Vertical Devices In Bulk GaN Drive Diode Performance To Near - Theoretical Limits.” [Online]. Available: http://www.how2power.com/article/2013/march/vertical-devices-in-bulk-gan-drive-diode-performance-to-near---theoretical-l-imits-.php.

[204] I. C. Kizilyalli et al., *IEEE Electron Device Lett.*, 35, 6, 654–656, 2014, DOI: 10.1109/LED.2014.2319214.

[205] Z. Hu et al., *Appl. Phys. Lett.*, 107, 24, 243501, 2015, DOI: 10.1063/1.4937436.

[206] K. Nomoto et al., “GaN-on-GaN p-n power diodes with 3.48 kV and 0.95 mΩ-cm2: A record high figure-of-merit of 12.8 GW/cm2,” in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, 9.7.1-9.7.4, DOI: 10.1109/IEDM.2015.7409665.

[207] Z. Hu et al., *IEEE Electron Device Lett.*, 38, 8, 1071–1074, 2017, DOI: 10.1109/LED.2017.2720747.

[208] M. Qi et al., *Appl. Phys. Lett.*, 107, 23, 232101, 2015, DOI: 10.1063/1.4936891.

[209] R. Yeluri et al., *Appl. Phys. Lett.*, 106, 18, 183502, 2015, DOI: 10.1063/1.4919866.

[210] H. Fu et al., *IEEE Electron Device Lett.*, 39, 7, 1018–1021, 2018, DOI: 10.1109/LED.2018.2837625.

[211] H. Fu et al., *IEEE Electron Device Lett.*, 38, 6, 763–766, 2017, DOI: 10.1109/LED.2017.2690974.

[212] K. Fu et al., *IEEE Electron Device Lett.*, 40, 11, 1728–1731, 2019, DOI: 10.1109/LED.2019.2941830.

[213] J. Wang et al., *IEEE Electron Device Lett.*, 39, 11, 1716–1719, 2018, DOI: 10.1109/LED.2018.2868560.

[214] J. Wang et al., *Appl. Phys. Lett.*, 113, 2, 023502, 2018, DOI: 10.1063/1.5035267.

[215] J. R. Dickerson et al., *IEEE Trans. Electron Devices*, 63, 1, 419–425, 2016, DOI:

10.1109/TED.2015.2502186.

[216] J. Lutz et al., “pin Diodes,” Springer International Publishing, Cham, 2018, 201–270.

[217] G. T. Dang et al., *IEEE Trans. Electron Devices*, 47, 4, 692–696, 2000, DOI: 10.1109/16.830981.

[218] M. Misra et al., *Appl. Phys. Lett.*, 76, 8, 1045–1047, 2000, DOI: 10.1063/1.125933.

[219] Y. Saitoh et al., *Appl. Phys. Express*, 3, 8, 081001, 2010, DOI: 10.1143/APEX.3.081001.

[220] M. Ueno et al., “Fast recovery performance of vertical GaN Schottky barrier diodes on low-dislocation-density GaN substrates,” in *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC’s (ISPSD)*, 2014, 309–312, DOI: 10.1109/ISPSD.2014.6856038.

[221] N. Tanaka et al., *Appl. Phys. Express*, 8, 7, 071001, 2015, DOI: 10.7567/APEX.8.071001.

[222] Y. Cao et al., *Appl. Phys. Lett.*, 108, 11, 112101, 2016, DOI: 10.1063/1.4943946.

[223] Y. Cao et al., *Appl. Phys. Lett.*, 108, 6, 062103, 2016, DOI: 10.1063/1.4941814.

[224] L. Sang et al., *Appl. Phys. Lett.*, 111, 12, 122102, 2017, DOI: 10.1063/1.4994627.

[225] K. Nagamatsu et al., *Jpn. J. Appl. Phys.*, 57, 10, 105501, 2018, DOI: 10.7567/JJAP.57.105501.

[226] A. Sandupatla et al., *AIP Adv.*, 9, 4, 045007, 2019, DOI: 10.1063/1.5087491.

[227] S. Abhinay et al., *Jpn. J. Appl. Phys.*, 59, 1, 010906, 2020, DOI: 10.7567/1347-4065/ab65cd.

[228] H. Fu et al., *Appl. Phys. Lett.*, 111, 15, 152102, 2017, DOI: 10.1063/1.4993201.

[229] S. Han et al., *IEEE Electron Device Lett.*, 39, 4, 572–575, 2018, DOI: 10.1109/LED.2018.2808684.

[230] S. Han et al., *IEEE Trans. Power Electron.*, 34, 6, 5012–5018, 2019, DOI: 10.1109/TPEL.2018.2876444.

[231] S. Han et al., *IEEE Electron Device Lett.*, 40, 7, 1040–1043, 2019, DOI:

10.1109/LED.2019.2915578.

[232] W.-F. Wang et al., *Chinese Phys. B*, 29, 4, 047305, 2020, DOI: 10.1088/1674-1056/ab7909.

[233] W. Li et al., *IEEE Trans. Electron Devices*, 64, 4, 1635–1641, 2017, DOI: 10.1109/TED.2017.2662702.

[234] Y. Zhang et al., *IEEE Electron Device Lett.*, 38, 8, 1097–1100, 2017, DOI: 10.1109/LED.2017.2720689.

[235] T. Hayashida et al., *Appl. Phys. Express*, 10, 6, 061003, 2017, DOI: 10.7567/APEX.10.061003.

[236] A. D. Koehler et al., *ECS J. Solid State Sci. Technol.*, 6, 1, Q10–Q12, 2017, DOI: 10.1149/2.0041701jss.

[237] Y. Zhang et al., "Novel GaN trench MIS barrier Schottky rectifiers with implanted field rings," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, 10.2.1-10.2.4, DOI: 10.1109/IEDM.2016.7838386.

[238] S. Chowdhury et al., *IEEE Electron Device Lett.*, 29, 6, 543–545, 2008, DOI: 10.1109/LED.2008.922982.

[239] D. Shibata et al., "1.7 kV/1.0 mΩcm 2 normally-off vertical GaN transistor on GaN substrate with regrown p-GaN/AlGaN/GaN semipolar gate structure," in *2016 IEEE International Electron Devices Meeting (IEDM)*, 2016, 10.1.1-10.1.4, DOI: 10.1109/IEDM.2016.7838385.

[240] I. Ben-Yaacov et al., *J. Appl. Phys.*, 95, 4, 2073–2078, 2004, DOI: 10.1063/1.1641520.

[241] T. J. Rodgers et al., *IEEE J. Solid-State Circuits*, 10, 5, 322–331, 1975, DOI: 10.1109/JSSC.1975.1050618.

[242] S. Chowdhury et al., *IEEE Electron Device Lett.*, 33, 1, 41–43, 2012, DOI: 10.1109/LED.2011.2173456.

[243] H. Nie et al., *IEEE Electron Device Lett.*, 35, 9, 939–941, 2014, DOI: 10.1109/LED.2014.2339197.

[244] D. Ji et al., *IEEE Trans. Electron Devices*, 64, 3, 805–808, 2017, DOI: 10.1109/TED.2016.2632150.

[245] D. Ji et al., *IEEE Electron Device Lett.*, 39, 6, 863–865, 2018, DOI: 10.1109/LED.2018.2828844.

[246] T. Oka et al., *Appl. Phys. Express*, 8, 5, 054101, 2015, DOI: 10.7567/APEX.8.054101.

[247] T. Oka et al., "Over 10 a operation with switching characteristics of 1.2 kV-class vertical GaN trench MOSFETs on a bulk GaN substrate," in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, 459–462, DOI: 10.1109/ISPSD.2016.7520877.

[248] H. Otake et al., *Jpn. J. Appl. Phys.*, 46, No. 25, L599–L601, 2007, DOI: 10.1143/JJAP.46.L599.

[249] H. Otake et al., *Appl. Phys. Express*, 1, 1, 011105, 2008, DOI: 10.1143/APEX.1.011105.

[250] M. Kodama et al., *Appl. Phys. Express*, 1, 021104, 2008, DOI: 10.1143/APEX.1.021104.

[251] T. Oka et al., *Appl. Phys. Express*, 7, 2, 021002, 2014, DOI: 10.7567/APEX.7.021002.

[252] T. Oka et al., "100 A Vertical GaN Trench MOSFETs with a Current Distribution Layer," in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2019, 303–306, DOI: 10.1109/ISPSD.2019.8757621.

[253] M. Ruzzarin et al., *Microelectron. Reliab.*, 114, 113828, 2020, DOI: 10.1016/j.microrel.2020.113828.

[254] C. Gupta et al., *IEEE Electron Device Lett.*, 38, 3, 353–355, 2017, DOI: 10.1109/LED.2017.2649599.

[255] D. Ji et al., "Demonstrating >1.4 kV OG-FET performance with a novel double field-plated geometry and the successful scaling of large-area devices," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017, 9.4.1-9.4.4, DOI: 10.1109/IEDM.2017.8268359.

[256] C. Gupta et al., *IEEE Electron Device Lett.*, 37, 12, 1601–1604, 2016, DOI: 10.1109/LED.2016.2616508.

[257] W. Li et al., *IEEE Trans. Electron Devices*, 65, 6, 2558–2564, 2018, DOI: 10.1109/TED.2018.2829125.

[258] W. Li et al., "600 V GaN vertical V-trench MOSFET with MBE regrown channel," in *2017 75th Annual Device Research Conference (DRC)*, 2017, 1–2, DOI: 10.1109/DRC.2017.7999414.

[259] Y. Zhang et al., "1200 V GaN vertical fin power field-effect transistors," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017, 9.2.1-9.2.4, DOI: 10.1109/IEDM.2017.8268357.

[260] M. Sun et al., *IEEE Electron Device Lett.*, 38, 4, 509–512, 2017, DOI: 10.1109/LED.2017.2670925.

[261] M. Ruzzarin et al., *IEEE Trans. Electron Devices*, 64, 8, 3126–3131, 2017, DOI: 10.1109/TED.2017.2716982.

[262] Y. Zhang et al., *IEEE Electron Device Lett.*, 1–1, 2018, DOI: 10.1109/LED.2018.2880306.

[263] M. F. Fatahilah et al., *Sci. Rep.*, 9, 1, 10301, 2019, DOI: 10.1038/s41598-019-46186-9.

[264] K. Strempel et al., *Semicond. Sci. Technol.*, 36, 1, 014002, 2021, DOI: 10.1088/1361-6641/abc5ff.

[265] M. Ruzzarin et al., *Appl. Phys. Lett.*, 117, 20, 203501, 2020, DOI: 10.1063/5.0027922.

[266] *IEEE Electron Device Lett.*, 35, 6, 618–620, 2014, DOI: 10.1109/LED.2014.2314637.

[267] Yuhao Zhang et al., *IEEE Trans. Electron Devices*, 62, 7, 2155–2161, 2015, DOI: 10.1109/TED.2015.2426711.

[268] "No Title." [Online]. Available: http://www.qromis.com/#thirdPage.

[269] H. Amano et al., *J. Phys. D. Appl. Phys.*, 51, 16, 163001, 2018, DOI: 10.1088/1361-6463/aaaf9d.

[270] A. Magnani et al., "Thermal resistance characterization of GaN power HEMTs on Si, SOI, and poly-AlN substrates," in *2020 21st International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems*

(EuroSimE), 2020, 1–6, DOI: 10.1109/EuroSimE48426.2020.9152656.

[271] A. Magnani et al., *Microelectron. Reliab.*, 118, 114061, 2021, DOI: 10.1016/j.microrel.2021.114061.

[272] X. Zou et al., *IEEE Electron Device Lett.*, 37, 5, 636–639, 2016, DOI: 10.1109/LED.2016.2548488.

[273] Y. Zhang et al., *IEEE Electron Device Lett.*, 38, 2, 248–251, 2017, DOI: 10.1109/LED.2016.2646669.

[274] S. Mase et al., *Appl. Phys. Express*, 9, 11, 111005, 2016, DOI: 10.7567/APEX.9.111005.

[275] Y. Zhang et al., *IEEE Electron Device Lett.*, 39, 5, 715–718, 2018, DOI: 10.1109/LED.2018.2819642.

[276] R. Abdul Khadar et al., *IEEE Electron Device Lett.*, 39, 3, 401–404, 2018, DOI: 10.1109/LED.2018.2793669.

[277] C. Liu et al., *IEEE Electron Device Lett.*, 39, 1, 71–74, 2018, DOI: 10.1109/LED.2017.2779445.

[278] R. A. Khadar et al., *IEEE Electron Device Lett.*, 40, 3, 443–446, 2019, DOI: 10.1109/LED.2019.2894177.

[279] W. Chen et al., "Monolithic integration of lateral field-effect rectifier with normally-off HEMT for GaN-on-Si switch-mode power supply converters," in *2008 IEEE International Electron Devices Meeting*, 2008, 1–4, DOI: 10.1109/IEDM.2008.4796635.

[280] P. Chyurlia et al., *Phys. Status Solidi (c)*, 8, 7–8, 2210–2212, 2011, DOI: 10.1002/pssc.201000914.

[281] W. Shaobing et al., *IEEE Trans. Electron Devices*, 63, 10, 3882–3886, 2016, DOI: 10.1109/TED.2016.2597244.

[282] J. Ma et al., *IEEE Electron Device Lett.*, 38, 12, 1704–1707, 2017, DOI: 10.1109/LED.2017.2761911.

[283] C. Liu et al., *IEEE Electron Device Lett.*, 39, 7, 1034–1037, 2018, DOI:

10.1109/LED.2018.2841959.

[284] K. Mukherjee et al., *Materials (Basel).*, 13, 21, 4740, 2020, DOI: 10.3390/ma13214740.

[285] K. Mukherjee et al., *Appl. Phys. Express*, 13, 2, 024004, 2020, DOI: 10.35848/1882-0786/ab6ddd.

[286] "JC-70 Wide Bandgap Power Electronic Conversion Semiconductors." [Online]. Available: https://www.jedec.org/committees/jc-70.

[287] "GUIDELINE FOR SWITCHING RELIABILITY EVALUATION PROCEDURES FOR GALLIUM NITRIDE POWER CONVERSION DEVICES." [Online]. Available: https://www.jedec.org/standards-documents/docs/jep18001.

[288] "DYNAMIC ON-RESISTANCE TEST METHOD GUIDELINES FOR GaN HEMT BASED POWER CONVERSION DEVICES, VERSION 1.0." [Online]. Available: https://www.jedec.org/standards-documents/docs/jep173.

[289] X. She et al., *IEEE Trans. Ind. Electron.*, 64, 10, 8193–8205, 2017, DOI: 10.1109/TIE.2017.2652401.

[290] M. J. Tadjer et al., *ECS J. Solid State Sci. Technol.*, 5, 2, P124–P127, 2016, DOI: 10.1149/2.0371602jss.

[291] M. Bockowski, *Appl. Phys. Lett.*, 115, 14, 142104, 2019, DOI: 10.1063/1.5116866.

[292] G. Koblmüller et al., *J. Appl. Phys.*, 107, 4, 043527, 2010, DOI: 10.1063/1.3285309.

[293] W. Götz et al., *Appl. Phys. Lett.*, 67, 18, 2666–2668, 1995, DOI: 10.1063/1.114330.

[294] W. Götz et al., *Appl. Phys. Lett.*, 69, 24, 3725–3727, 1996, DOI: 10.1063/1.117202.

[295] S. Nakamura et al., *Jpn. J. Appl. Phys.*, 31, Part 1, No. 5A, 1258–1266, 1992, DOI: 10.1143/JJAP.31.1258.

[296] S. Nakamura et al., *Jpn. J. Appl. Phys.*, 31, Part 2, No. 2B, L139–L142, 1992, DOI: 10.1143/JJAP.31.L139.

[297] J.-D. Hwang et al., *Appl. Surf. Sci.*, 253, 10, 4694–4697, 2007, DOI: 10.1016/j.apsusc.2006.10.026.

[298] C. Gupta et al., *Appl. Phys. Express*, 9, 12, 121001, 2016, DOI: 10.7567/APEX.9.121001.

[299] "No Title." [Online]. Available: http://www.qromis.com/.

[300] H. G. Grimmeiss, *Annu. Rev. Mater. Sci.*, 7, 1, 341–376, 1977, DOI: 10.1146/annurev.ms.07.080177.002013.

[301] "Defects," John Wiley & Sons, Inc., Hoboken, NJ, USA, 2005, 251–317.

[302] A. R. Peaker et al., *J. Appl. Phys.*, 123, 16, 161559, 2018, DOI: 10.1063/1.5011327.

[303] R. Vetury et al., *IEEE Trans. Electron Devices*, 48, 3, 560–566, 2001, DOI: 10.1109/16.906451.

[304] I. Daumiller et al., *IEEE Electron Device Lett.*, 22, 2, 62–64, 2001, DOI: 10.1109/55.902832.

[305] S. C. Binari et al., *IEEE Trans. Electron Devices*, 48, 3, 465–471, 2001, DOI: 10.1109/16.906437.

[306] G. Meneghesso et al., *IEEE Trans. Electron Devices*, 53, 12, 2932–2941, 2006, DOI: 10.1109/TED.2006.885681.

[307] M. Faqir et al., *IEEE Trans. Device Mater. Reliab.*, 8, 2, 240–247, 2008, DOI: 10.1109/TDMR.2008.922017.

[308] W. Saito et al., *IEEE Trans. Electron Devices*, 54, 8, 1825–1830, 2007, DOI: 10.1109/TED.2007.901150.

[309] D. Jin et al., *IEEE Trans. Electron Devices*, 60, 10, 3190–3196, 2013, DOI: 10.1109/TED.2013.2274477.

[310] D. Bisi et al., *IEEE Electron Device Lett.*, 35, 10, 1004–1006, 2014, DOI: 10.1109/LED.2014.2344439.

[311] M. Meneghini et al., *IEEE Trans. Electron Devices*, 62, 3, 782–787, 2015, DOI: 10.1109/TED.2014.2386391.

[312] S. Huang et al., *Jpn. J. Appl. Phys.*, 50, 110202, 2011, DOI: 10.1143/JJAP.50.110202.

[313] P. Lagger et al., “Towards understanding the origin of threshold voltage instability of AlGaN/GaN MIS-HEMTs,” in *2012 International Electron Devices Meeting*, 2012, 13.1.1-13.1.4, DOI: 10.1109/IEDM.2012.6479033.

[314] M. Ťapajna et al., *Appl. Phys. Lett.*, 102, 24, 243509, 2013, DOI: 10.1063/1.4811754.

[315] P. Lagger et al., *IEEE Electron Device Lett.*, 34, 9, 1112–1114, 2013, DOI: 10.1109/LED.2013.2272095.

[316] M. Van Hove et al., *IEEE Trans. Electron Devices*, 60, 10, 3071–3078, 2013, DOI: 10.1109/TED.2013.2274730.

[317] M. Meneghini et al., *IEEE Electron Device Lett.*, 37, 4, 474–477, 2016, DOI: 10.1109/LED.2016.2530693.

[318] A. Guo et al., *IEEE Trans. Electron Devices*, 64, 5, 2142–2147, 2017, DOI: 10.1109/TED.2017.2686840.

[319] G. Meneghesso et al., *IEEE Electron Device Lett.*, 30, 2, 100–102, 2009, DOI: 10.1109/LED.2008.2010067.

[320] M. Wang et al., *IEEE Electron Device Lett.*, 32, 4, 482–484, 2011, DOI: 10.1109/LED.2011.2105460.

[321] M. Asghar et al., *Mater. Sci. Eng. B*, 113, 3, 248–252, 2004, DOI: 10.1016/j.mseb.2004.09.001.

[322] Z.-Q. Fang et al., “Deep centers in as-grown and electron-irradiated n-GaN,” in *2000 International Semiconducting and Insulating Materials Conference. SIMC-XI (Cat. No.00CH37046)*, 35–42, DOI: 10.1109/SIM.2000.939193.

[323] D. C. Look et al., *J. Cryst. Growth*, 281, 1, 143–150, 2005, DOI: 10.1016/j.jcrysgro.2005.03.035.

[324] S. Belahsene et al., *Electronics*, 4, 4, 1090–1100, 2015, DOI: 10.3390/electronics4041090.

[325] M. Lee et al., *Sci. Rep.*, 9, 1, 7128, 2019, DOI: 10.1038/s41598-019-43583-y.

[326] I. Boturchuk et al., *Phys. Status Solidi (a)*, 215, 9, 1700516, 2018, DOI:

10.1002/pssa.201700516.

[327] A. Y. Polyakov et al., *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, 34, 4, 041216, 2016, DOI: 10.1116/1.4953347.

[328] Z. Zhang et al., *Appl. Phys. Lett.*, 106, 2, 022104, 2015, DOI: 10.1063/1.4905783.

[329] U. Honda et al., *Jpn. J. Appl. Phys.*, 51, 04DF04, 2012, DOI: 10.1143/JJAP.51.04DF04.

[330] Y. Tokuda, *ECS Trans.*, 75, 4, 39–49, 2016, DOI: 10.1149/07504.0039ecst.

[331] H. K. Cho et al., *J. Appl. Phys.*, 94, 3, 1485–1489, 2003, DOI: 10.1063/1.1586981.

[332] H. K. Cho et al., *J. Cryst. Growth*, 223, 1–2, 38–42, 2001, DOI: 10.1016/S0022-0248(00)00982-9.

[333] D. Kindl et al., *J. Appl. Phys.*, 105, 9, 093706, 2009, DOI: 10.1063/1.3122290.

[334] G. A. Umana-Membreno et al., *J. Electron. Mater.*, 37, 5, 569–572, 2008, DOI: 10.1007/s11664-007-0313-3.

[335] L. Stuchlikova et al., "Investigation of deep energy levels in heterostructures based on GaN by DLTS," in *The Eighth International Conference on Advanced Semiconductor Devices and Microsystems*, 2010, 135–138, DOI: 10.1109/ASDAM.2010.5666319.

[336] P. Hacke et al., *J. Appl. Phys.*, 76, 1, 304–309, 1994, DOI: 10.1063/1.357144.

[337] H. M. Chung et al., *Appl. Phys. Lett.*, 76, 7, 897–899, 2000, DOI: 10.1063/1.125622.

[338] S. Chen et al., *J. Appl. Phys.*, 112, 5, 053513, 2012, DOI: 10.1063/1.4748170.

[339] Y. Nakano, *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.*, 36, 2, 023001, 2018, DOI: 10.1116/1.5017867.

[340] G. A. Umana-Membreno et al., *Appl. Phys. Lett.*, 80, 23, 4354–4356, 2002, DOI: 10.1063/1.1483390.

[341] C. B. Soh et al., *J. Phys. Condens. Matter*, 16, 34, 6305–6315, 2004, DOI: 10.1088/0953-8984/16/34/027.

[342] Y. S. Park et al., *Appl. Phys. Lett.*, 97, 11, 112110, 2010, DOI: 10.1063/1.3491798.

[343] D. K. Johnstonea et al., *MRS Proc.*, 692, H2.7.1, 2001, DOI: 10.1557/PROC-692-H2.7.1.

[344] Z.-Q. Fang et al., *Appl. Phys. Lett.*, 72, 18, 2277–2279, 1998, DOI: 10.1063/1.121274.

[345] K. J. Choi et al., *Appl. Phys. Lett.*, 82, 8, 1233–1235, 2003, DOI: 10.1063/1.1557316.

[346] A. R. Arehart et al., *Phys. Status Solidi (c)*, 5, 6, 1750–1752, 2008, DOI: 10.1002/pssc.200778622.

[347] H. K. Cho et al., *J. Phys. D. Appl. Phys.*, 41, 15, 155314, 2008, DOI: 10.1088/0022-3727/41/15/155314.

[348] A. R. Arehart et al., *Appl. Phys. Lett.*, 96, 24, 242112, 2010, DOI: 10.1063/1.3453660.

[349] O. Gelhausen et al., *Phys. Rev. B*, 69, 12, 125210, 2004, DOI: 10.1103/PhysRevB.69.125210.

[350] Q. Deng et al., *J. Phys. D. Appl. Phys.*, 44, 34, 345101, 2011, DOI: 10.1088/0022-3727/44/34/345101.

[351] M. L. Nakarmi et al., *Appl. Phys. Lett.*, 94, 9, 091903, 2009, DOI: 10.1063/1.3094754.

[352] X. S. Nguyen et al., *Phys. Status Solidi (b)*, 253, 11, 2225–2229, 2016, DOI: 10.1002/pssb.201600364.

[353] A. Hierro et al., *Appl. Phys. Lett.*, 80, 5, 805–807, 2002, DOI: 10.1063/1.1445274.

[354] A. Y. Polyakov et al., *J. Appl. Phys.*, 95, 10, 5591–5596, 2004, DOI: 10.1063/1.1697616.

[355] E. Calleja et al., *Phys. Rev. B*, 55, 7, 4689–4694, 1997, DOI: 10.1103/PhysRevB.55.4689.

[356] Z. Zhang et al., *Appl. Phys. Lett.*, 100, 5, 052114, 2012, DOI: 10.1063/1.3682528.

[357] A. Hierro et al., *Appl. Phys. Lett.*, 77, 10, 1499–1501, 2000, DOI: 10.1063/1.1290042.

[358] T. A. Henry et al., *Appl. Phys. Lett.*, 100, 8, 082103, 2012, DOI: 10.1063/1.3687700.

[359] A. Armstrong et al., *Opt. Express*, 20, S6, A812, 2012, DOI: 10.1364/OE.20.00A812.

[360] Z.-Q. Fang et al., *Appl. Phys. Lett.*, 87, 18, 182115, 2005, DOI: 10.1063/1.2126145.

[361] K. Galiano et al., *J. Appl. Phys.*, 123, 22, 224504, 2018, DOI: 10.1063/1.5022806.

[362] X. D. Chen et al., *Appl. Phys. Lett.*, 82, 21, 3671–3673, 2003, DOI: 10.1063/1.1578167.

[363] A. Sasikumar et al., *IEEE Electron Device Lett.*, 33, 5, 658–660, 2012, DOI: 10.1109/LED.2012.2188710.

[364] T. Kogiso et al., *Jpn. J. Appl. Phys.*, 58, SC, SCCB36, 2019, DOI: 10.7567/1347-4065/ab0408.

[365] A. Y. Polyakov et al., *Mater. Sci. Eng. B*, 166, 3, 220–224, 2010, DOI: 10.1016/j.mseb.2009.11.030.

[366] C. D. Wang et al., *Appl. Phys. Lett.*, 72, 10, 1211–1213, 1998, DOI: 10.1063/1.121016.

[367] W. I. Lee et al., *Appl. Phys. Lett.*, 67, 12, 1721–1723, 1995, DOI: 10.1063/1.115028.

[368] M. Caesar et al., "Generation of traps in AlGaN/GaN HEMTs during RF-and DC-stress test," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, 2012, CD.6.1-CD.6.5, DOI: 10.1109/IRPS.2012.6241883.

[369] D. W. Cardwell et al., *Appl. Phys. Lett.*, 102, 19, 193509, 2013, DOI: 10.1063/1.4806980.

[370] M. Silvestri et al., *Appl. Phys. Lett.*, 102, 7, 073501, 2013, DOI: 10.1063/1.4793196.

[371] T. Aggerstam et al., *J. Electron. Mater.*, 36, 12, 1621–1624, 2007, DOI: 10.1007/s11664-007-0202-9.

[372] R. Heitz et al., *Phys. Rev. B*, 55, 7, 4382–4387, 1997, DOI: 10.1103/PhysRevB.55.4382.

[373] A. Sasikumar et al., "Direct correlation between specific trap formation and electric stress-induced degradation in MBE-grown AlGaN/GaN HEMTs," in *2012 IEEE International Reliability Physics Symposium (IRPS)*, 2012, 2C.3.1-2C.3.6, DOI: 10.1109/IRPS.2012.6241780.

[374] Z. Zhang et al., *Appl. Phys. Lett.*, 101, 15, 152104, 2012, DOI: 10.1063/1.4759037.

[375] I.-H. Lee et al., *Appl. Phys. Lett.*, 110, 19, 192107, 2017, DOI: 10.1063/1.4983556.

[376] *J. Appl. Phys.*, 124, 21, 215701, 2018, DOI: 10.1063/1.5057373.

[377] M. Huber et al., *Appl. Phys. Lett.*, 107, 3, 032106, 2015, DOI: 10.1063/1.4927405.

[378] W. Götz et al., *Appl. Phys. Lett.*, 68, 22, 3144–3146, 1996, DOI: 10.1063/1.115805.

[379] M. Kumar et al., *Mater. Res. Bull.*, 47, 6, 1306–1309, 2012, DOI: 10.1016/j.materresbull.2012.03.016.

[380] Y. Irokawa et al., *J. Appl. Phys.*, 97, 8, 083505, 2005, DOI: 10.1063/1.1863458.

[381] T. Tanaka et al., *Appl. Phys. Lett.*, 65, 5, 593–594, 1994, DOI: 10.1063/1.112309.

[382] H. Nakayama et al., *Jpn. J. Appl. Phys.*, 35, Part 2, No. 3A, L282–L284, 1996, DOI: 10.1143/JJAP.35.L282.

[383] M. Horita et al., *Appl. Phys. Express*, 13, 7, 071007, 2020, DOI: 10.35848/1882-0786/ab9e7c.

[384] K. Sharma et al., "Impact of the Location of Iron Buffer Doping on Trap Signatures in GaN HEMTs," in *2020 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMiC)*, 2020, 1–3, DOI: 10.1109/INMMiC46721.2020.9160114.

[385] J. L. Lyons et al., *Phys. Rev. B*, 89, 3, 035204, 2014, DOI: 10.1103/PhysRevB.89.035204.

[386] E. Kohn et al., *IEEE Trans. Microw. Theory Tech.*, 51, 2, 634–642, 2003, DOI: 10.1109/TMTT.2002.807687.

[387] W. S. Tan et al., *IEEE Electron Device Lett.*, 27, 1, 1–3, 2006, DOI: 10.1109/LED.2005.860383.

[388] M. Meneghini et al., *IEEE Trans. Power Electron.*, 29, 5, 2199–2207, 2014, DOI: 10.1109/TPEL.2013.2271977.

[389] M. Neuburger et al., *IEEE Electron Device Lett.*, 25, 5, 256–258, 2004, DOI: 10.1109/LED.2004.827283.

[390] G. Meneghesso et al., *Semicond. Sci. Technol.*, 28, 7, 074021, 2013, DOI: 10.1088/0268-1242/28/7/074021.

[391] B. M. Green et al., *IEEE Electron Device Lett.*, 21, 6, 268–270, 2000, DOI: 10.1109/55.843146.

[392] T. Kikkawa et al., “Surface-charge controlled AlGaN/GaN-power HFET without current collapse and gm dispersion,” in *International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224)*, 25.4.1-25.4.4, DOI: 10.1109/IEDM.2001.979574.

[393] N.-Q. Zhang et al., *IEEE Electron Device Lett.*, 21, 9, 421–423, 2000, DOI: 10.1109/55.863096.

[394] A. Chini et al., *Electron. Lett.*, 40, 1, 73, 2004, DOI: 10.1049/el:20040017.

[395] M. Meneghini et al., *Appl. Phys. Lett.*, 100, 23, 233508, 2012, DOI: 10.1063/1.4723848.

[396] D. Jin et al., *Microelectron. Reliab.*, 52, 12, 2875–2879, 2012, DOI: 10.1016/j.microrel.2012.08.023.

[397] I. Hwang et al., *IEEE Electron Device Lett.*, 34, 12, 1494–1496, 2013, DOI: 10.1109/LED.2013.2286173.

[398] I. Rossetto et al., *IEEE Trans. Electron Devices*, 64, 9, 3734–3739, 2017, DOI: 10.1109/TED.2017.2728785.

[399] M. Higashiwaki et al., *J. Appl. Phys.*, 108, 6, 063719, 2010, DOI: 10.1063/1.3481412.

[400] M. Matys et al., *J. Appl. Phys.*, 120, 22, 225305, 2016, DOI: 10.1063/1.4971409.

[401] E. Ber et al., *IEEE Trans. Electron Devices*, 66, 5, 2100–2105, 2019, DOI: 10.1109/TED.2019.2901869.

[402] B. Bakeroot et al., *J. Appl. Phys.*, 116, 13, 134506, 2014, DOI: 10.1063/1.4896900.

[403] M. Faqir et al., *Microelectron. Reliab.*, 50, 9–11, 1520–1522, 2010, DOI: 10.1016/j.microrel.2010.07.020.

[404] M. Grupen, *IEEE Trans. Electron Devices*, 66, 9, 3777–3783, 2019, DOI: 10.1109/TED.2019.2928536.

[405] M. J. Uren et al., *IEEE Trans. Electron Devices*, 53, 2, 395–398, 2006, DOI: 10.1109/TED.2005.862702.

[406] E. Bahat-Treidel et al., *IEEE Trans. Electron Devices*, 57, 11, 3050–3058, 2010, DOI: 10.1109/TED.2010.2069566.

[407] M. J. Uren et al., *IEEE Trans. Electron Devices*, 59, 12, 3327–3333, 2012, DOI: 10.1109/TED.2012.2216535.

[408] C. Zhou et al., *IEEE Electron Device Lett.*, 33, 8, 1132–1134, 2012, DOI: 10.1109/LED.2012.2200874.

[409] M. Wang et al., *IEEE Electron Device Lett.*, 35, 11, 1094–1096, 2014, DOI: 10.1109/LED.2014.2356720.

[410] A. Guo et al., "Negative-bias temperature instability of GaN MOSFETs," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, 2016, 4A-1-1-4A-1–6, DOI: 10.1109/IRPS.2016.7574526.

[411] D. Jin et al., "Total current collapse in high-voltage GaN MIS-HEMTs induced by Zener trapping," in *2013 IEEE International Electron Devices Meeting*, 2013, 6.2.1-6.2.4, DOI: 10.1109/IEDM.2013.6724572.

[412] M. J. Uren et al., *IEEE Trans. Electron Devices*, 64, 7, 2826–2834, 2017, DOI: 10.1109/TED.2017.2706090.

[413] N. Zagni et al., "Trap Dynamics Model Explaining the R ON Stress/Recovery Behavior in Carbon-Doped Power AlGaN/GaN MOS-HEMTs," in *2020 IEEE International Reliability Physics Symposium (IRPS)*, 2020, 1–5, DOI: 10.1109/IRPS45951.2020.9128816.

[414] J. Neugebauer et al., "Native defects and impurities in GaN," 1996, 25–44.

[415] P. B. Klein et al., *Appl. Phys. Lett.*, 79, 21, 3527–3529, 2001, DOI: 10.1063/1.1418452.

[416] Y.-F. Wu et al., *IEEE Electron Device Lett.*, 25, 3, 117–119, 2004, DOI: 10.1109/LED.2003.822667.

[417] A. Armstrong et al., *Appl. Phys. Lett.*, 88, 8, 082114, 2006, DOI: 10.1063/1.2179375.

[418] X. Li et al., *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, 33, 2, 021208, 2015, DOI: 10.1116/1.4914316.

[419] A. Armstrong et al., *J. Appl. Phys.*, 98, 5, 053704, 2005, DOI: 10.1063/1.2005379.

[420] A. F. Wright, *J. Appl. Phys.*, 92, 5, 2575–2585, 2002, DOI: 10.1063/1.1498879.

[421] J. L. Lyons et al., *Appl. Phys. Lett.*, 97, 15, 152108, 2010, DOI: 10.1063/1.3492841.

[422] M. Matsubara et al., *J. Appl. Phys.*, 121, 19, 195701, 2017, DOI: 10.1063/1.4983452.

[423] G. Meneghesso et al., "Threshold voltage instabilities in D-mode GaN HEMTs for power switching applications," in *2014 IEEE International Reliability Physics Symposium*, 2014, 6C.2.1-6C.2.5, DOI: 10.1109/IRPS.2014.6861109.

[424] A. Chini et al., *IEEE Trans. Electron Devices*, 63, 9, 3473–3478, 2016, DOI: 10.1109/TED.2016.2593791.

[425] V. Joshi et al., *IEEE Trans. Electron Devices*, 66, 1, 561–569, 2019, DOI: 10.1109/TED.2018.2878770.

[426] N. Zagni et al., *Microelectron. Reliab.*, 100–101, 113374, 2019, DOI: 10.1016/j.microrel.2019.06.066.

[427] N. Zagni et al., *Phys. Status Solidi (a)*, 217, 7, 1900762, 2020, DOI: 10.1002/pssa.201900762.

[428] N. Zagni et al., *J. Comput. Electron.*, 19, 4, 1555–1563, 2020, DOI: 10.1007/s10825-020-01573-8.

[429] A. Fariza et al., *Appl. Phys. Lett.*, 109, 21, 212102, 2016, DOI: 10.1063/1.4968823.

[430] I. Chatterjee et al., "Impact of buffer charge on the reliability of carbon doped AlGaN/GaN-on-Si HEMTs," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, 2016, 4A-4-1-4A-4–5, DOI: 10.1109/IRPS.2016.7574529.

[431] B. Rackauskas et al., *IEEE Trans. Electron Devices*, 65, 5, 1838–1842, 2018, DOI: 10.1109/TED.2018.2813542.

[432] M. Singh et al., *IEEE Trans. Electron Devices*, 65, 9, 3746–3753, 2018, DOI: 10.1109/TED.2018.2860902.

[433] C. Koller et al., *IEEE Trans. Electron Devices*, 65, 12, 5314–5321, 2018, DOI: 10.1109/TED.2018.2872552.

[434] C. Poblenz et al., *J. Vac. Sci. Technol. B Microelectron. Nanom. Struct.*, 22, 3, 1145, 2004,

DOI: 10.1116/1.1752907.

[435] A. Nardo et al., *Appl. Phys. Express*, 13, 7, 074003, 2020, DOI: 10.35848/1882-0786/ab9623.

[436] J. He et al., *IEEE Trans. Electron Devices*, 65, 8, 3185–3191, 2018, DOI: 10.1109/TED.2018.2850042.

[437] F. Sang et al., *Jpn. J. Appl. Phys.*, 54, 4, 044101, 2015, DOI: 10.7567/JJAP.54.044101.

[438] M. Ruzzarin et al., *Microelectron. Reliab.*, 100–101, 113488, 2019, DOI: 10.1016/j.microrel.2019.113488.

[439] A. G. Viey et al., *IEEE Trans. Electron Devices*, 68, 4, 2017–2024, 2021, DOI: 10.1109/TED.2021.3050127.

[440] G. L. Bilbro et al., *Electron. Lett.*, 42, 24, 1425, 2006, DOI: 10.1049/el:20062113.

[441] Hou-Yu-Wang et al., "Effects of the Fe-doped GaN buffer in AlGaN/GaN HEMTs on SiC substrate," in *2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2015, 645–648, DOI: 10.1109/EDSSC.2015.7285198.

[442] F. Iucolano et al., "Correlation between dynamic Rdsou transients and Carbon related buffer traps in AlGaN/GaN HEMTs," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, 2016, CD-2-1-CD-2-4, DOI: 10.1109/IRPS.2016.7574586.

[443] K. Tanaka et al., *Jpn. J. Appl. Phys.*, 52, 4S, 04CF07, 2013, DOI: 10.7567/JJAP.52.04CF07.

[444] D. Bisi et al., *Phys. Status Solidi (a)*, 212, 5, 1122–1129, 2015, DOI: 10.1002/pssa.201431744.

[445] G. Meneghesso et al., *Semicond. Sci. Technol.*, 31, 9, 093004, 2016, DOI: 10.1088/0268-1242/31/9/093004.

[446] N. Zagni et al., *IEEE Trans. Electron Devices*, 68, 2, 697–703, 2021, DOI: 10.1109/TED.2020.3045683.

[447] M. Meneghini et al., "Total suppression of dynamic-ron in AlGaN/GaN-HEMTs through proton irradiation," in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017,

33.5.1-33.5.4, DOI: 10.1109/IEDM.2017.8268492.

[448] P. Moens et al., “Impact of buffer leakage on intrinsic reliability of 650V AlGaN/GaN HEMTs,” in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, 35.2.1-35.2.4, DOI: 10.1109/IEDM.2015.7409831.

[449] S. Karboyan et al., *Microelectron. Reliab.*, 81, 306–311, 2018, DOI: 10.1016/j.microrel.2017.10.006.

[450] M. J. Uren et al., *IEEE Electron Device Lett.*, 35, 3, 327–329, 2014, DOI: 10.1109/LED.2013.2297626.

[451] M. Meneghini et al., *Mater. Sci. Semicond. Process.*, 78, 118–126, 2018, DOI: 10.1016/j.mssp.2017.10.009.

[452] M. Van Hove et al., *IEEE Electron Device Lett.*, 33, 5, 667–669, 2012, DOI: 10.1109/LED.2012.2188016.

[453] J. A. del Alamo et al., *IEEE Trans. Electron Devices*, 66, 11, 4578–4590, 2019, DOI: 10.1109/TED.2019.2931718.

[454] M. Hua et al., *IEEE Electron Device Lett.*, 39, 3, 413–416, 2018, DOI: 10.1109/LED.2018.2791664.

[455] A. G. Viey et al., “Investigation of nBTI degradation on GaN-on-Si E-mode MOSc-HEMT,” in *2019 IEEE International Electron Devices Meeting (IEDM)*, 2019, 4.3.1-4.3.4, DOI: 10.1109/IEDM19573.2019.8993588.

[456] M. Hua et al., *IEEE Trans. Electron Devices*, 65, 9, 3831–3838, 2018, DOI: 10.1109/TED.2018.2856998.

[457] M. Hua et al., “Reverse-bias stability and reliability of hole-barrier-free E-mode LPCVD-SiN<inf>x</inf>/GaN MIS-FETs,” in *2017 IEEE International Electron Devices Meeting (IEDM)*, 2017, 33.2.1-33.2.4, DOI: 10.1109/IEDM.2017.8268489.

[458] A. Guo et al., “Positive-bias temperature instability (PBTI) of GaN MOSFETs,” in *2015 IEEE International Reliability Physics Symposium*, 2015, 6C.5.1-6C.5.7, DOI: 10.1109/IRPS.2015.7112770.

[459] T.-L. Wu et al., *IEEE Trans. Electron Devices*, 63, 5, 1853–1860, 2016, DOI: 10.1109/TED.2016.2539341.

[460] L. Sayadi et al., *IEEE Trans. Electron Devices*, 65, 6, 2454–2460, 2018, DOI: 10.1109/TED.2018.2828702.

[461] I. Rossetto et al., *Microelectron. Reliab.*, 55, 9–10, 1692–1696, 2015, DOI: 10.1016/j.microrel.2015.06.130.

[462] J. K. Kaushik et al., *IEEE Trans. Electron Devices*, 60, 10, 3351–3357, 2013, DOI: 10.1109/TED.2013.2279158.

[463] P. Altuntas et al., "On the correlation between kink effect and effective mobility in InAlN/GaN HEMTs," in *2014 9th European Microwave Integrated Circuit Conference*, 2014, 88–91, DOI: 10.1109/EuMIC.2014.6997798.

[464] S. D. Nsele et al., *IEEE Trans. Electron Devices*, 60, 4, 1372–1378, 2013, DOI: 10.1109/TED.2013.2248158.

[465] X.-H. Ma et al., *Chinese Phys. B*, 23, 2, 027302, 2014, DOI: 10.1088/1674-1056/23/2/027302.

[466] B. Brar et al., "Impact ionization in high performance AlGaN/GaN HEMTs," in *Proceedings. IEEE Lester Eastman Conference on High Performance Devices*, 487–491, DOI: 10.1109/LECHPD.2002.1146791.

[467] H. Hirshy et al., *IEEE Trans. Electron Devices*, 65, 12, 5307–5313, 2018, DOI: 10.1109/TED.2018.2872513.

[468] A. Chini et al., *Microelectron. Reliab.*, 54, 9–10, 2222–2226, 2014, DOI: 10.1016/j.microrel.2014.07.085.

[469] O. Axelsson et al., *IEEE Trans. Electron Devices*, 63, 1, 326–332, 2016, DOI: 10.1109/TED.2015.2499313.

[470] R. Williams, *J. Appl. Phys.*, 37, 9, 3411–3416, 1966, DOI: 10.1063/1.1708872.

[471] C. T. Sah et al., *Solid. State. Electron.*, 13, 6, 759–788, 1970, DOI: 10.1016/0038-1101(70)90064-X.

[472] D. V. Lang, *J. Appl. Phys.*, 45, 7, 3023–3032, 1974, DOI: 10.1063/1.1663719.

[473] A. M. White et al., *J. Appl. Phys.*, 47, 7, 3230–3239, 1976, DOI: 10.1063/1.323120.

[474] A. Chantre et al., *Phys. Rev. B*, 23, 10, 5335–5359, 1981, DOI: 10.1103/PhysRevB.23.5335.

[475] A. Hierro et al., *Appl. Phys. Lett.*, 76, 21, 3064–3066, 2000, DOI: 10.1063/1.126580.

[476] Z. Zhang et al., *J. Appl. Phys.*, 118, 15, 155701, 2015, DOI: 10.1063/1.4933174.

[477] O. Mitrofanov et al., *Superlattices Microstruct.*, 34, 1–2, 33–53, 2003, DOI: 10.1016/j.spmi.2003.12.002.

[478] T. Mizutani et al., *Phys. Status Solidi (a)*, 200, 1, 195–198, 2003, DOI: 10.1002/pssa.200303464.

[479] T. Okino et al., *IEEE Electron Device Lett.*, 25, 8, 523–525, 2004, DOI: 10.1109/LED.2004.832788.

[480] A. R. Arehart et al., "Spatially-discriminating trap characterization methods for HEMTs and their application to RF-stressed AlGaN/GaN HEMTs," in *2010 International Electron Devices Meeting*, 2010, 20.1.1-20.1.4, DOI: 10.1109/IEDM.2010.5703396.

[481] D. Bisi et al., *IEEE Trans. Electron Devices*, 60, 10, 3166–3175, 2013, DOI: 10.1109/TED.2013.2279021.

[482] N. Modolo et al., *Semicond. Sci. Technol.*, 36, 1, 014001, 2021, DOI: 10.1088/1361-6641/abc456.

[483] D. Bisi et al., "High-voltage double-pulsed measurement system for GaN-based power HEMTs," in *2014 IEEE International Reliability Physics Symposium*, 2014, CD.11.1-CD.11.4, DOI: 10.1109/IRPS.2014.6861130.

[484] J. Joh et al., *IEEE Trans. Electron Devices*, 58, 1, 132–140, 2011, DOI: 10.1109/TED.2010.2087339.

[485] M. Tapajna et al., *IEEE Electron Device Lett.*, 31, 7, 662–664, 2010, DOI: 10.1109/LED.2010.2047092.

[486] G. Meneghesso et al., *IEEE Trans. Electron Devices*, 51, 10, 1554–1561, 2004, DOI:

10.1109/TED.2004.835025.

[487] A. Chini et al., “Experimental and numerical correlation between current-collapse and fe-doping profiles in GaN HEMTs,” in *2012 IEEE International Reliability Physics Symposium (IRPS)*, 2012, CD.2.1-CD.2.4, DOI: 10.1109/IRPS.2012.6241881.

[488] A. Chini et al., *IEEE Trans. Electron Devices*, 60, 10, 3176–3182, 2013, DOI: 10.1109/TED.2013.2278290.

[489] O. Mitrofanov et al., *J. Appl. Phys.*, 95, 11, 6414–6419, 2004, DOI: 10.1063/1.1719264.

[490] A. Chini et al., *Mater. Sci. Semicond. Process.*, 78, 127–131, 2018, DOI: 10.1016/j.mssp.2017.10.029.

[491] L. M. Terman, *Solid. State. Electron.*, 5, 5, 285–299, 1962, DOI: 10.1016/0038-1101(62)90111-9.

[492] C. N. Berglund, *IEEE Trans. Electron Devices*, ED-13, 10, 701–705, 1966, DOI: 10.1109/T-ED.1966.15827.

[493] H. Mazari et al., *J. New Technol. Mater.*, 8, 1, 97–101, 2018, DOI: 10.12816/0048929.

[494] E. H. Nicollian et al., *Bell Syst. Tech. J.*, 46, 6, 1055–1133, 1967, DOI: 10.1002/j.1538-7305.1967.tb01727.x.

[495] W. A. Hill et al., *Solid. State. Electron.*, 23, 9, 987–993, 1980, DOI: 10.1016/0038-1101(80)90064-7.

[496] A. Das et al., *AIP Adv.*, 2, 3, 032159, 2012, DOI: 10.1063/1.4750481.

[497] Z.-F. Zhu et al., *Chinese Phys. Lett.*, 34, 9, 097301, 2017, DOI: 10.1088/0256-307X/34/9/097301.

[498] L. Szaro, *J. Phys. E.*, 22, 7, 503–510, 1989, DOI: 10.1088/0022-3735/22/7/017.

[499] J. Schmitz et al., “Leakage current correction in quasi-static C-V measurements,” in *Proceedings of the 2004 International Conference on Microelectronic Test Structures (IEEE Cat. No.04CH37516)*, 179–181, DOI: 10.1109/ICMTS.2004.1309475.

[500] T. S. Lay et al., *Electron. Lett.*, 37, 9, 595, 2001, DOI: 10.1049/el:20010403.

[501] S.-B. Bae et al., *Microelectron. Eng.*, 109, 10–12, 2013, DOI: 10.1016/j.mee.2013.03.108.

[502] M. Cui et al., "Characterization of Transient Threshold Voltage Shifts in Enhancement- and Depletion-mode AlGaN/GaN Metal-Insulator-Semiconductor (MIS)-HEMTs," in *2018 IEEE International Conference on Electron Devices and Solid State Circuits (EDSSC)*, 2018, 1–2, DOI: 10.1109/EDSSC.2018.8487160.

[503] M. Miczek et al., *J. Appl. Phys.*, 103, 10, 104510, 2008, DOI: 10.1063/1.2924334.

[504] M. Capriotti et al., *J. Appl. Phys.*, 117, 2, 024506, 2015, DOI: 10.1063/1.4905945.

[505] B. L. Swenson et al., *J. Appl. Phys.*, 106, 6, 064902, 2009, DOI: 10.1063/1.3224852.

[506] B. Monemar, *Phys. Rev. B*, 10, 2, 676–681, 1974, DOI: 10.1103/PhysRevB.10.676.

[507] M. A. Reshchikov et al., *J. Appl. Phys.*, 97, 6, 061301, 2005, DOI: 10.1063/1.1868059.

[508] T. Ogino et al., *Jpn. J. Appl. Phys.*, 19, 12, 2395–2405, 1980, DOI: 10.1143/JJAP.19.2395.

[509] M. Julkarnain et al., *Opt. Mater. (Amst).*, 60, 481–486, 2016, DOI: 10.1016/j.optmat.2016.09.003.

[510] G. Santana et al., *Materials (Basel).*, 6, 3, 1050–1060, 2013, DOI: 10.3390/ma6031050.

[511] M. Meneghini et al., *Mater. Sci. Semicond. Process.*, 2017, DOI: 10.1016/J.MSSP.2017.10.009.

[512] R. Degraeve et al., *Microelectron. Reliab.*, 39, 10, 1445–1460, 1999, DOI: 10.1016/S0026-2714(99)00051-7.

[513] P. Moens et al., *Proc. ESSDERC 2015*, 64–67, 2015, DOI: 10.1109/ESSDERC.2015.7324714.

[514] Jiechen Wu et al., "Electrical characterization and reliability analysis of Al<inf>2</inf>O<inf>3</inf>/AlGaN/GaN MISH structure," in *2014 IEEE International Reliability Physics Symposium*, 2014, CD.6.1-CD.6.5, DOI: 10.1109/IRPS.2014.6861129.

[515] T. Wu et al., *2015 IEEE Int. Reliab. Phys. Symp.*, 4–9, 2015, DOI: 10.1109/IRPS.2015.7112769.

[516] S. Warnock et al., “Progressive breakdown in high-voltage GaN MIS-HEMTs,” in *2016 IEEE International Reliability Physics Symposium (IRPS)*, 2016, 4A-6-1-4A-6–6, DOI: 10.1109/IRPS.2016.7574531.

[517] K. Mukherjee et al., *IEEE Int. Reliab. Phys. Symp. Proc.*, 2020-April, 2–6, 2020, DOI: 10.1109/IRPS45951.2020.9129098.

[518] M. Ruzzarin et al., *Microelectron. Reliab.*, 88–90, June, 620–626, 2018, DOI: 10.1016/j.microrel.2018.06.044.

[519] M. Ťapajna et al., *Appl. Phys. Lett.*, 107, 19, 193506, 2015, DOI: 10.1063/1.4935223.

[520] I. Rossetto et al., *IEEE Trans. Electron Devices*, 63, 6, 2334–2339, 2016, DOI: 10.1109/TED.2016.2553721.

[521] T.-L. Wu et al., *IEEE Electron Device Lett.*, 36, 10, 1001–1003, 2015, DOI: 10.1109/LED.2015.2465137.

[522] I. Rossetto et al., *Microelectron. Reliab.*, 64, 547–551, 2016, DOI: 10.1016/j.microrel.2016.07.127.

[523] M. Meneghini et al., *Microelectron. Reliab.*, 58, 177–184, 2016, DOI: 10.1016/j.microrel.2015.11.026.

[524] J. He et al., “Temperature-Dependent Gate Degradation of p-GaN Gate HEMTs under Static and Dynamic Positive Gate Stress,” in *2019 31st International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2019, 295–298, DOI: 10.1109/ISPSD.2019.8757574.

[525] M. Meneghini et al., “Degradation of GaN-HEMTs with p-GaN Gate: Dependence on temperature and on geometry,” in *IEEE International Reliability Physics Symposium Proceedings*, 2017, 4B5.1-4B5.5, DOI: 10.1109/IRPS.2017.7936311.

[526] F. Masin et al., *Appl. Phys. Lett.*, 115, 5, 052103, 2019, DOI: 10.1063/1.5109301.

[527] J. He et al., *IEEE Trans. Electron Devices*, 66, 8, 3453–3458, 2019, DOI: 10.1109/TED.2019.2924675.

[528] I. C. Kizilyalli et al., *Microelectron. Reliab.*, 55, 9–10, 1654–1661, 2015, DOI:

10.1016/j.microrel.2015.07.012.

[529] E. Fabris et al., *Microelectron. Reliab.*, 88–90, 568–571, 2018, DOI: 10.1016/J.MICROREL.2018.06.041.

[530] K. Orita et al., *IEEE J. Quantum Electron.*, 48, 9, 1169–1176, 2012, DOI: 10.1109/JQE.2012.2203795.

[531] E. Zanoni et al., "Reliability of Gallium Nitride microwave transistors," in *2016 21st International Conference on Microwave, Radar and Wireless Communications (MIKON)*, 2016, 1–6, DOI: 10.1109/MIKON.2016.7492013.

[532] A. Chini et al., *Micromachines*, 5, 3, 570–582, 2014, DOI: 10.3390/mi5030570.

[533] M. Rzin et al., *Microelectron. Reliab.*, 88–90, 397–401, 2018, DOI: 10.1016/j.microrel.2018.07.122.

[534] D. Bisi et al., *IEEE Electron Device Lett.*, 36, 10, 1011–1014, 2015, DOI: 10.1109/LED.2015.2474116.

[535] M. Caesar et al., *IEEE Int. Reliab. Phys. Symp.*, 1–5, 2012, DOI: 10.1109/IRPS.2012.6241883.

[536] N. Moultif et al., *Microelectron. Reliab.*, 100–101, 113434, 2019, DOI: 10.1016/j.microrel.2019.113434.

[537] K. Tanaka et al., "Reliability of hybrid-drain-embedded gate injection transistor," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2017, 4B-2.1-4B–2.10, DOI: 10.1109/IRPS.2017.7936308.

[538] M. Ruzzarin et al., "Degradation of vertical GaN FETs under gate and drain stress," in *2018 IEEE International Reliability Physics Symposium (IRPS)*, 2018, 4B.1-1-4B.1-5, DOI: 10.1109/IRPS.2018.8353579.

[539] M. Meneghini et al., *IEEE Trans. Electron Devices*, 62, 8, 2549–2554, 2015, DOI: 10.1109/TED.2015.2446032.

[540] I. Rossetto et al., *IEEE Trans. Electron Devices*, 64, 1, 73–77, 2017, DOI: 10.1109/TED.2016.2623774.

[541] I. Rossetto et al., *IEEE Trans. Electron Devices*, 65, 4, 1303–1307, 2018, DOI: 10.1109/TED.2018.2802449.

[542] I. L. Guy et al., *Appl. Phys. Lett.*, 75, 26, 4133–4135, 1999, DOI: 10.1063/1.125560.

[543] M. A. der Maur et al., *IEEE Trans. Electron Devices*, 60, 10, 3142–3148, 2013, DOI: 10.1109/TED.2013.2267547.

[544] M. Power et al., "Reverse-biased induced mechanical stress in AlGaN/GaN power diodes," in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, 103–106, DOI: 10.1109/ISPSD.2016.7520788.

[545] J. Joh et al., "Mechanisms for Electrical Degradation of GaN High-Electron Mobility Transistors," in *2006 International Electron Devices Meeting*, 2006, 29, 4, 1–4, DOI: 10.1109/IEDM.2006.346799.

[546] J. Joh et al., "Impact of electrical degradation on trapping characteristics of GaN high electron mobility transistors," in *2008 IEEE International Electron Devices Meeting*, 2008, 1–4, DOI: 10.1109/IEDM.2008.4796725.

[547] J. Joh et al., *IEEE Electron Device Lett.*, 29, 4, 287–289, 2008, DOI: 10.1109/LED.2008.917815.

[548] C.-Y. Chang et al., *IEEE Trans. Device Mater. Reliab.*, 11, 1, 187–193, 2011, DOI: 10.1109/TDMR.2010.2103314.

[549] P. Makaram et al., *Appl. Phys. Lett.*, 96, 23, 233509, 2010, DOI: 10.1063/1.3446869.

[550] F. Gao et al., *Appl. Phys. Lett.*, 99, 22, 223506, 2011, DOI: 10.1063/1.3665065.

[551] F. Gao et al., *IEEE Trans. Electron Devices*, 61, 2, 437–444, 2014, DOI: 10.1109/TED.2013.2293114.

[552] M. M. Bajo et al., *Appl. Phys. Lett.*, 104, 22, 223506, 2014, DOI: 10.1063/1.4881637.

[553] D. Marcon et al., "A comprehensive reliability investigation of the voltage-, temperature- and device geometry-dependence of the gate degradation on state-of-the-art GaN-on-Si HEMTs," in *2010 International Electron Devices Meeting*, 2010, 20.3.1-20.3.4, DOI: 10.1109/IEDM.2010.5703398.

[554] P. Moens et al., *Tech. Dig. - Int. Electron Devices Meet. IEDM*, 2016-Febru, 35.2.1-35.2.4, 2015, DOI: 10.1109/IEDM.2015.7409831.

[555] C. De Santi et al., *IEEE Electron Device Lett.*, 37, 5, 611–614, 2016, DOI: 10.1109/LED.2016.2543805.

[556] M. Borga et al., *IEEE Trans. Electron Devices*, 64, 9, 3616–3621, 2017, DOI: 10.1109/TED.2017.2726440.

[557] M. Borga et al., *Microelectron. Reliab.*, 100–101, September, 113461, 2019, DOI: 10.1016/j.microrel.2019.113461.

[558] A. Tajalli et al., *Micromachines*, 11, 1, 2020, DOI: 10.3390/mi11010101.

[559] M. Borga et al., *IEEE Trans. Electron Devices*, 67, 2, 595–599, 2020, DOI: 10.1109/TED.2020.2964060.

[560] B. Rackauskas et al., *Microelectron. Reliab.*, 95, 48–51, 2019, DOI: 10.1016/J.MICROREL.2019.02.013.

[561] C. De Santi et al., *IEEE Electron Device Lett.*, 41, 9, 1300–1303, 2020, DOI: 10.1109/LED.2020.3009649.

[562] E. Fabris et al., *IEEE Trans. Electron Devices*, 66, 11, 4597–4603, 2019, DOI: 10.1109/TED.2019.2943014.

[563] M. Rzin et al., *Microelectron. Reliab.*, 100–101, 2019, DOI: 10.1016/j.microrel.2019.06.080.

[564] A. Sasikumar et al., *IEEE Int. Reliab. Phys. Symp. Proc.*, 1–6, 2012, DOI: 10.1109/IRPS.2012.6241780.

[565] A. Minetto et al., *IEEE Trans. Electron Devices*, 67, 11, 4602–4605, 2020, DOI: 10.1109/TED.2020.3025983.

[566] F. Yang et al., *IEEE Trans. Electron Devices*, 67, 3, 869–874, 2020, DOI: 10.1109/TED.2020.2968212.

[567] J. Joh et al., “Current collapse in GaN heterojunction field effect transistors for high-voltage

switching applications," in *2014 IEEE International Reliability Physics Symposium*, 2014, 6C.5.1-6C.5.4, DOI: 10.1109/IRPS.2014.6861112.

[568] N. Modolo et al., *Microelectron. Reliab.*, 114, 113830, 2020, DOI: 10.1016/j.microrel.2020.113830.

[569] A. Barbato et al., *IET Power Electron.*, 13, 11, 2390–2397, 2020, DOI: 10.1049/iet-pel.2019.1455.

[570] N. Modolo et al., *IEEE Electron Device Lett.*, 42, 5, 673–676, 2021, DOI: 10.1109/LED.2021.3067796.

[571] M. Meneghini et al., *IEEE Electron Device Lett.*, 33, 3, 375–377, 2012, DOI: 10.1109/LED.2011.2181815.

[572] J. Kuzmík et al., *Solid. State. Electron.*, 48, 2, 271–276, 2004, DOI: 10.1016/S0038-1101(03)00295-8.

[573] Shih-Hung Chen et al., *IEEE Trans. Device Mater. Reliab.*, 12, 4, 589–598, 2012, DOI: 10.1109/TDMR.2012.2217746.

[574] B. Shankar et al., "Unique ESD behavior and failure modes of AlGaN/GaN HEMTs," in *2016 IEEE International Reliability Physics Symposium (IRPS)*, 2016, EL-7-1-EL-7-5, DOI: 10.1109/IRPS.2016.7574608.

[575] I. Rossetto et al., *IEEE Trans. Electron Devices*, 62, 9, 2830–2836, 2015, DOI: 10.1109/TED.2015.2463713.

[576] C. De Santi et al., *IET Power Electron.*, 11, 4, 668–674, 2018, DOI: 10.1049/iet-pel.2017.0403.

[577] A. Y. Polyakov et al., *J. Mater. Chem. C*, 1, 5, 877–887, 2013, DOI: 10.1039/C2TC00039C.

[578] S. J. Pearton et al., *ECS J. Solid State Sci. Technol.*, 5, 2, Q35–Q60, 2016, DOI: 10.1149/2.0251602jss.

[579] A. Y. Polyakov et al., *Mater. Sci. Eng. R Reports*, 94, 1–56, 2015, DOI: 10.1016/j.mser.2015.05.001.

[580] A. Stockman et al., *IEEE Trans. Electron Devices*, 66, 1, 372–377, 2019, DOI: 10.1109/TED.2018.2881325.

[581] X. Hu et al., *IEEE Trans. Nucl. Sci.*, 51, 2, 293–297, 2004, DOI: 10.1109/TNS.2004.825077.

[582] L. Liu et al., *J. Vac. Sci. Technol. B, Nanotechnol. Microelectron. Mater. Process. Meas. Phenom.*, 31, 2, 022201, 2013, DOI: 10.1116/1.4788904.

[583] B. D. White et al., *IEEE Trans. Nucl. Sci.*, 50, 6, 1934–1941, 2003, DOI: 10.1109/TNS.2003.821827.

[584] Xinwen Hu et al., *IEEE Trans. Nucl. Sci.*, 50, 6, 1791–1796, 2003, DOI: 10.1109/TNS.2003.820792.

[585] A. P. Karmarkar et al., *IEEE Trans. Nucl. Sci.*, 51, 6, 3801–3806, 2004, DOI: 10.1109/TNS.2004.839199.

[586] B. Luo et al., *Appl. Phys. Lett.*, 79, 14, 2196–2198, 2001, DOI: 10.1063/1.1408606.

[587] B. Luo et al., *Solid. State. Electron.*, 47, 6, 1015–1020, 2003, DOI: 10.1016/S0038-1101(02)00468-9.

[588] M. P. King et al., *IEEE Trans. Nucl. Sci.*, 62, 6, 2912–2918, 2015, DOI: 10.1109/TNS.2015.2480071.

[589] J. Chen et al., *IEEE Trans. Nucl. Sci.*, 60, 6, 4080–4086, 2013, DOI: 10.1109/TNS.2013.2281771.

[590] B. Luo et al., *J. Electron. Mater.*, 31, 5, 437–441, 2002, DOI: 10.1007/s11664-002-0097-4.

[591] A. Goyal et al., *J. Appl. Phys.*, 117, 22, 225702, 2015, DOI: 10.1063/1.4922286.

[592] B. Luo et al., *Appl. Phys. Lett.*, 80, 4, 604–606, 2002, DOI: 10.1063/1.1445809.

[593] A. Yadav et al., *Radiat. Eff. Defects Solids*, 170, 5, 377–385, 2015, DOI: 10.1080/10420150.2015.1010170.

[594] C. Schwarz et al., *Appl. Phys. Lett.*, 102, 6, 062102, 2013, DOI: 10.1063/1.4792240.

[595] S. A. Vitusevich et al., *Phys. Status Solidi (a)*, 195, 1, 101–105, 2003, DOI: 10.1002/pssa.200306264.

[596] B. D. Weaver et al., *IEEE Trans. Nucl. Sci.*, 59, 6, 3077–3080, 2012, DOI: 10.1109/TNS.2012.2224371.