

75 nm Gate Length PHEMT With $f_{max} = 800$ GHz Using Asymmetric Gate Recess: RF and Noise Investigation

M. Samnoui, N. Wichmann, X. Wallart, C. Coinon, S. Lepilliet and S. Bollaert

Abstract—We report a high maximum frequency of oscillation (f_{max}) and a current-gain cutoff frequency (f_T) of 800 GHz and 260 GHz respectively with pseudomorphic high-electron mobility transistor (PHEMT), using an InGaAs/InAs composite channel and an asymmetric gate recess. This result was achieved with long gate length $L_G = 75$ nm. The RF Small Signal Equivalent Circuit (SSEC) was extracted up to 110 GHz. Moreover, noise parameters extraction gives a minimum noise figure (NF_{min}) of 0.8 dB (with associated gain $G_{ass} = 16$ dB) and 1.8 dB (with associated gain $G_{ass} = 11.6$ dB) at 40 GHz and 94 GHz respectively. In this study, the gate leakage current was considered in the SSEC of the transistor (g_{gr} and g_{dr}) and for extraction of the noise parameters.

Index Terms—Asymmetric gate recess, high-electron mobility transistor (HEMT), noise figure (NF), small-signal equivalent circuit (SSEC).

I. INTRODUCTION

HIGH electron-mobility transistors (HEMTs) technology, is the best candidate for low noise amplifier and Terahertz applications [1]. Due to their superior high-frequency characteristics InP-based HEMTs are very promising for millimeter-wave applications and image sensor systems [2]. InP based transistors have held the record in frequency response as assessed by the current-gain cutoff frequency f_T and the maximum oscillation frequency f_{max} . Currently, the record for f_T is 738 GHz [3], and f_{max} is 1.5 THz ($f_T = 610$ GHz) [4] with pseudomorphic-HEMTs (PHEMTs) on InP substrate. A minimum noise figure (NF_{min}) was reported less than 1 dB at 94 GHz with associated gain $G_{ass} = 8.9$ dB [5]. Moreover, Low Noise Amplifier (LNA) operated beyond 850 GHz and 1 THz was also demonstrated [6][4]. In fact, for the last 10 years, the strategy used to improve

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electrical performance of FETs was to reduce the gate length below 50 nm combined with epilayer engineering. This approach allows high cutoff frequencies and excellent transconductance with a record g_m of 3.1 mS/ μ m [4]. However, recently published papers report high f_{max} while keeping larger gate length $L_G = 75$ nm [7][8].

In this work, InGaAs/InAlAs PHEMT with InGaAs/InAs composite channel were fabricated on InP substrate with gate length of 75 nm with an asymmetric gate recess. This technique was reported in [9] [10]. The results achieved are $f_T = 260$ GHz and $f_{max} = 800$ GHz. Furthermore, this work describes the influence of the drain side recess L_{RD} on the f_{max} . Increase of the drain side recess L_{RD} improve the f_{max} due to the reduction of output conductance g_d and capacitance C_{gd} . Moreover, the noise characteristics are given to compare the results of this work with similar technologies.

II. PROCESS TECHNOLOGY

PHEMT epitaxial layers were grown on semi-insulating InP substrate by gas source molecular beam epitaxy (MBE). The layer structure (figure 1), from bottom to top, consists of an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ buffer layer, a bottom silicon-delta doped plane, an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ first spacer, an $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{InAs}/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ composite channel, an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ second spacer, a top silicon-delta doped plane, an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier, an InP etch-stop layer, and finally a thick

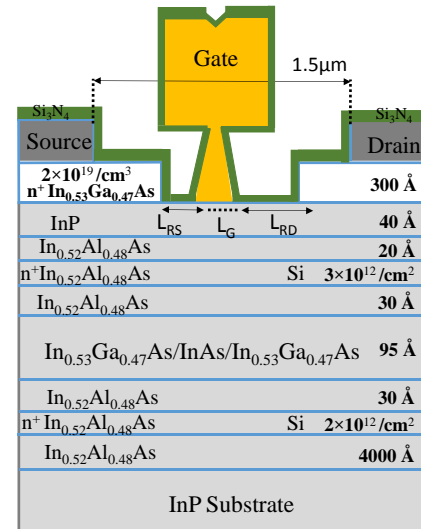


Fig. 1. Cross-section schematic of epitaxial layer structure.

In_{0.53}Ga_{0.47}As cap layer. The epilayer structure was optimized for high electron density and mobility in the channel.

To achieve high channel mobility, strained pure InAs layer was inserted in InGaAs channel. A highly doped thick cap layer was used to ensure low access resistance.

For PHEMT fabrication, electron beam lithography was used except for the mesa isolation, where standard optical lithography is sufficient. The first step of the fabrication was mesa isolation by wet chemical etching. The InGaAs cap layer was removed by Orthophosphoric acid based solution (H₃PO₄ solution). InP layer was then suppressed by Hydrochloric acid based solution (HCl-solution) followed by a second etching with H₃PO₄-solution to finish the mesa down to the InAlAs buffer layer. Next, Ohmic contact was realized as follow: after defining the Drain-Source with 1.5 μ m distance by e-beam lithography, Ti/Pt/Au metals was evaporated followed by thermal annealing. TLM measurement reports a low contact resistance (R_c) of 30 Ω . μ m. Next, the asymmetric recess was defined by e-beam lithography and the InGaAs cap layer was etched by H₃PO₄-solution down to the InP layer acting as an etch-stopped layer. The gate was then formed on InP layer by e-beam lithography [11] and evaporation of Ti/Pt/Au metals. Figure 1b, 1c gives some pictures of the PHEMT. Finally, the

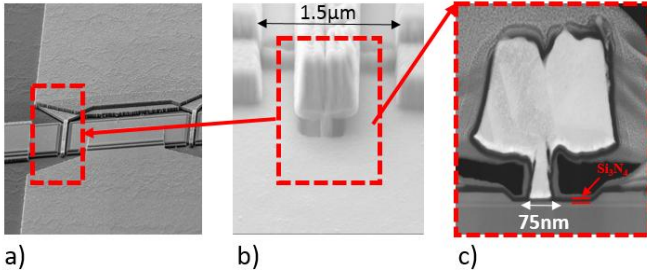


Fig. 2. a) and b) SEM Images of PHEMT c) FIB STEM image of PHEMT

sample was loaded into PECVD chamber where 30 nm-thick Si₃N₄ were deposited to form a passivation layer. This deposition is conformable and covers the sample mainly in the recess region (figure 1c) to further improve the access resistance.

To verify the electrical characteristics of the epilayer and the benefit of the Si₃N₄ passivation, Hall measurements were performed at room temperature on Hall bar at different steps of the process. Three samples were measured. Sample A consists on a Hall bar realized on the whole epilayer. On sample B, the

TABLE I
HALL MEASUREMENT EPILAYER AT DIFFERENT STEPS OF FABRICATION PROCESS

Sample	N_{Hall} (cm ⁻²)	μ_{Hall} (cm ² /V.s)	R_{\square} (Ω/\square)
A	2.4×10^{13}	4760	57
B	1.74×10^{12}	10325	346
C	2.65×10^{12}	12000	196

InGaAs cap layer was removed by wet chemical etching. On sample C, Hall bar without cap layer, was covered by 30 nm Si₃N₄ passivation layer formed by PECVD. In table 1, the Hall measurements are reported for the three samples at room temperature.

In sample A, the sheet carrier density is high and corresponds partly to the 2D electrons gas (2DEG) in the channel and mainly free electron in the n-doped cap layer. As the cap layer is highly doped, the mobility is low leading to poor Hall mobility.

In sample B, mobility is larger as it corresponds to the electron in the composite channel. However, the sheet carrier density is low.

To obtain a higher electron density, a Si₃N₄ passivation was used. Better electron density $N_{Hall} = 2.65 \times 10^{12}$ cm⁻² and mobility $\mu_{Hall} = 12000$ cm²/V.s are obtained with sample C. This Si₃N₄ layer reduces the surface potential and tends to improve the sheet electron density. Moreover, the mobility increases by better electron screening effect. This Si₃N₄ passivation allows the reduction of access resistance of our PHEMT since 2DEG channel electron concentration in the recessed area is improved.

III. DC AND RF CHARACTERIZATION

DC measurements of PHEMT with 75 nm gate length and an asymmetric recess ($L_{RS} = 65$ nm, $L_{RD} = 175$ nm) are given in figure 3 and 4. High current $I_D = 800$ mA/mm and extrinsic peak transconductance g_m of 1331 mS/mm are obtained at $V_{DS} = 0.8$ V (1V) and $V_{GS} = -0.3$ V. The drain and source resistances were estimated from DC-measurements $R_D + R_S = 430$ Ω . μ m, it can be also extracted from Small Signal Equivalent Circuit (SSEC) using a cold FET method [12] ($R_D = 242$ Ω . μ m and $R_S = 187$ Ω . μ m).

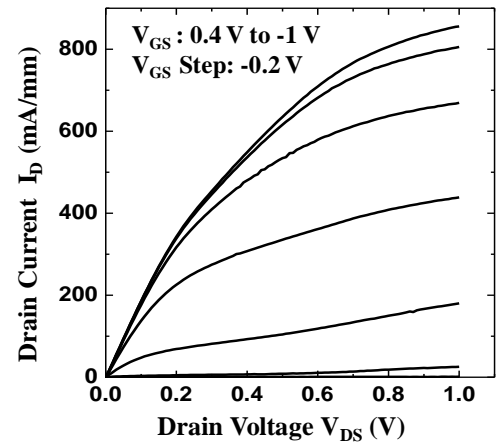


Fig. 3. Output Characteristics (I_D - V_{DS}) of the $L_G = 75$ nm and $W_G = 2 \times 12 \mu$ m PHEMT.

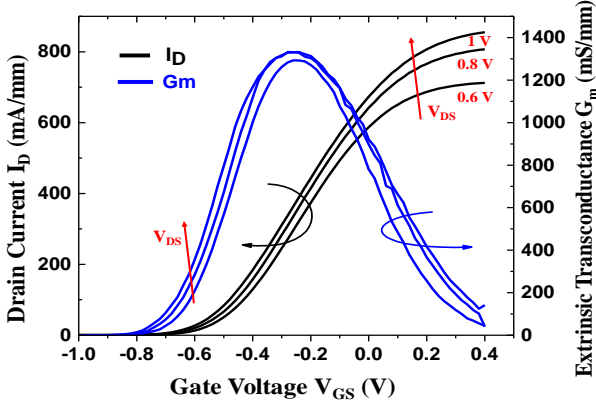


Fig. 4. Transfer and transconductance characteristics of the $L_G = 75\text{nm}$ and $W_G = 2 \times 12\mu\text{m}$ PHEMT.

S-Parameters were measured on PHEMT up to 110 GHz using a Rohde & Schwarz Vector Network Analyzer (VNA). Standard de-embedding method with open and short realized on the same wafer were used after Line-Reflect-Reflect-Match (LRRM) off-wafer calibration. The calculated (solid) and measured (dashed) short circuit current gain $|h_{21}|^2$ and unilateral Mason's power gain U are shown in figure 5. The extrapolation by (20 dB/decade) of $|h_{21}|^2$ and U gives $f_T = 260$ GHz and $f_{\max} = 800$ GHz at $V_{DS} = 1$ V and $V_{GS} = -0.08$ V. The extrapolated and calculated f_{\max} are similar and gives the same frequency. However, f_T has a 40 GHz of drift. Note that the calculated f_T and f_{\max} were plotted using the equivalent circuit parameters reported in table II. The extraction method of the SSEC will be shown in the part IV.

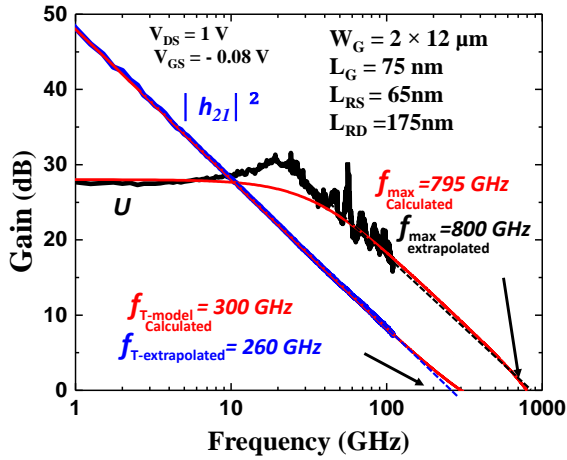


Fig. 5. Measured and simulated U and $|h_{21}|^2$ of PHEMT ($L_G = 75\text{nm}$, $W_G = 2 \times 12\mu\text{m}$, $L_{RS} = 56\text{nm}$ and $L_{RD} = 175\text{nm}$).

To understand the L_{RD} side recess dependency of f_{\max} , four devices were characterized up to 110 GHz. The source side recess was fixed at ~ 65 nm and L_{RD} varies from 70 nm to ~ 195 nm. The results are shown in figure 6. The symmetric devices, with $L_{RD} = L_{RS} \approx 65$ nm had a $f_{\max} = 520$ GHz. When the L_{RD} increased up to 195 nm, the unilateral gain value

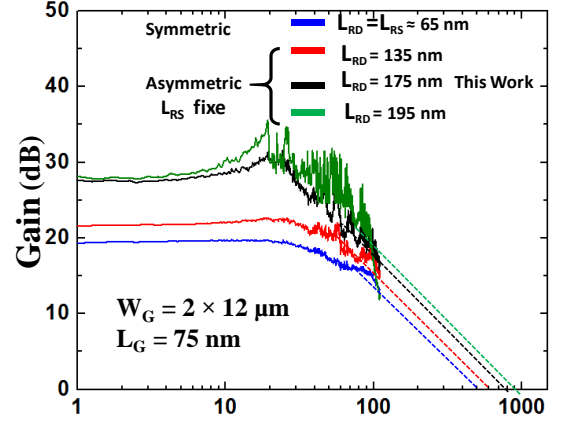


Fig. 6. Evolution of unilateral Mason's gain U versus drain side recess length L_{RD} . The source side recess L_{RS} is kept at 65nm.

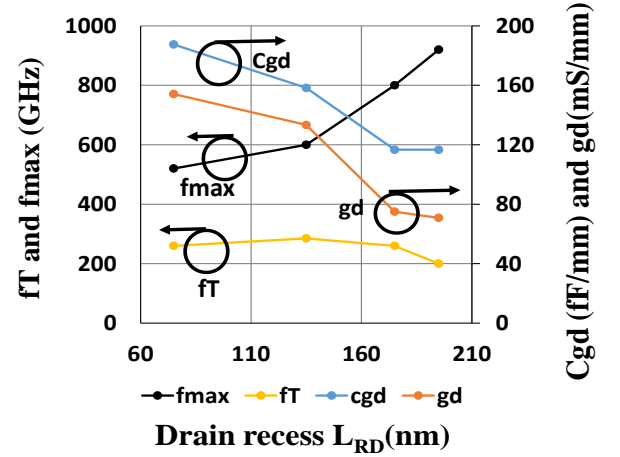


Fig. 7(a). Evolution of f_{\max} , C_{gd} and g_d and versus drain side recess L_{RD} . The source recess L_{RS} is kept at 65nm.

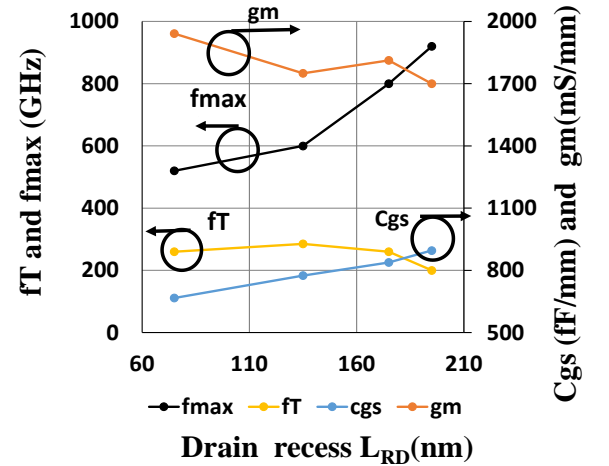


Fig. 7(b). Evolution of f_{\max} , C_{gs} and g_m versus drain side recess L_{RD} . The source side recess L_{RS} is kept at 65nm.

becomes more important in the whole frequency range. Therefore, increased unilateral gain is related to the improvement of the output conductance g_D and gate to drain capacitance C_{GD} of the transistor also shown in figure 7a. These two parameters help to improve the unilateral gain. This indicates that the electrical coupling between the gate and the drain is lower comparing to the coupling between the gate and the source [10].

TABLE II
EXTRACTED SMALL EQUIVALENT PARAMETERS OF PHEMT ($L_G = 75\text{NM}$
AND $W_G = 2 \times 12\mu\text{M}$)

Intrinsic	Values	Extrinsic	Values
g_m (mS)	43.5	R_g (Ω)	1.25
g_d (mS)	1.8	R_d (Ω)	10.1
C_{gs} (fF)	20.1	R_s (Ω)	7.8
C_{gd} (fF)	2.8	C_{pd} (fF)	2.8
C_{ds} (fF)	0.5	C_{pg} (fF)	1
R_i (Ω)	2.5	L_g (pH)	6
R_{gd} (Ω)	4	L_d (pH)	1
g_{df} (mS)	12×10^{-3}	L_s (pH)	3
g_{gf} (mS)	0.8×10^{-3}		

IV. SMALL SIGNAL EQUIVALENT CIRCUIT AND NOISE MEASUREMENT

In order to extract the four noise parameters of the transistor, NF_{50} method [13]–[16] has been used, in three different frequency bands 6 GHz – 20 GHz, 20 GHz – 42 GHz and W 75 GHz – 110 GHz. The method is based on noise figure measurement on 50 Ω (source and load) and a noise model. The noise model is composed of two temperatures uncorrelated noise sources (see figure 8) associated with the SSEC.

The setup description [15] of the measurement with NF_{50} method using Noise Figure Meter (NFM) gives the results shown in figure 9 with gate-to-source voltage V_{GS} from -0.5 V to 0.2 V and drain-to-source voltage $V_{DS} = 1$ V. The minimum NF_{50} is obtain at the optimal gate-to-source voltage $V_{GS_Opt} = -0.3$ V. At this bias, NF_{50} is 2.58 dB and 3.7 dB for 40 GHz and 94 GHz respectively.

To extract the four noise parameters, accurate SSEC is needed, as the extraction method of the four noise parameters [14] is based on the SSEC associated with two noise sources (figure 8). Standard cold FET method [12] was applied to extract the SSEC from S-parameters measurement using VNA in a 0.25 GHz – 110 GHz frequency range. To validate the SSEC, measured and simulated S-parameters are plotted in figure 10 at the biasing point corresponding to optimal of NF_{50} . The simulated S-parameters are defined by calculation using SSEC of figure 8 implemented on Advanced design System (ADS) software from Keysight technologies.

The noise model is based on two “uncorrelated” noise sources ($\overline{i_d e_g} = 0$) depending on input and output noise temperature (T_{in} and T_{out}). They are defined as follows [17][14]

$$T_{in} = \frac{\overline{e_g^2}}{4KRe(\frac{1}{Y_{11}}).\Delta f} \quad (1)$$

$$T_{out} = \frac{\overline{i_d^2}}{4KRe(\frac{1}{Z_{22}}).\Delta f} \quad (2)$$

Where K is the Boltzmann constant, Δf is the frequency bandwidth while $Re(\frac{1}{Y_{11}})$ and $Re(\frac{1}{Z_{22}})$ are the extrinsic Y and Z parameters constituted by the intrinsic SSEC to which is added the series resistances R_g , R_s , R_d and gate leakage conductance g_{gf} and g_{df} (red dashed line in figure 8). These conductances were added in the SSEC to fit the U gain at low frequency (see figure 5). These conductances g_{gf} and g_{df} are related to gate leakage. Indeed the Schottky contact used, Titanium (Ti) on InP, have more current leakage compare to others contacts [18].

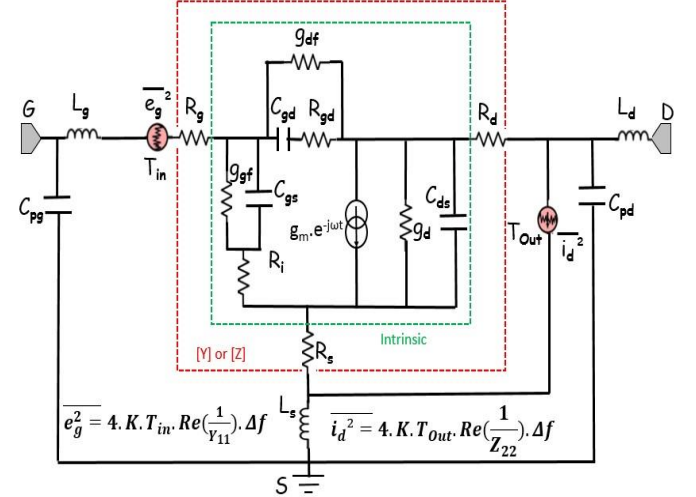


Fig. 8. PHEMT SSEC including two uncorrelated noise sources

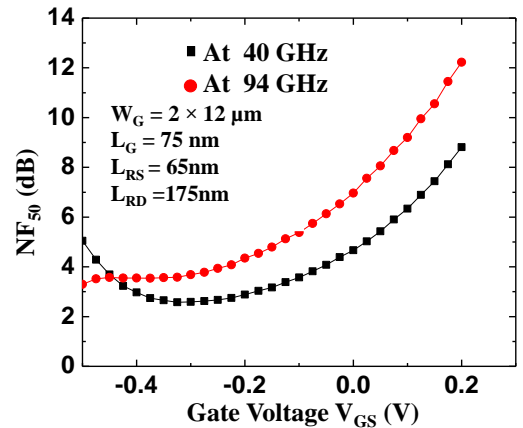


Fig. 9. NF_{50} measurement versus V_{GS} , measured at 40 GHz and 90GHz with $V_{DS} = 1$ V ($L_G = 75\text{nm}$, $W_G = 2 \times 12\mu\text{m}$, $L_{RS} = 65\text{nm}$ and $L_{RD} = 175\text{nm}$).

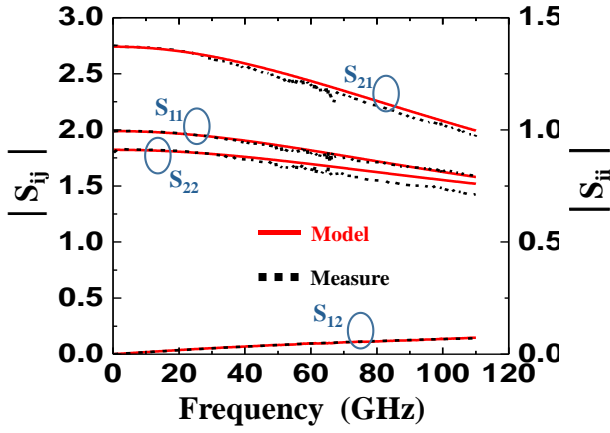


Fig. 10 (a). Measured and simulated S-parameters (magnitude) up to 110 GHz ($L_G = 75\text{nm}$, $W_G = 2 \times 12\ \mu\text{m}$, $L_{RS} = 56\text{nm}$ and $L_{RS} = 175\text{nm}$).

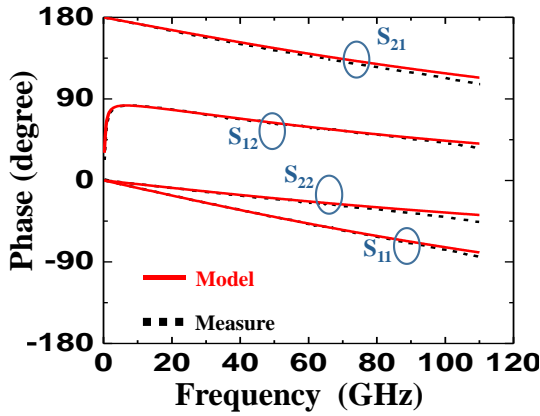


Fig. 10 (b). Measured and simulated S-parameters (Phase) up to 110 GHz ($L_G = 75\text{nm}$, $W_G = 2 \times 12\ \mu\text{m}$, $L_{RS} = 56\text{nm}$ and $L_{RS} = 175\text{nm}$).

To determine the four noise parameters of the transistor, comparison was achieved between measured NF_{50} and the calculated NF_{50} using noise model, under ADS software. The input noise temperature T_{in} is fixed at ambient temperature ($T_{in} = 293\text{K}$). The output noise temperature T_{out} is determined from the fitting of the noise figure measurement (NF_{50}) data and the noise model. In figure 11, the simulated NF_{50} was plotted in 6 GHz – 110 GHz frequency range in order to deduce the T_{out} as close as possible to the measure of NF_{50} .

These experimental and modeling studies show that the fitting needs to take into account the dispersion of NF_{50} measurements. There are several reasons for this significant dispersion: the setup bench and the influence of receiver noise and return losses on the noise measurements [14]. From this plot (see figure 11) a good agreement is observed, it is obvious to note that the simulated data are close as possible to the experimental ones from $T_{out} = 1200\text{K}$ to $T_{out} = 1600\text{K}$. The maximum error bars that we can have in extraction of the output noise temperature has been estimated at 400 K. Furthermore, an optimal temperature T_{out} is observed at 1350 K.

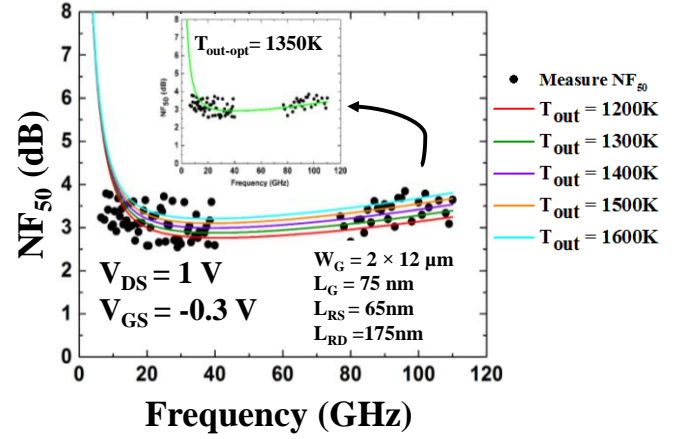


Fig. 11. PHEMT noise characteristics up to 110 GHz for measured and simulated NF_{50} ($L_G = 75\text{nm}$, $W_G = 2 \times 12\ \mu\text{m}$, $L_{RS} = 65\text{nm}$ and $L_{RS} = 175\text{nm}$).

To quantify the influence of T_{out} on the extracted four noise parameters specifically NF_{min} , five different temperatures T_{out} are used (figure 12).

These output temperatures take into account the measurements dispersion of NF_{50} . We relied on NF_{50} model projection to determine an error of 30 % (400 K) in T_{out} extraction, then we calculate the influence of this error on the values of the four noise parameters.

In order to see any sign of a possible influence of the NF_{50} dispersion with T_{out} variation, the four noise parameters were plotted in 0.25 GHz – 110 GHz frequency range (figure 12).

At 94 GHz the values extracted of NF_{min} were 1.71 dB and 1.95 dB at $T_{out} = 1200\text{K}$ and $T_{out} = 1600\text{K}$ respectively, it gives only $\pm 0.24\text{dB}$ (14 %) in extraction NF_{min} error. The magnitude and the phase of the optimal reflection factor of the generator (Γ_{Opt}) are not influenced by this dispersion. On the other hand, we have around (20 %) error with noise resistance R_n . At 40 GHz the variation of the four noise parameters are insignificant as a function of the T_{out} temperature at low frequency.

Finally, the noise performance are deduced with an optimal $T_{out-opt} = 1350\text{K}$. The results are listed in table 3 at two different frequencies 40 GHz and 94 GHz. The results achieved at 94 GHz were NF_{min} of 1.8 dB (with associated gain of 11.6 dB) for an optimal voltage gate-to-source $V_{GS,Opt} = -0.3\text{V}$. The value of NF_{min} is higher than results found in the state-of-the-art (less than 1 dB) [5]. However, the associated gain (11.6 dB) is higher compared to the value of the state of the art of 8.9 dB. The noise resistance was almost stable ($R_n = 41.6\ \Omega - 45.1\ \Omega$) and typically independent of frequency. Finally, the optimal reflection factor of the generator (Γ_{Opt}) to obtain the minimum noise (NF_{min}) is reported in phase and magnitude forms. The value at 94 GHz were $\text{Mag}(\Gamma_{Opt}) = 0.64$ and $\text{phase}(\Gamma_{Opt}) = 48\text{degrees}$.

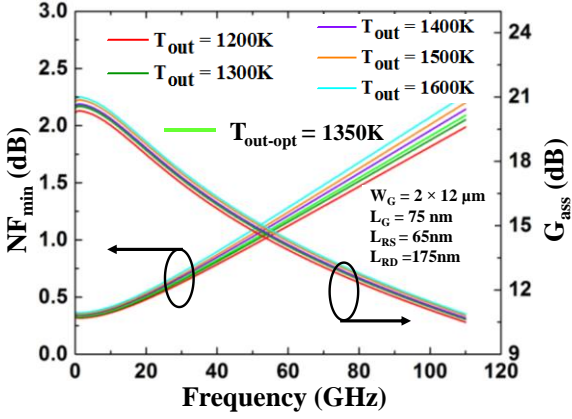


Fig. 12 (a). Extracted NF_{min} up to 110 GHz with various values of output temperature (from 1200K to 1600 K), ($L_G = 75\text{nm}$, $W_G = 2 \times 12 \mu\text{m}$, $L_{RS} = 65\text{nm}$ and $L_{RD} = 175\text{nm}$).

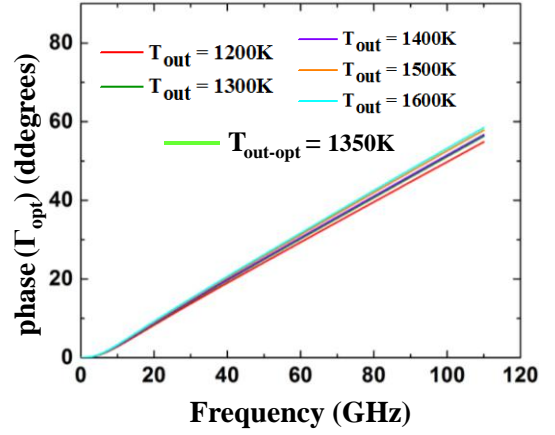


Fig. 12 (d). Extracted phase Γ_{opt} up to 110 GHz with various values of output temperature (from 1200K to 1600 K), ($L_G = 75\text{nm}$, $W_G = 2 \times 12 \mu\text{m}$, $L_{RS} = 65\text{nm}$ and $L_{RD} = 175\text{nm}$).

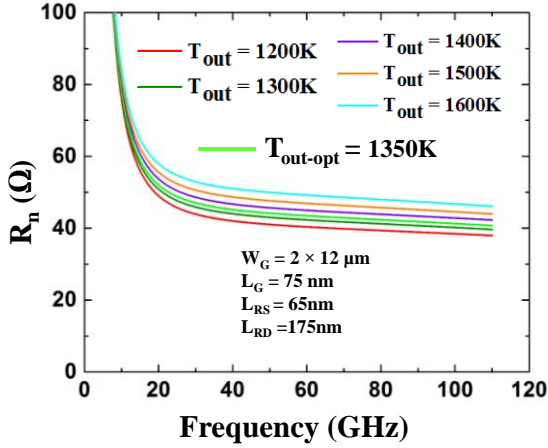


Fig. 12 (b). Extracted R_n up to 110 GHz with various values of output temperature (from 1200K to 1600 K), ($L_G = 75\text{nm}$, $W_G = 2 \times 12 \mu\text{m}$, $L_{RS} = 65\text{nm}$ and $L_{RD} = 175\text{nm}$).

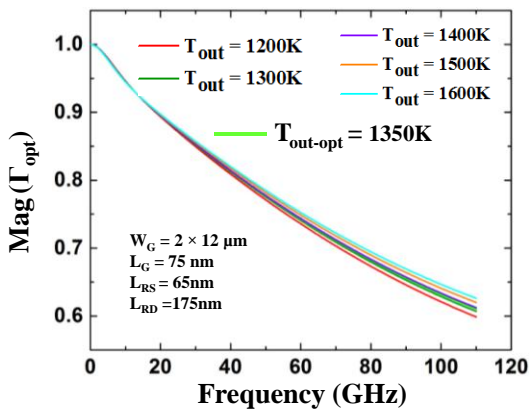


Fig. 12 (c). Extracted magnitude Γ_{opt} up to 110 GHz with various values of output temperature (from 1200K to 1600 K), ($L_G = 75\text{nm}$, $W_G = 2 \times 12 \mu\text{m}$, $L_{RS} = 65\text{nm}$ and $L_{RD} = 175\text{nm}$).

TABLE III
FOUR NOISE PARAMETERS VALUES OF PHEMT ($L_G = 75\text{NM}$, $W_G = 2 \times 12 \mu\text{M}$, $L_{RS} = 65\text{NM}$ AND $L_{RD} = 175\text{NM}$).

Parameters	At 40 GHz	At 94 GHz	State of the art
NF_{min} (dB)	0.82	1.8	
G_{ass} (dB)	16	11.6	
R_n (Ω)	45.1	41.6	
$Mag(\Gamma_{opt})$	0.8	0.64	
$Phase(\Gamma_{opt})$ deg	19.7	48.3	

V. CONCLUSION

In this paper, we have presented a complete work of HEMT's components from the epilayer structure description followed by the device fabrication and concluded by the RF and noise measurements. We achieved a $f_{max} = 800$ GHz using asymmetric gate recess on PHEMT with large gate length of 75 nm. This performance was obtained thanks to improvement of the epilayer structure with mobility channel of $\mu_{Hall} = 12000$ $\text{cm}^2/\text{V}\cdot\text{s}$. and the use of asymmetric recess. The measured and simulated S-parameters were presented and validated using the Small Signal Equivalent Circuit (SSEC) up to 110 GHz with considering the gate leakage current. Furthermore, noise parameters were also extracted using the NF_{50} method. Our transistors have a NF_{min} of 0.82 dB at 40 GHz ($G_{ass} = 16$ dB), and NF_{min} of 1.8 dB at 94 GHz with a huge associated gain $G_{ass} = 11.6$ dB.

REFERENCES

- [1] W. R. Deal, "InP HEMT for sub-millimeter wave space applications: Status and challenges," in *2014 39th International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, Sep. 2014, pp. 1–3, doi: 10.1109/IRMMW-THz.2014.6956216.
- [2] M. Sato *et al.*, "Compact receiver module for a 94 GHz band passive millimetre-wave imager," *Antennas Propag. IET Microw.*, vol. 2, no. 8, pp. 848–853, Dec. 2008, doi: 10.1049/iet-map:20070322.
- [3] H.-B. Jo *et al.*, "Lg = 19 nm In_{0.8}Ga_{0.2}As composite-channel HEMTs with $f_T = 738$ GHz and $f_{max} = 492$ GHz," 2020, p. 8.4.1-8.4.4, doi: 10.1109/IEDM13553.2020.9372070.
- [4] X. Mei *et al.*, "First Demonstration of Amplification at 1 THz Using 25-nm InP High Electron Mobility Transistor Process," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 327–329, Apr. 2015, doi: 10.1109/LED.2015.2407193.
- [5] T. Takahashi, K. Makiyama, N. Hara, M. Sato, and T. Hirose, "Improvement in high frequency and noise characteristics of InP-based HEMTs by reducing parasitic capacitance," in *2008 20th International Conference on Indium Phosphide and Related Materials*, May 2008, pp. 1–4, doi: 10.1109/ICIPRM.2008.4702964.
- [6] K. M. K. H. Leong *et al.*, "A 0.85 THz Low Noise Amplifier Using InP HEMT Transistors," *IEEE Microw. Wirel. Compon. Lett.*, vol. 25, no. 6, pp. 397–399, Jun. 2015, doi: 10.1109/LMWC.2015.2421336.
- [7] T. Takahashi *et al.*, "Enhancement of f_{max} to 910 GHz by Adopting Asymmetric Gate Recess and Double-Side-Doped Structure in 75-nm-Gate InAlAs/InGaAs HEMTs," *IEEE Trans. Electron Devices*, vol. 64, no. 1, pp. 89–95, Jan. 2017, doi: 10.1109/TED.2016.2624899.
- [8] T. Takahashi *et al.*, "Maximum frequency of oscillation of 1.3 THz obtained by using an extended drain-side recess structure in 75-nm-gate InAlAs/InGaAs high-electron-mobility transistors," *Appl. Phys. Express*, vol. 10, no. 2, p. 024102, Jan. 2017, doi: 10.7567/APEX.10.024102.
- [9] K. Shinohara, T. Matsui, T. Mimura, and S. Hiyamizu, "Novel asymmetric gate-recess engineering for sub-millimeter-wave InP-based HEMTs," in *2001 IEEE MTT-S International Microwave Symposium Digest (Cat. No.01CH37157)*, May 2001, vol. 3, pp. 2159–2162 vol.3, doi: 10.1109/MWSYM.2001.967342.
- [10] D. G. Ballegeer, I. Adesida, C. Caneau, and R. Bhat, "Physics and behavior of asymmetrically recessed InP-based MODFET's fabricated with an electron beam resist process," in *Proceedings of 1994 IEEE 6th International Conference on Indium Phosphide and Related Materials (IPRM)*, Mar. 1994, pp. 331–334, doi: 10.1109/ICIPRM.1994.328237.
- [11] N. Wichmann *et al.*, "Fabrication technology and device performances of ultra-short 30-nm-gate pseudomorphic In_{0.52}Al_{0.48}As/In_{0.75}Ga_{0.25}As HEMTs," in *2008 20th International Conference on Indium Phosphide and Related Materials*, May 2008, pp. 1–4, doi: 10.1109/ICIPRM.2008.4702912.
- [12] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 7, pp. 1151–1159, Jul. 1988, doi: 10.1109/22.3650.
- [13] M. W. Pospieszalski, "Modeling of noise parameters of MESFETs and MODFETs and their frequency and temperature dependence," *IEEE Trans. Microw. Theory Tech.*, vol. 37, no. 9, pp. 1340–1350, Sep. 1989, doi: 10.1109/22.32217.
- [14] G. Dambrine, J.-Raskin, F. Danneville, D. V. Janvier, J.-Colinge, and A. Cappy, "High-frequency four noise parameters of silicon-on-insulator-based technology MOSFET for the design of low-noise RF integrated circuits," *IEEE Trans. Electron Devices*, vol. 46, no. 8, pp. 1733–1741, Aug. 1999, doi: 10.1109/16.777164.
- [15] F. Danneville *et al.*, "RF and broadband noise investigation in High-k/Metal Gate 28-nm CMOS bulk transistor," *Int. J. Numer. Model. Electron. Netw. Devices Fields*, vol. 27, no. 5–6, pp. 736–747, Sep. 2014, doi: 10.1002/jnm.1972.
- [16] G. Dambrine, H. Happy, F. Danneville, and A. Cappy, "A new method for on wafer noise measurement," *IEEE Trans. Microw. Theory Tech.*, vol. 41, no. 3, pp. 375–381, Mar. 1993, doi: 10.1109/22.223734.
- [17] R. J. Hawkins, "Limitations of Nielsen's and related noise equations applied to microwave bipolar transistors, and a new expression for the frequency and current dependent noise figure," *Solid-State Electron.*, vol. 20, no. 3, pp. 191–196, Mar. 1977, doi: 10.1016/0038-1101(77)90183-6.
- [18] D. Kim, J. A. del Alamo, J. Lee, and K. Seo, "Logic Suitability of 50-nm In_{0.7}Ga_{0.3}As HEMTs for Beyond-CMOS Applications," *IEEE Trans. Electron Devices*, vol. 54, no. 10, pp. 2606–2613, Oct. 2007, doi: 10.1109/TED.2007.904986.