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Thomas Lerond, Dmitri Yarekha, Vanessa Avramovic, Thierry Melin, S. Arscott. Surface micromachining of chip-edge silicon microcantilevers using xenon difluoride etching of silicon-on-insulator. *Journal of Micromechanics and Microengineering*, 2021, 31 (8), pp.085001. 10.1088/1361-6439/ac0807. hal-03411474

**HAL Id: hal-03411474**

**<https://hal.science/hal-03411474v1>**

Submitted on 2 Nov 2021

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# **Surface micromachining of chip-edge silicon microcantilevers using xenon difluoride etching of silicon-on-insulator**

Thomas Lerond, Dmitri Yarekha, Vanessa Avramovic, Thierry Mélin, and Steve Arscott

University of Lille, CNRS, Centrale Lille, Univ. Polytechnique Hauts-de-France, UMR 8520-IEMN, F-59000 Lille, France.

Email: [steve.arscott@univ-lille.fr](mailto:steve.arscott@univ-lille.fr)

## **Abstract**

We demonstrate a straightforward surface micromachining process for the rapid prototyping of thin ‘chip-edge’ silicon microcantilevers protruding from the edge of a silicon-on-insulator chip. The process uses a single photolithographic mask—with xenon difluoride used to both pattern the silicon microcantilevers and release them by etching part of the underlying silicon wafer. During the release step, the silicon microcantilevers are protected from the xenon difluoride by a combination of photoresist and buried silicon dioxide. The use of common microfabrication materials (silicon-on-insulator and positive photoresist) and chemicals (buffered hydrofluoric acid and xenon difluoride), along with a maximum process temperature of 100°C, makes for a generic, soft micromachining process which is—in principle—compatible with preserving the integrity of any pre-patterned circuitry present on the silicon microcantilever top surface. Doppler vibrometry measurements of the silicon microcantilevers reveal a well-defined resonant frequency and a quality factor comparable with that of similar silicon microcantilevers fabricated using other means. Our enabling technological process allows the rapid prototyping of chip-edge silicon microcantilevers—potentially integrating sensitive circuitry for novel probe technologies—by avoiding the relatively cumbersome, expensive, and potentially circuit-damaging front-to-back processing/deep etching combination.

## 1. Introduction

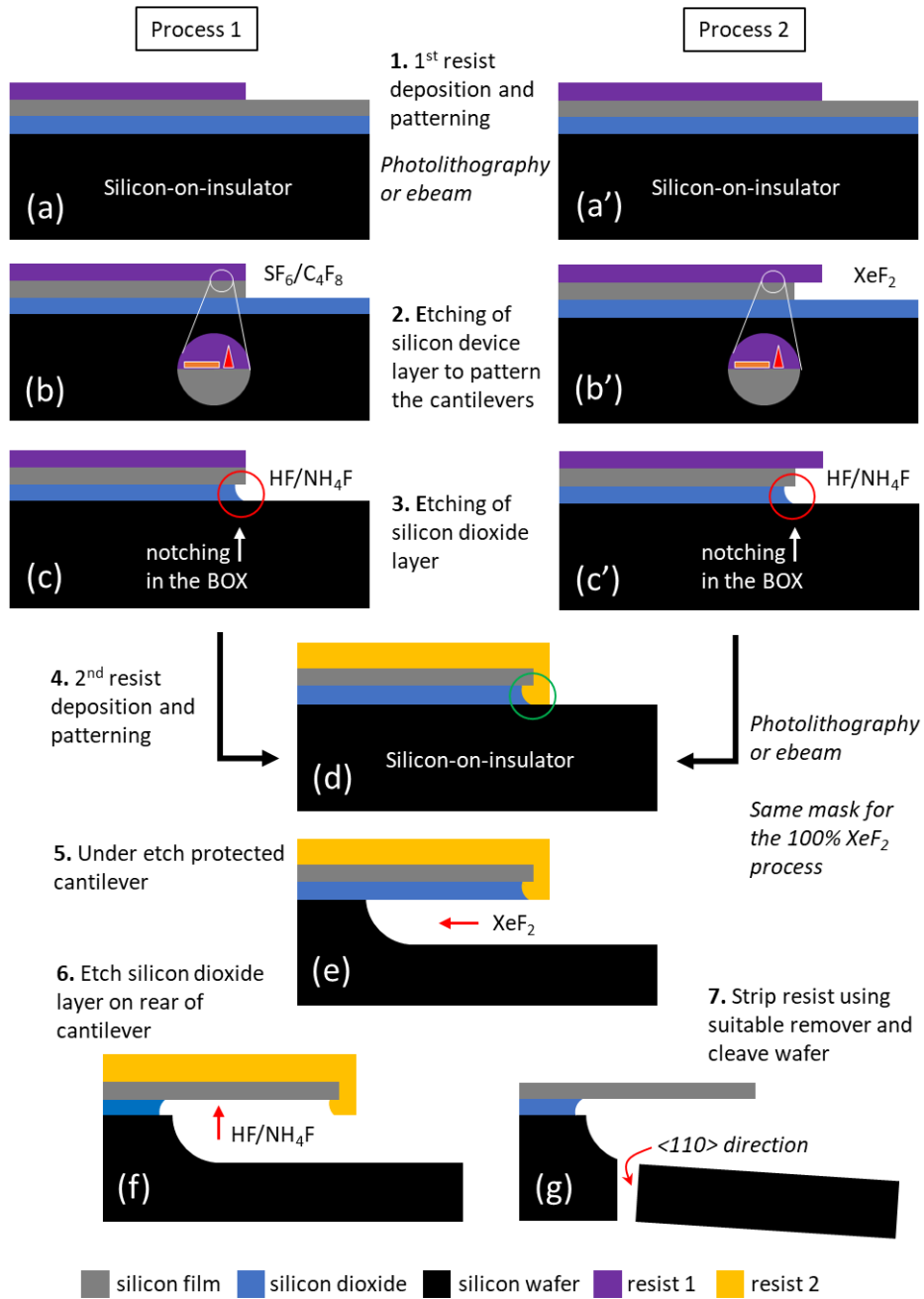
Silicon microcantilevers [1] have been applied to areas ranging from components for fundamental studies [2], to physical [3], chemical [4], biological [5], and electrical [6] probing technologies. The choice of silicon as the microcantilever material enables the integration of microfabricated electronic circuitry. However, such circuitry must not be damaged by the subsequent micromachining process employed to fabricate the microcantilevers. Silicon microcantilevers are either ‘on-chip’ or ‘chip-edge’—in the latter case, the microcantilever protrudes from the edge of the silicon chip. It is a relatively trivial procedure to fabricate on-chip silicon microcantilevers using surface micromachining [7,8] by combining lithographically-derived masking and selective sacrificial etching [9]. In contrast, the fabrication of chip-edge microcantilevers requires bulk micromachining [10] to remove a portion of the underlying silicon wafer. This process involves relatively-cumbersome front-to-back lithography [11] combined with some means of rear-face deep etching of parts of the entire silicon wafer thickness. Wet chemical-based deep etching of silicon, employing basic solutions, e.g. potassium hydroxide [12] or tetramethylammonium hydroxide [13], is possible—but this route can suffer from a lack of suitable masking material for any sensitive front-side circuitry. Plasma-based deep etching of silicon, e.g. using the cyclic etch/passivation (sulphur hexafluoride/octafluorocyclobutane) process [14], is also possible—but requires relatively expensive plasma equipment. Besides being costly, such front-to-back processing can lead to wafer bowing which may cause clamping problems which leads to back etch process non-uniformity due to thermal issues. In addition to this, exposure of sensitive parts of the wafer to high-power plasmas and residual amorphous fluoropolymer deposits can result in post-process cleaning problems (due to the necessity of lengthy wet chemical exposures and plasma ashing) which can, in turn, lead to damage in any circuitry pre-fabricated before the bulk micromachining. It has thus been noted that the micromachining of chip-edge silicon microcantilevers, integrating electrical circuitry, remains challenging and requires further developments and innovation [15]. One solution is to reconsider to surface micromachining by using xenon difluoride to selectively etch parts of the underlying silicon from the surface [16]. This approach has been used for the fabrication of microcantilevers composed of various materials [17–26]. However, a silicon microcantilever must be completely masked whilst the xenon difluoride etches the underlying silicon. Silicon dioxide or silicon nitride have been used as masking materials [20,21], but such materials are deposited at relatively high temperature and need to be chemically removed after cantilever releasing—both procedures put pre-fabricated circuitry at risk of damage.

This article describes a straightforward surface micromachining process for the rapid prototyping of chip-edge silicon microcantilevers using xenon difluoride etching of silicon-on-insulator (SOI) material. The process has several originalities compared to previous approaches. The process involves two lithographic masking steps—and can be performed using a single photolithographic mask. A positive photoresist in combination with the buried silicon dioxide are used to fully encapsulate and

protect the silicon microcantilever during the subsequent xenon difluoride under etching. The combination of materials (silicon-on-insulator and positive photoresist) and processing chemicals (buffered hydrofluoric acid and xenon difluoride) makes for a ‘soft’ process, which is compatible with preserving the integrity of any pre-patterned circuitry [27,28] present on the silicon microcantilever top surface. The maximum temperature used in the process is 100 °C—no high temperature-deposited masking materials, e.g. silicon dioxide/nitride, are required. Finally, the cleaving/dicing step completes rapid prototyping of chip-edge microcantilevers by avoiding front-to-back processing.

## **2. Micromachining process**

Figure 1 shows a schematic diagram of the principal steps of the micromachining process developed here for the fabrication of chip-edge silicon microcantilevers using silicon-on-insulator material. The process enables the silicon microcantilevers to be patterned using one of two methods (Process 1 and Process 2). In Process 1, the silicon microcantilevers are patterned using plasma-based etching—in Process 2, the silicon microcantilevers are patterned using xenon difluoride etching. For both Process 1 and Process 2, the silicon microcantilevers are under etched using xenon difluoride—Process 2 is therefore a 100% xenon difluoride process.



**Figure 1.** Schematic diagram of the surface micromachining process for the fabrication of chip-edge silicon microcantilevers using silicon-on-insulator (SOI) wafers. Definition of microcantilever shape using lithographic resist patterning (a and a') followed by plasma-based dry etching (b) or gas-phase xenon difluoride etching (b'). Etching of the buried silicon dioxide layer (BOX) using hydrofluoric acid/ammonium fluoride based wet etching (c and c')—note the small notching caused by under etching (red circles). Patterning of the second resist layer using lithography (d)—note that the second resist fills the under etched notch in the BOX (green circle). Under etching of the silicon microcantilever using xenon difluoride gas (e). Removal of the silicon dioxide BOX layer from beneath the silicon microcantilever using hydrofluoric acid/ammonium fluoride-based wet etch (f). Removal of the second

resist layer using resist stripper and subsequent wafer dicing along the  $\langle 110 \rangle$  direction to produce a chip-edge silicon microcantilever (g). The zoomed inset circles in (b) and (b') indicate the possibility of protecting pre-existing circuitry and features on the top silicon surface during the micromachining process.

### 2.1 Patterning of the silicon microcantilevers

Commercial 3-inch diameter SOI [29–31] wafers (Si-Mat, Germany) were purchased for the study. The silicon device layer thickness is  $5 \pm 0.5 \mu\text{m}$ , the buried silicon dioxide layer (BOX) thickness is  $1 \pm 0.1 \mu\text{m}$ , and the silicon handle wafer thickness is  $400 \pm 10 \mu\text{m}$ . The orientation of the crystalline silicon layers is (100)—with the principal wafer flat aligned along the  $\langle 110 \rangle$  crystal direction. The electrical resistivity of silicon (device layer and handle wafer) is  $>1000 \Omega \text{ cm}$ .

First of all, the SOI wafer is cleaned and dehydrated [32]. Following the application of an adherence promoter (hexamethyldisilazane—HMDS), the resist (either ebeam- or photo-sensitive) is then spin coated onto the surface of the SOI wafer. We employed a  $5 \mu\text{m}$  thick layer of AZ® 40XT (MicroChem GmbH, Germany) positive photoresist. The resist is then patterned using an in-house photolithographic mask containing 94 microcantilevers, all of which were aligned perpendicular to the  $\langle 110 \rangle$  principal wafer flat to facilitate the wafer dicing later in the process—see Fig. 1(a) and Fig. 1(a'). The photomask contained microcantilevers designs which are  $1000 \mu\text{m}$  long and  $100 \mu\text{m}$  wide—the microcantilever thickness being defined by the silicon device layer thickness ( $5 \mu\text{m}$ ). The photolithographic dose for the AZ® 40XT photoresist was  $100 \text{ mJ cm}^{-2}$  (10 s at  $10 \text{ mW cm}^{-2}$ ), performed in an MA/BA6 mask aligner (Suss Microtech, Germany). The photoresist is then developed in AZ® 236MIF for 120 seconds, rinsed thoroughly with deionized water, and finally dried using dry nitrogen.

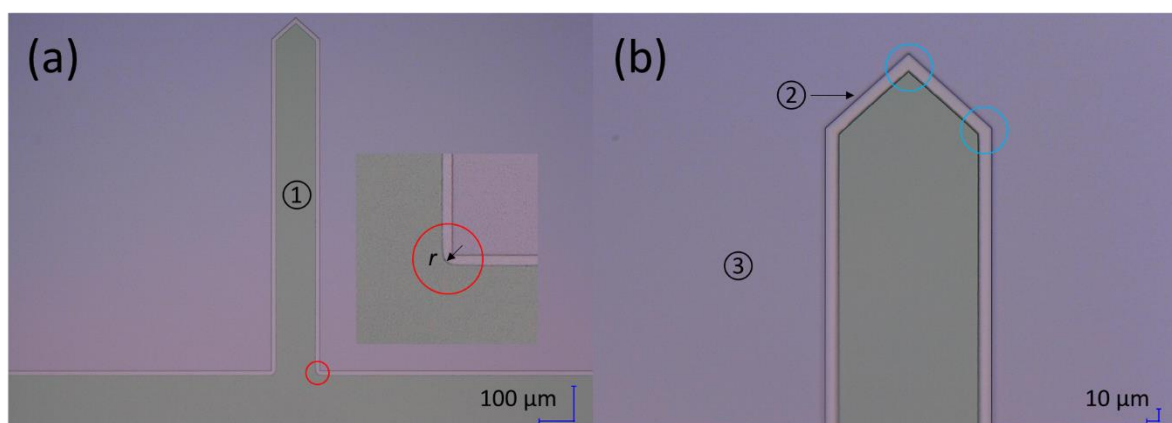
To demonstrate the flexibility of the approach here, the silicon microcantilevers are patterned in the silicon device layer using two methods—see Fig. 1. We refer to these two methods as ‘Process 1’ and ‘Process 2’ throughout the article.

For one SOI wafer, the silicon microcantilevers were defined using plasma-based, inductively-coupled ion etching (Bosch process [14]) in a PlasmaLab Pro 100 Estrelas (Oxford Instruments, UK)—Fig. 1(b). For a second SOI wafer, the silicon microcantilevers were defined using xenon difluoride etching (Xactix, USA)—see Fig. 1(b'). The former method demonstrates compatibility with plasma processes and enables precise alignment. The latter method demonstrates that a complete xenon difluoride approach is feasible—effectively eliminating plasma etching from the prototyping.

For the plasma-based patterning in Process 1, alternating  $\text{SF}_6$  (etch) and  $\text{C}_4\text{F}_8$  (passivation) plasma cycles [14] defined the microcantilever with a vertical silicon etch rate of  $\sim 4 \mu\text{m min}^{-1}$ . For the xenon difluoride etching in Process 2, 15 send etching cycles at a pressure of 4 Torr were used. In the

unmasked zones, we observed a vertical etch rate of the silicon device layer equal to  $1.3 \mu\text{m min}^{-1}$ , under the masked zone we recorded a lateral etch rate of  $1.8 \mu\text{m min}^{-1}$ . However, once the silicon dioxide BOX layer is exposed, the lateral silicon etch rate (underneath the masked zones) increases to  $9.3 \pm 0.3 \mu\text{m min}^{-1}$ . Thus, for Process 2, the silicon microcantilever is formed by (i) xenon difluoride vertical etching of the silicon device layer in the unmasked zones and (ii) xenon difluoride lateral etching underneath the mask. Both these etch rates were quantified for the specific device layer thickness that we used ( $5 \mu\text{m}$ ). The lateral etch rate of the silicon device layer underneath the mask is larger once the silicon device layer is fully etched in the unmasked regions. This is due to a reduction in the overall silicon surface exposed to the xenon difluoride [33]. This is a key point since the lateral etch rate (up to the removal of the silicon device layer in the unmasked zones) effectively determines the minimum size (microcantilever width) that is possible in Process 2. In our case here (a  $5 \mu\text{m}$  thick device layer), the vertical etch rate of the silicon device layer is  $1.3 \mu\text{m min}^{-1}$  and the lateral etch rate underneath the mask before the silicon device layer is fully etched is  $1.8 \mu\text{m min}^{-1}$ —therefore, for an etch time of  $5/1.3 \cong 3.85$  minutes, the feature size must be larger than  $1.8 \times 3.85 \times 2 \cong 13.9 \mu\text{m}$ —the factor 2 accounts for the etch progressing from both sides of the masking feature.

Figure 2 shows a silicon microcantilever that has been patterned by xenon difluoride etching in Process 2. The etching of the silicon device layer under the photoresist mask is visible. It is also interesting to note that the silicon device layer edge profile is rounded ( $r \sim 15 \mu\text{m}$ ) for external acute mask angles due to isotropic etching—see red circles in Fig. 2(a); whereas for external reflex mask angles, the silicon edge profile reproduces faithfully the lithographic mask pattern—see light blue circles in Fig. 2(b).



**Figure 2.** Optical microscopy images of the patterning of the silicon microcantilevers using photoresist masking and xenon difluoride etching in Process 2. The numbers correspond to the following layers: ① the silicon device layer, ② the photoresist (AZ® 40XT), and ③ the silicon dioxide BOX layer.

The red circle in (a) highlights the rounding of the silicon device layer edge for acute mask angles. The blue circles in (b) indicate that the mask patterning is reproduced for reflex mask angles.

## *2.2 Etching of the silicon dioxide film*

For both Process 1 and Process 2, **part of** the silicon dioxide BOX layer on top of the silicon handle wafer is selectively etched away using a commercial 7:1 ‘buffered’ hydrofluoric acid solution (HF/NH<sub>4</sub>F)—see Fig. 1(c) and Fig. 1(c’). To do this, the first positive resist mask remains in place. Note that the presence of this resist would effectively protect any potential circuitry present on the silicon microcantilever surface from the buffered HF. The buffered HF does not etch the silicon microcantilever side walls and stops on the silicon handle surface due to its high selectivity. The 1 μm thick silicon dioxide BOX layer was etched in 16±1 minutes—corresponding to an etch rate of ~62.5±10.8 nm min<sup>-1</sup> (allowing for the ±0.1 μm variation in the silicon dioxide BOX thickness). As buffered hydrofluoric acid etches silicon dioxide isotropically, there is a small—yet significant (~1 μm)—under etching of the silicon dioxide underneath the edges of the silicon microcantilevers. The resulting notching is indicated in Fig. 1(c) and Fig. 1(c’) by red circles. Finally, the first layer of resist (AZ® 40XT) is removed using SVC-14 positive photoresist remover (1h at 70°C), rinsed with isopropyl alcohol, and dried with nitrogen.

## *2.3 Under etching of the microcantilevers using xenon difluoride*

To under etch the silicon microcantilevers and release them from the silicon handle a second resist mask is required—see Fig. 1(d). The role of this mask is threefold. First, to protect the top surface of the silicon microcantilever from the xenon difluoride. Second, to protect the silicon microcantilever sidewalls from the xenon difluoride. Third, to shield the small, exposed silicon area underneath the microcantilever edges—i.e. the notch formation visible in Fig. 1(c) and Fig. 1(c’)—caused by the previous silicon dioxide etching step. The silicon dioxide BOX layer, which is still present underneath the silicon microcantilever, protects the bottom surface of the silicon microcantilever from the xenon difluoride under etch.

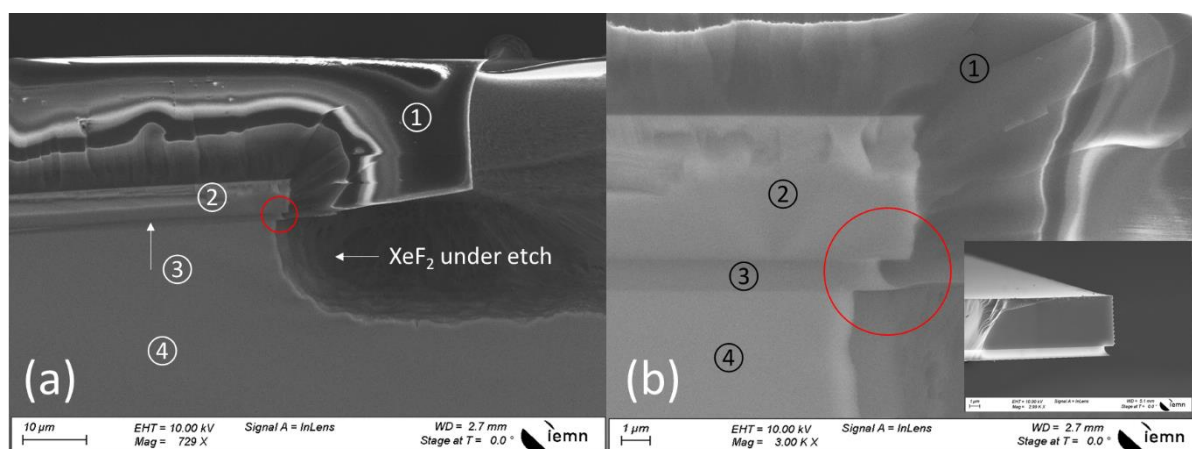
Following a deposition of HMDS onto the wafer surface, a ~30 μm thick layer of AZ® 40XT is spin coated to cover the patterned surface of the SOI wafer—see Fig. 1(d). Note that it is important that this photoresist wets and spontaneously fills [34] the small notch gap in the silicon dioxide BOX layer present underneath the edges of the microcantilevers—see the green circle in Fig. 1(d)—this is vital for the success of subsequent xenon difluoride etching of the silicon handle. A 30 μm thick photoresist was chosen for the second lithography for two reasons: (i) to enable planarization of the photoresist over the etched surface topography (6 μm – the etched silicon device layer plus the etched



silicon dioxide BOX) and (ii) to enable the process to be extended to SOI wafers having thicker device layers if required. It should be noted that Process 1 uses two different-sized masks, whereas Process 2 uses one mask—this is seen by comparing Fig. 1(a), Fig. 1(a’), and Fig. 1(d). In the case of Process 1, a second laterally-larger (140  $\mu\text{m}$ ) masking is necessary to completely cover and protect the microcantilevers during the xenon difluoride under etching step. In the case of Process 2, the same mask that is used to define to microcantilever can be used to protect the microcantilevers during the xenon difluoride under etching release step. The reason for this is the lateral etching of the microcantilevers during the first xenon difluoride etch—see Fig. 1(b’)—that does not occur when defining the microcantilevers using  $\text{SF}_6/\text{C}_4\text{F}_8$  in Process 1—see Fig. 1(b). **Note that although both Process 1 and Process 2 require two masking steps (ebeam or photolithographic), Process 2 can be performed using a single mask (ebeam or photolithographic).** The AZ® 40XT photoresist layer is now patterned using photolithographic masking. The photolithographic dose of the AZ® 40XT (30  $\mu\text{m}$  thick) was 400  $\text{mJ cm}^{-2}$  (40 s at 10  $\text{mW cm}^{-2}$ ). The AZ® 40XT was developed in AZ® 326MIF for 250 s.

The same parameters were used as above for the xenon difluoride under etching of the silicon handle. For this step, 177×15 second cycles at a pressure of 4 Torr were required to under etch the microcantilevers by laterally etching  $\sim 80 \mu\text{m}$  of the silicon handle wafer, the lateral and vertical etch rates of the silicon were measured to be  $\sim 1.8 \mu\text{m min}^{-1}$  throughout the etch.

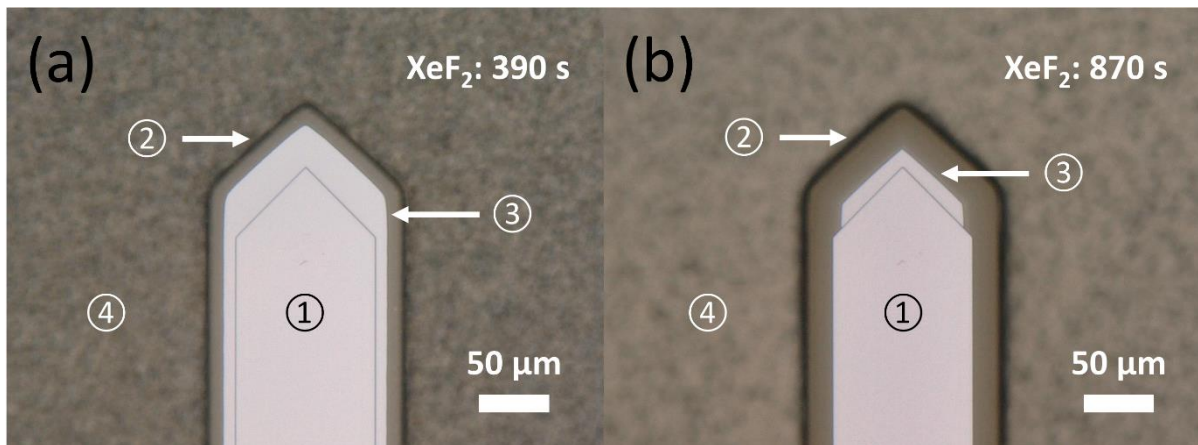
Figure 3 shows scanning electron microscopy (SEM) images of cleaved, mid-process SOI wafers during under etching of the patterned silicon device layer using xenon difluoride. The photoresist, patterned silicon device layer, buried oxide, and silicon handle wafer are all apparent. The small notching that is caused by the HF etching of the buried oxide is also visible in Fig. 3—this is filled by the photoresist (red circles). This sample has followed Process 1, scalloping is visible on the vertical edge of the patterned silicon device layer due to the  $\text{SF}_6/\text{C}_4\text{F}_8$  etch—see inset to Fig. 3(b) where the photoresist has been removed.



**Figure 3.** Scanning electron microscopy images showing sectional views of (a) the xenon difluoride under etching of the silicon device layer and (b) the capillary filling of the under etched silicon dioxide

layer by the photoresist (red circles). The numbers correspond to: ① the AZ® 40XT photoresist, ② the silicon device layer, ③ the buried silicon dioxide layer, and ④ the silicon handle wafer. **The inset to (b) shows the scalloping on the vertical face of the silicon device layer fabricated using Process 1.**

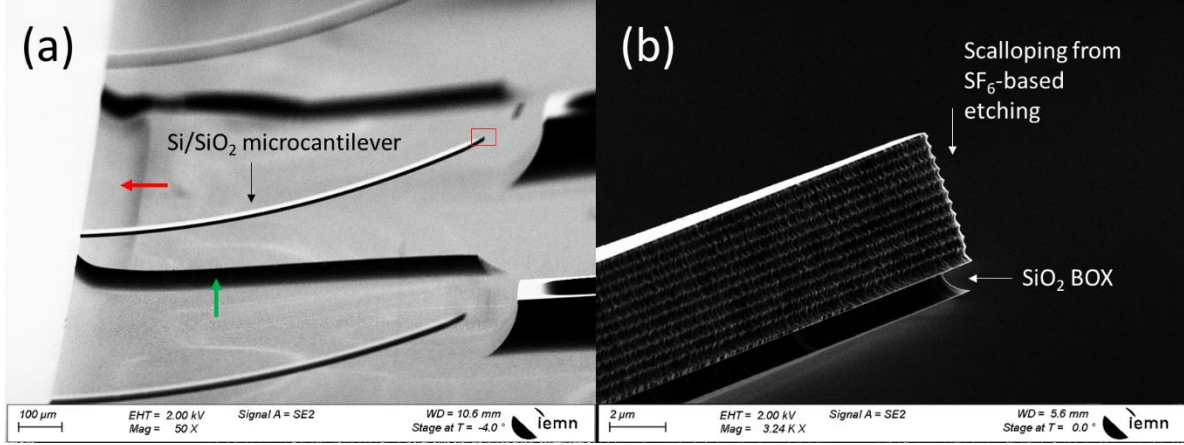
Figure 4 shows optical microscopy images of the progression of the under etching of the silicon microcantilevers using xenon difluoride. The laterally-larger masking ( $140\ \mu\text{m}$ ) compared to the silicon cantilever size is visible in Fig. 4(a). The silicon handle wafer under the mask is etched at a rate of  $\sim 1.8\ \mu\text{m}\ \text{min}^{-1}$ —with the shape of the mask being maintained as the xenon difluoride etch cycles are increased.



**Figure 4.** Optical microscopy images of the progression of the under etching of the photoresist-protected silicon microcantilevers using xenon difluoride. The numbers correspond to: ① the silicon microcantilever patterned in the device layer using Process 1, ② the AZ® 40XT photoresist masking, and ③ and ④ the silicon handle wafer being etched by the xenon difluoride. (a) is taken after 26 xenon difluoride 15 s etching cycles (390 s) and (b) is taken after 58 xenon difluoride 15 s cycles (870 s).

Figure 5 shows mid-process SEM images of the silicon microcantilevers with the rear face protective silicon dioxide BOX still in place following the completion of the xenon difluoride under etching of the silicon handle wafer. Some interesting observations can be made from these images. First, the silicon/silicon dioxide microcantilevers are observed to be bending away from the SOI wafer surface—see Fig.5(a). Second, our experiments indicate a larger vertical etch rate of the silicon handle in the vicinity and under the resist mask—see Fig. 5(a) (red arrow)—this is known as ‘trenching’ [35]. Third, a silicon mesa structure is present underneath the microcantilever (green arrow). Finally, the well-

defined scalloping observed in Fig. 5(b) indicates the successful protection of the silicon microcantilever by the photoresist.



**Figure 5.** Released silicon/silicon dioxide microcantilevers in mid-process (**Process 1**) with the protective photoresist removed to estimate the compressive stress in the silicon dioxide layer. xenon difluoride etch ‘trenching’ is visible in (a)—red arrow. The scalloping on the silicon device layer edge due to plasma-based etching in Process 1 and the notching due to the HF-based under etching of the silicon dioxide BOX are visible in (b). A silicon mesa remains under the released microcantilever (b)—green arrow.

The principal reason for the cantilever bending away from the wafer surface is the presence of compressive stress in the silicon dioxide BOX layer under the silicon microcantilever—see Fig. 5(b). To estimate the value of this stress, we removed the second AZ® 40XT layer from a test sample—using photoresist remover SVC-14—to leave silicon/silicon dioxide microcantilevers. By using scanning electron microscopy (SEM) we measured the radius of curvature  $r$  of the microcantilevers to be  $3.3 \pm 0.1$  mm. SEM also enabled a precise measurement of film thicknesses—the silicon device layer was measured to be  $5.1 \mu\text{m}$  and the silicon dioxide BOX layer to be  $0.96 \mu\text{m}$  (for the wafer processed using Process 1).

The following linear plate theory formula relates the curvature of a bilayer to stresses and mechanical properties:

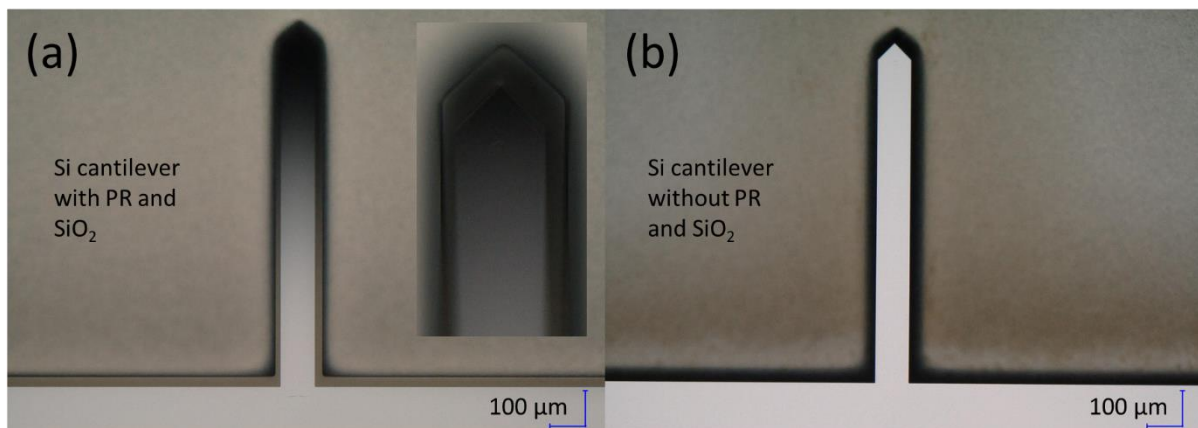
$$\kappa = \frac{-1}{h_r} \frac{6nm(1+m)(\epsilon_r - \epsilon_f)}{1+nm(4+6m+4m^2)+m^4n^2} \quad (1)$$

where  $\kappa = 1/r$  is the curvature of the microcantilever,  $n = \bar{E}_f/\bar{E}_r$  is the ratio of the biaxial modulus of the film and the reference material,  $m = h_f/h_r$  is the ratio of the film thickness and the reference

thickness, and  $\varepsilon_f$  and  $\varepsilon_r$  are the residual strains in the film and the reference material. The biaxial modulus  $\bar{E} = E/1 - \nu$ , where  $E$  and  $\nu$  are the Young's modulus and Poisson's ratio. We consider the reference material to be silicon and the film material to be silicon dioxide. To compute  $\varepsilon_f$ , we require an estimate of  $E_f$ . The Young's modulus of thin film silicon dioxide is taken to be 65 GPa—based on values found in the literature [36–39]. The Poisson's ratio of thin film silicon dioxide is  $\sim 0.15$ . The Young's modulus and Poisson's ratio of silicon (in the  $\langle 110 \rangle$  directions) are 169 GPa and 0.064 [40]. Using Eq. (1), the compressive stress in the silicon dioxide BOX layer is estimated to be  $243.7 \pm 7.6$  MPa—this value is in comparable with those found in the literature [36,39]. It should be noted that the accuracy of the calculations will be affected by the fact that microcantilever deflection ( $\sim 200 \mu\text{m}$ ) is greater than 10% of the microcantilever length—which defines small deflection of a long, thin ( $L > 5w$ ) beam [40].

#### 2.4 Removal of the silicon dioxide from the rear face of the microcantilever and wafer cleaning

Once the under etching of the silicon microcantilevers is complete, the silicon dioxide BOX layer present underneath the microcantilever can be removed. This is done by selective wet etching of the silicon dioxide BOX using buffered HF, with the photoresist still in place—see Fig. 1(f). Again, the presence of the resist means that any potential circuitry on the surface of the microcantilever is not damaged by exposure to the HF/ $\text{NH}_4\text{F}$  based solution. The resist is then removed using positive photoresist remover to prepare the chip for dicing. In the case here, the  $30 \mu\text{m}$  thick AZ® 40XT is removed in an SVC-14 bath ( $70^\circ\text{C}$  for 1h). Figure 6 shows the effect on the cantilever bending by removal of the silicon dioxide from underneath the cantilever and subsequent removal of the photoresist mask.



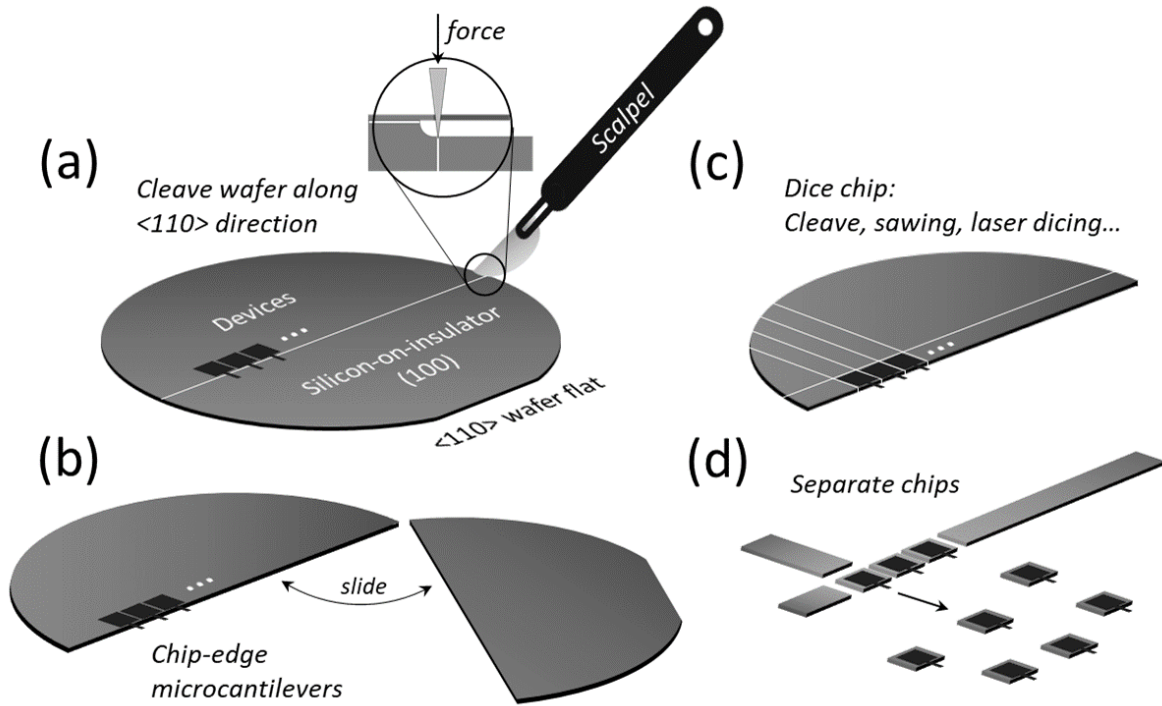
**Figure 6.** Optical microscopy images showing the effect of the removal of the silicon dioxide from the rear surface of the photoresist-protected silicon microcantilever. In (a) the composite photoresist/silicon/silicon dioxide is bending outwards from the silicon handle wafer. In (b) the silicon

dioxide BOX and the photoresist masking have been sequentially removed to leave a very flat microcantilever. These microcantilevers were fabricated using Process 1.

In both surface and bulk micromachining prototyping processes, post-process cleaning is by no means trivial and can have a major impact on device yield. Indeed, the authors have had experience with challenges in plasma-based, rear-side bulk micromachining of silicon microcantilevers which contain circuitry [6]. We note that the ease of post-process cleaning here using standard positive photoresist remover is a major advantage.

### *2.5 Chip dicing for ‘chip-edge’ silicon microcantilevers*

Chip dicing to leave ‘chip-edge’ silicon microcantilevers protruding from the edge of the silicon handle support wafer is performed using an adaptation of simple method developed by one of the authors [41]—see Fig. 7. The SOI handle wafer underneath the microcantilever is initially manually cleaved; this can be done using the etch profile created by the xenon difluoride etching of the handle—see Fig. 7(a). A small volume of isopropanol (using a pipette) can be used to adhere the SOI wafer to a flat metal surface using capillary forces. A no.10 curved blade scalpel (Swann-Morton, UK) is used to cleave the SOI handle wafer along the  $\langle 110 \rangle$  natural cleavage direction. Following this, the unwanted parts of the SOI are removed by sliding the wafers in the plane of the metal surface—see Fig. 7(b); in this way the now-protruding microcantilevers are not damaged. The individual chips can now be diced without danger of damaging the chip-edge microcantilevers. This can be done using several techniques: manual cleaving along natural cleavage planes for rapidity, or more accurate techniques—to produce miniature chips—such as precision diamond sawing, scribing or laser cutting—see Fig. 7(c). Finally, the chips containing the chip-edge microcantilevers can be separated and boxed—see Fig. 7(d).



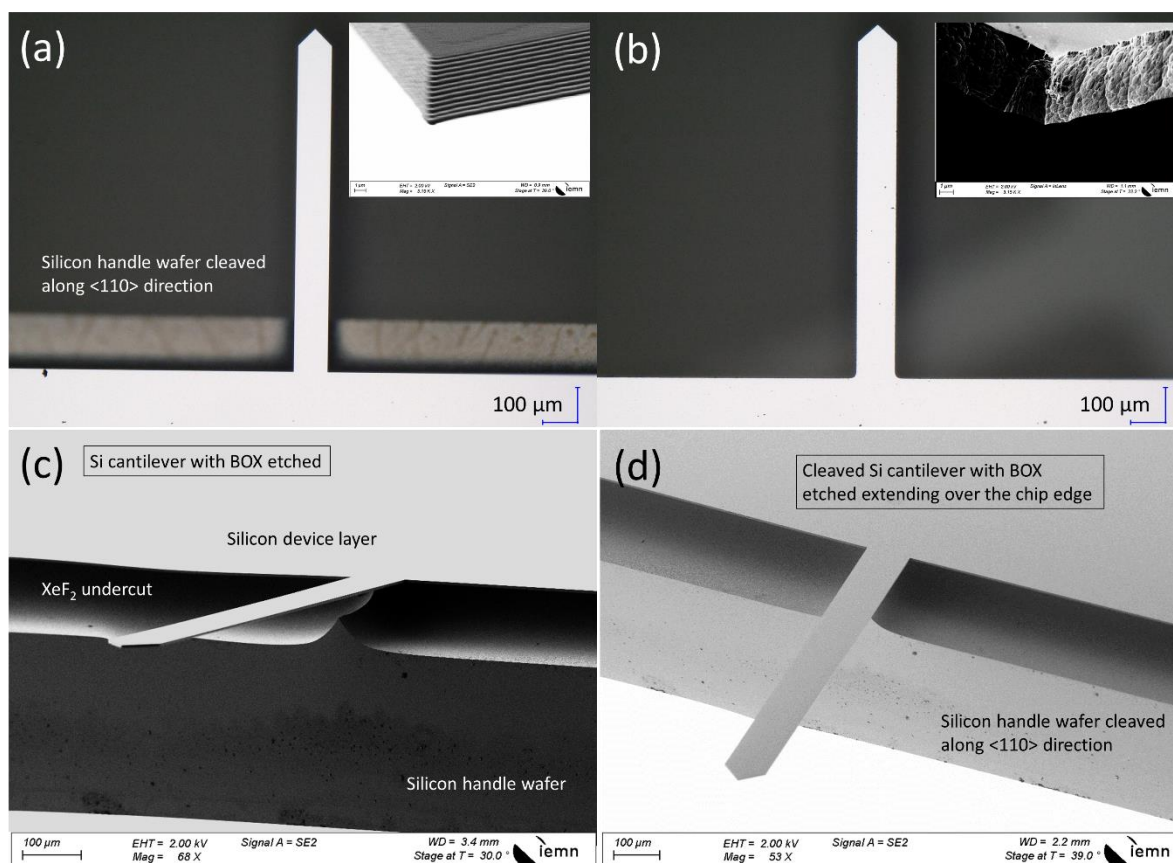
**Figure 7.** Schematic diagram illustrating the cleaving process of the chip-edge microcantilevers. (a) manual cleaving of the silicon handle wafer along the  $\langle 110 \rangle$  silicon wafer direction. (b) slide removal of silicon wafer to reveal chip-edge microcantilevers. (c) chip dicing using either manual cleaving (for rapidity) or other dicing techniques. (d) separation and boxing of chips containing chip-edge microcantilevers.

As the microcantilevers are cleaved using natural cleavage crystal planes in the silicon rather than being lithographically-aligned and back-etched, the impact of inaccurate cleaving and/or variability of cleavage plane on yield can be discussed. First, concerning inaccurate cleaving, if one compares the present method (using SOI) to the more rudimentary approaches [41]; in the current approach, the cleaving breaks the silicon handle wafer and not the device layer. This means that the mechanical part of the device (microcantilever plus overhang) is not affected by cleaving—see the inset to Fig. 7(a). Concerning wafer orientation, the current method relies on the natural cleaving plane in silicon. If one were to use another silicon orientation, the lithographic layout of the microcantilevers would need to take the new natural cleaving plane into account. In the current dicing approach, as the cleaving is ‘manual’, the device yield is mainly prone to poor scalpel positioning and off-axis alignment of the microcantilevers—the latter being more apparent if a wider silicon wafer is cleaved.

### 3. Results and discussions

#### 3.1 Optical and SEM observations of the completed chip-edge silicon microcantilevers

Figure 8 shows optical and scanning electron microscopy images of the chip-edge silicon microcantilevers fabricated using the process described here. For both patterning methods, the microcantilevers were well-defined. Process 1 produced silicon microcantilevers having highly vertical side-walls. Interestingly, for Process 2 we observed that the edges of the resulting microcantilevers were quasi-vertical but having a characteristic roughness [42]—see the inset to Fig. 8(b). This was achieved by allowing a short, additional xenon difluoride etching (at  $9.3 \mu\text{m min}^{-1}$ ) of the silicon device layer underneath the mask, once the silicon device layer had been fully etched in the unmasked zones.



**Figure 8.** Optical and Scanning electron microscopy images of the completed chip-edge silicon microcantilevers fabricated using the process described here. Silicon microcantilevers fabricated using (a) Process 1 and (b) Process 2. SEM images indicating the xenon difluoride undercut (c) and the cantilever release by cleaving the SOI wafer along the  $\langle 110 \rangle$  direction (d). The insets to (a) and (b) show the side walls of the microcantilevers in the case of  $\text{SF}_6/\text{C}_4\text{F}_8$  dry etching and xenon difluoride gas-phase etching.

In addition to micromachining process-validation, inspection using digital optical microscopy VHX-6000 (Keyence, France) and scanning electron microscopy Ultra55 (Zeiss, Germany) enabled the dimensions (and their variations) of the microcantilevers to be determined—these are given in Table 1.

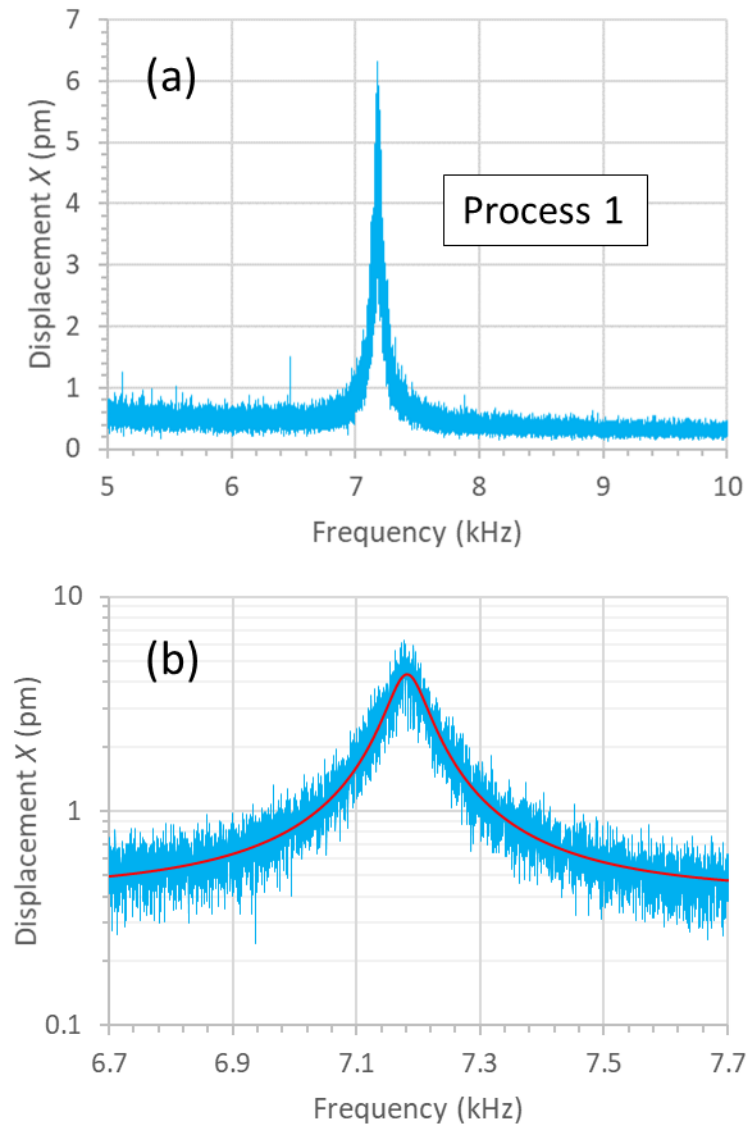
**Table 1.** Experimental microcantilever dimensions length  $L$ , width  $w$ , and thickness  $t$  determined using optical microscopy and scanning electron microscopy.

| <b>Cantilever patterning</b> | <b><math>L</math> (<math>\mu\text{m}</math>)</b> | <b><math>w</math> (<math>\mu\text{m}</math>)</b> | <b><math>t</math> (<math>\mu\text{m}</math>)</b> |
|------------------------------|--|--|--|
| Process 1                    | 995.9 $\pm$ 1.3                                  | 100.1 $\pm$ 1                                    | 5.1 $\pm$ 0.1                                    |
| Process 2                    | 1024.2 $\pm$ 4.3                                 | 115.1 $\pm$ 2.7                                  | 5 $\pm$ 0.1                                      |

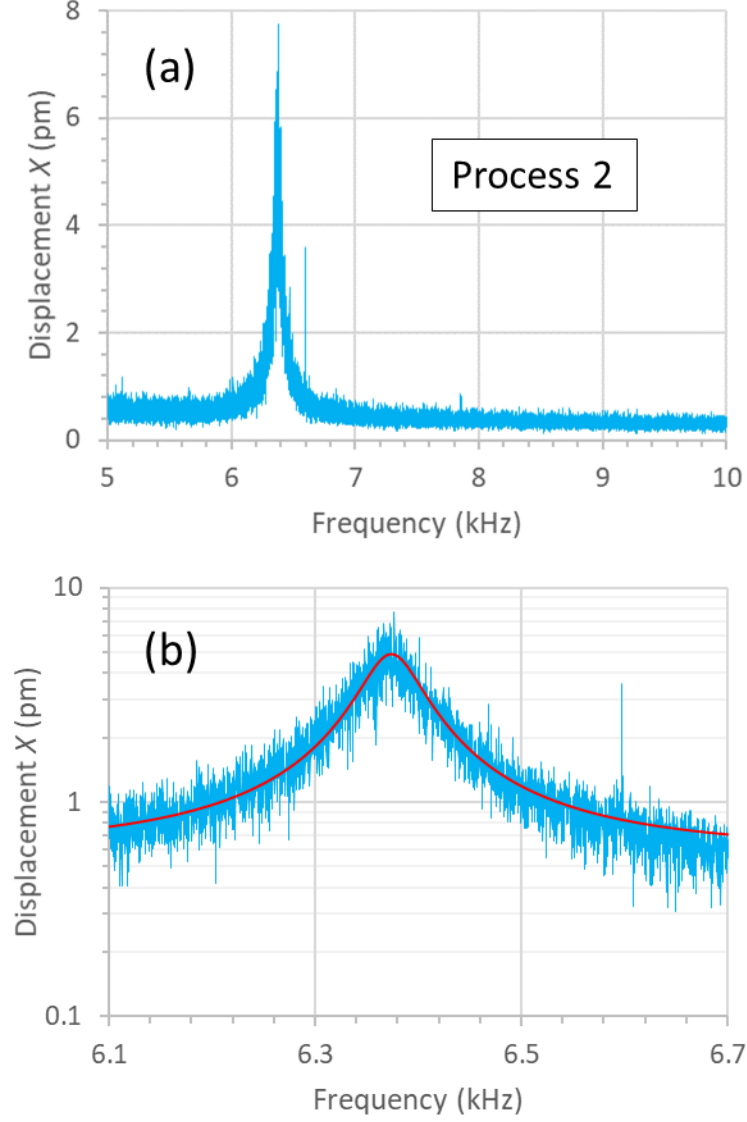
### *3.2 Vibrometry measurements of the silicon microcantilevers*

The silicon microcantilevers were measured using laser Doppler vibrometry in an MSA-500 Micro System Analyzer (Polytec, Germany). Figure 9 and Figure 10 show the results (unsmoothed data) of vibrometry measurements performed on chip-edge silicon microcantilevers fabricated in the study.





**Figure 9.** Experimental plots of the displacement amplitude  $X$  at the tip of the microcantilever as a function of frequency for a silicon microcantilever fabricated using Process 1. (a) 5-10 kHz frequency sweep and (b) zoom over 1 kHz with the displacement amplitude  $X$  plotted on logarithmic axis. The red curve in (b) shows a spectral fit of the data using Eq. (2).



**Figure 10.** Experimental plots of the displacement amplitude  $X$  at the tip of the microcantilever as a function of frequency for a silicon microcantilever fabricated using Process 2. (a) 5-10 kHz frequency sweep and (b) zoom over 600 Hz with the displacement amplitude  $X$  plotted on logarithmic axis. The red curve in (b) shows a spectral fit of the data using Eq. (2).

A single, well-defined resonance was observed for all microcantilevers tested. The vibration amplitude  $X(f)$  near the cantilever tip can be modelled by the following relationship [43]:

$$X(f) = \sqrt{\Delta f \left( \frac{2k_B T}{\pi \kappa f_0} \frac{1/Q}{(1-u^2)^2 + u^2/Q^2} + S \right)} \quad (2)$$

Where  $\Delta f$  is the spectral bins bandwidth [43],  $k_B$  is the Boltzmann constant ( $\sim 1.38 \times 10^{-23} \text{ JK}^{-1}$ ),  $T$  is the absolute temperature,  $\kappa$  is the spring constant of the cantilever,  $u = f/f_0$  where  $f$  is the frequency and  $f_0$  is the resonant frequency,  $Q$  is the mechanical quality factor, and  $S$  is the detector noise.

The characterization of several microcantilevers of each type and the fitting of Eq. (2) enabled the quality factor, the resonant frequency, the maximum cantilever amplitude at the tip  $X_{max}$ , and the detector noise to be evaluated—these values are presented in Table 2.

**Table 2.** Summary of the vibrometry measurements (in air) of the silicon microcantilevers fabricated during the study. Averages and standard deviations of the resonant frequency  $f_0$ , the mechanical quality factor  $Q$ , the maximum displacement amplitude  $X_{max}$ , and the spring constant  $\kappa$  of the microcantilever at the tip are given.  $S$  is the detector noise in units  $\text{pm}/\sqrt{\text{Hz}}$ .

| Microcantilever patterning | $f_0$ (Hz)   | $Q$       | $X_{max}$ (pm) | $\kappa$ (N m <sup>-1</sup> ) | $S$ (pm/ $\sqrt{\text{Hz}}$ ) |
|----------------------------|--------------|-----------|----------------|-------------------------------|-------------------------------|
| Process 1                  | 7188.2±18.6  | 119.2±5.8 | 4.83±0.41      | 0.38±0.06                     | 1.05±0.18                     |
| Process 2                  | 6382.4±103.4 | 111±4.2   | 4.97±0.22      | 0.38±0.05                     | 1.26±0.05                     |

We can compare some of these experimental values with those that can be calculated using an analytical approach. The resonant frequency of a fixed-free cantilever (in a vacuum) is given by the following equation [44]:

$$f_0^{vac} = \frac{1}{2\pi} \sqrt{\frac{\kappa}{0.2427\rho_{Si}wLt}} \quad (3)$$

Where  $\kappa$  is the spring constant of the cantilever,  $\rho_{Si}$  is the mass density of crystalline silicon, and  $L$ ,  $w$ , and  $t$  are the microcantilever's physical dimensions. Note that here  $L/w > 5$ , meaning that the normalized effective mass of the microcantilever is 0.2427 in Eq. 3 [45]. The spring constant  $\kappa$  of the microcantilever in Eq. 3 is given by:

$$\kappa = \frac{E_{Si}t^3w}{4L^3} \quad (4)$$

The correction factor  $\alpha$  for the presence of air during the measurements is given by:

$$\alpha = \left(1 + \frac{\pi\rho_{air}w}{4\rho_{Si}t}\right)^{-1/2} \quad (5)$$

The resonant frequency of the microcantilever in air  $f_0^{air}$  is thus given by:

$$f_0^{air} = \alpha f_0^{vac} \quad (6)$$

By using equations 3-6, the relevant physical constants, and experimentally-obtained microcantilever dimensions given in Table 1, the values and variations of the resonant frequency (in air) and the spring constant of the microcantilevers were computed—these values are given in Table 3. The

Young's modulus of silicon  $E_{Si} = 169$  GPa in the  $\langle 110 \rangle$  crystal direction [40] and its density  $\rho_{Si} = 2329$  kg m<sup>-3</sup>. The density of air  $\rho_{air} = 1.2$  kg m<sup>-3</sup>.

| Microcantilever patterning | $f_0^{air}$ (Hz) | $\kappa$ (Nm <sup>-1</sup> ) |
|----------------------------|------------------|------------------------------|
| Process 1                  | 7047±19          | 0.568±0.03                   |
| Process 2                  | 6528±56          | 0.566±0.06                   |

**Table 3.** Calculated values and variations of the resonant frequency  $f_0^{air}$  and the spring constant  $\kappa$  of the microcantilevers based on the experimentally-measured microcantilever dimensions length  $L$ , width  $w$ , and thickness  $t$  given in Table 1.

The experimental resonant frequencies are comparable with those predicted by the analytical approach. The experimental spring constants are lower than those predicted by analytical modelling considering an ideal cantilever. In terms of the mechanical quality factor  $Q$ , the measured values are comparable to those published in the literature for single crystal silicon cantilevers in air [46–49]. The variations in the experimental values can be explained, at least in part, by variations in dimension due to processing. The variations between the experimental values and those predicted by theory can be explained by considering that the microcantilevers here are not ideally-anchored, rectangular cantilevers. The variations of the resonant frequencies are explained by the variations in the microcantilevers dimensions (see Table 1)—these are large in the case of microcantilevers fabricated using Process 2 (the uniquely xenon difluoride-based process) due to a lower etch uniformity observed during the first etch step. In addition, deviations from theory can also be explained by the specific anchoring of the microcantilevers here. First, the rounded shape at the base of the cantilevers caused by using isotropic xenon difluoride etching to define the microcantilevers in Process 2. Second, the overhang of the silicon device layer due to the xenon difluoride under etching in both Process 1 and Process 2. Both these issues could have an impact of the performance of the mechanical behaviour of the microcantilevers to a certain extent. Concerning the first issue, the curvature radius of the rounding at the microcantilever base is  $\sim 15$   $\mu\text{m}$  for a 5  $\mu\text{m}$  thick etched device layer using xenon difluoride (Process 2). This is very small compared to the length of the microcantilevers fabricated here (1000  $\mu\text{m}$ ) and will have negligible effect on the overall mechanical properties of the microcantilever. Indeed, the rounding of the anchoring avoids the sharp angle incurred with dry etching, this should—at least in principle—result in less bending stress concentration. Concerning the second issue, the under etching of the device and BOX layers caused by the xenon difluoride etching cannot be neglected. The effect of this is an ‘overhang’ feature having a width of approximately half the thickness of the cantilever  $\sim 50$   $\mu\text{m}$  for the case here. The stiffness of this overhang can be approximated by using Eq. 4—using an overhang length of 1 mm, this value is 4 orders of magnitudes larger than the stiffness of the microcantilever. In addition,

overhang features are not uncommon in the fabrication of microcantilevers even for relatively short cantilevers [50]. However, we note that a numerical study would be interesting for future work.

#### **4. Conclusion**

A straightforward surface micromachining process has been demonstrated for the fabrication of ‘chip-edge’ silicon microcantilevers starting with silicon-on-insulator material. In principle, the generic nature of the process implies that any pre-patterning of circuitry located on the silicon microcantilever surface would be intact following the whole process. The process involves lithographic masking, xenon difluoride selective etching of silicon, buffered hydrofluoric acid selective etching of silicon dioxide, solvent cleaning, and chip dicing. We have been able to successfully fabricate long, thin chip-edge silicon microcantilevers using the approach. The microcantilever releasing uses xenon difluoride, which does not etch many microelectronics’ processing materials (insulators, metals, photo and electron beam resists, polymers...) other than silicon. The photoresist masking material is not damaged by the process and is relatively simple to remove using appropriate solvents. The maximum temperature of the process is 100°C (required for the photoresist baking) which is advantageous for sensitive pre-fabricated circuitry. If xenon difluoride is used to both pattern and release the silicon microcantilevers, then a single photomask can be used for the whole process. We have also demonstrated that the under etch release process is compatible with a plasma-based etch pattern definition of the microcantilever. The manual cleaving of the silicon wafers, to leave the silicon microcantilevers protruding from the chip edge, means that rapid prototyping is possible by avoiding cumbersome front-to-back processing. Finally, we are not suggesting that the process described here can replace deep etching—on the contrary, plasma-based deep etching is essential for the fabrication of narrow, deep holes and channels in silicon. Rather, we propose an enabling technological process that can be employed for the development, rapid prototyping, and manufacture of silicon microcantilevers containing pre-fabricated circuitry for novel probe applications. In this way, one avoids the relatively cumbersome, expensive, and time-consuming front-to-back processing/deep etching combination. It is our hope that other researchers and engineers will apply our straightforward process for their specific applications.

#### **Acknowledgements**

The work was partly funded by the following projects: The IEMN-HORIBA *Equipe Mixte* project, the TIPTOP\_1 project (ANR-16-CE09-0029), and the French RENATECH network. The authors would like to thank François Vaurette (engineer at IEMN) for electron beam lithography performed during the initial optimization stages and Christophe Boyaval (technician at IEMN) for help in fabrication the photolithographic masks.

## ORCID iDs

Steve Arscott <https://orcid.org/0000-0001-9938-2683>

Vanessa Avramovic <https://orcid.org/0000-0002-0259-5373>

Thomas Lerond <https://orcid.org/0000-0003-3281-1281>

Thierry Melin <https://orcid.org/0000-0003-1777-3512>

Dmitri Yarekha <https://orcid.org/0000-0002-6136-1315>

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