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Investigation of SiC thyristors with varying amplifying gate design

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Due to their superior performance in terms of current density and blocking voltage, silicon carbide (SiC) thyristors are of particular interest for pulsed power applications [1, 2]. Furthermore, in view of the tremendous progress made in SiC crystal quality and wafer size, large-area SiC thyristors appear to be feasible today. In this context, both electrically and optically triggered SiC thyristors require adequate amplifying gate structures. With the aim to investigate this aspect, a mask set featuring numerous SiC thyristor devices with varying amplifying gate structures has been conceived [3]. And based thereon, a 100 mm epitaxial SiC wafer has been processed recently. Resulting from this process run, the present paper reports on the electrical characteristics measured on-wafer as well as on singularized and encapsulated SiC thyristor devices with and without amplifying gate.

The fabricated devices are asymmetrically blocking vertical SiC thyristors, of which the 10 μm thick p-base (drift) layer ($5 \times 10^{15} \text{ cm}^{-3}$) is separated by a 4 μm p-type buffer ($5 \times 10^{17} \text{ cm}^{-3}$) from the wafer substrate ($> 1 \times 10^{19} \text{ cm}^{-3}$). The n-base (gate) and the anode layers have a nominal thickness (and doping concentration) of 2 μm ($1 \times 10^{17} \text{ cm}^{-3}$) and 1 μm ($1 \times 10^{19} \text{ cm}^{-3}$), respectively. The gate and the single-step junction termination extension (JTE) are formed simultaneously by reactive ion etching (RIE). A second RIE step was used to define the JTE length and thus the device mesa. Following the etching, the primary metallization of gate/cathode (Ti/Ni) and anode (Ni/Ti/Al) was created separately by e-beam evaporation, lift-off and subsequent annealing. The surface was passivated with 1 μm thick, deposited SiO_2 . The over-metallization consists of 1 μm Al and 0.7 μm Ti/Ni/Au on the top-side (anode/gate) and the backside (cathode) contacts, respectively

Fig. 1 shows a scheme of circular shaped SiC amplifying gate thyristors with the characteristic dimensions (radii). All fabricated amplifying gate thyristors have a central, circular gate (G) with a radius of $r_{\text{EA}} = 160 \mu\text{m}$ and a main anode (A), expanding from an inner radius of $r_{\text{EM}} = 500 \mu\text{m}$ to a distance of $r_{\text{SM}} = 1200 \mu\text{m}$, where an optional anode short and the beginning of the JTE is situated. With a JTE length of 150 μm and a security margin to the cutting edge, the die size measures 3.2 mm \times 3.2 mm (0.1 cm^2). In-between gate and main anode lies the amplifying gate, consisting of the anode A' of the pilot thyristor and the auxiliary gate G'. The etch-step separating A' and G' forms a circle with varying radius of r_{SA} . This way, the resulting thyristors meet the amplifying gate design criterion ($R_{\text{P}} > R_{\text{M}} \Rightarrow r_{\text{SA}}/r_{\text{EA}} > r_{\text{SM}}/r_{\text{EM}}$) [3, 4] to different degrees: non-adequate ($r_{\text{SA}} = 300 \mu\text{m}$), adequate ($r_{\text{SA}} = 400 \mu\text{m}$), and safe ($r_{\text{SA}} = 460 \mu\text{m}$).

On-wafer (in a vacuum probing chamber), the best devices demonstrated stable blocking up to 2 kV. After dicing, bonding and encapsulation they were successfully tested up to 1.2 kV. Fig. 2 shows the micrograph of one of the fabricated and bonded devices, a square shaped amplifying gate thyristor with dotted anode shorts. Fig. 3 shows on-state characteristics (at varying gate currents) of one of the amplifying gate thyristors (lower graph) compared to a device without amplifying gate. As expected, the amplifying gate thyristor shows a characteristic snap-back and requires a higher gate current to trigger. Fig. 4 shows the gate-anode characteristics of an amplifying gate thyristor, allowing to determine the characteristic resistances R_{P} and R_{M} of pilot and main thyristor, which confirm the application of the above mentioned design rule. Fig. 5 shows turn-on characteristics of SiC thyristors with circular and square shaped anode (cf. Fig. 2), each with varying amplifying gate design. The missing peak-shaped inversion in the gate current transient confirms that the pilot thyristor of non-adequately designed devices is not triggered.

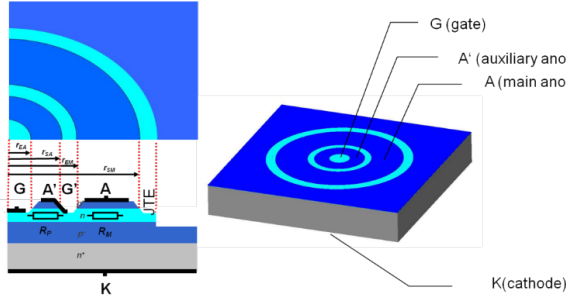


Fig. 1. Scheme of an SiC amplifying gate thyristor.

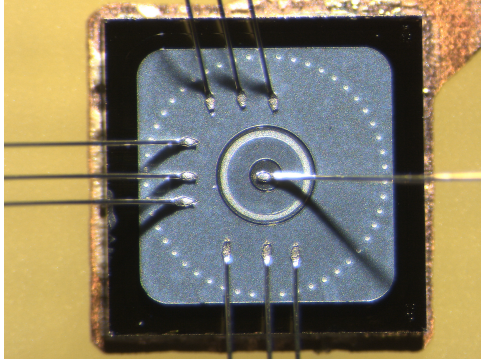


Fig. 2. Micrograph of an SiC amplifying gate thyristor with square-shaped anode and dotted shorts.

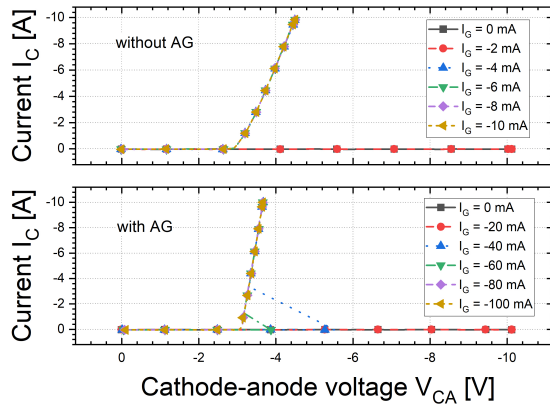


Fig. 3. On-state characteristics of SiC thyristors with and without amplifying gate (AG).

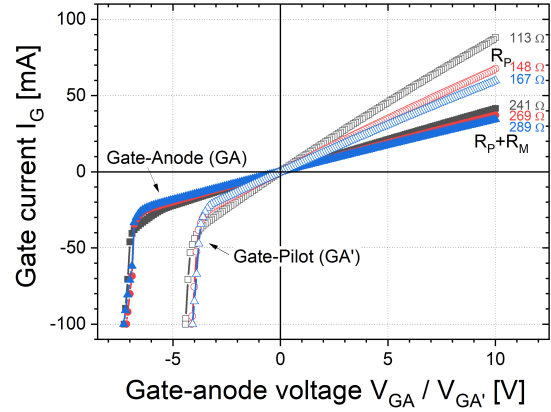


Fig. 4. Gate-anode characteristics of SiC thyristors with differently dimensioned amplifying gate.

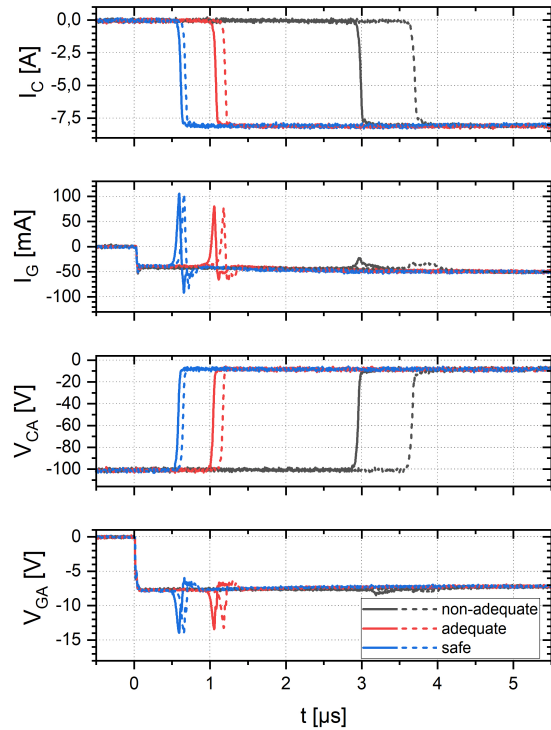


Fig. 5. Turn-on characteristics of SiC thyristors with circular (solid lines) and square shaped (dotted lines) anode, each with differently dimensioned amplifying gate (cf. legend).

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