Electro-thermal limitations and device degradation of SiGe HBTs with emphasis on circuit performance (Invited)

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Abstract— **This paper examines the performance of SiGe HBTs under DC and AC pulsed operating conditions beyond the breakdown voltage. Two state-of-the-art technologies are investigated. The limitations when biasing the transistor at or beyond peak f_T are thermal only, thus penalizing deep trench architectures. Furthermore, the reliability implications are explored and their impact on device degradation is assessed.**

***Index Terms*— SiGe HBTs, avalanche breakdown, self-heating, limitations, reliability, safe operating area (SOA), HICUM compact model, Aging Laws**

I. INTRODUCTION

Today, SiGe BiCMOS is the technology of choice for demanding (sub) mm-wave applications like high-data rate wireless communications, optoelectronic data links, next-generation automotive radar sensors and future novel THz applications. Compared to III-V devices, SiGe HBTs possess attractive thermal and reliability properties as well as a much higher integration density coupled with an efficient BEOL architecture allowing the realization of transmission lines in micro-strip configuration as well as manifold additional passive devices. The only drawback is, however, the lower breakdown voltage (BV) of SiGe HBTs due to their smaller bandgap and the higher current gain β compared to most of the III–V HBTs. Thus, obtaining a high output power density of SiGe HBT-based power amplifier (PA) is a challenging design task.

To achieve this, several strategies are possible.

1- The maximum current swing can be increased by the use of PA-cells composed of multiple emitter finger configurations. The drawback here is related to the design of the input and output matching circuits due to the lower input and output impedances [1] of large area devices.

2- The maximum voltage swing can be increased by operating the device at higher collector voltage. Typically, DC collector-to-emitter breakdown voltage with base open (BV_{CEO}) or DC collector-to-base breakdown voltage with open emitter (BV_{CBO}) are used as the metrics for voltage limit of PA devices. In practical PA circuits, the RF envelope voltage can swing well beyond BV_{CEO} without causing a failure. An analysis of output power swing limitations and DC breakdown is presented with a focus on biasing and temperature in [2].

For both strategies, reliability is a concern.

Other strategies exist that are based on circuit design, which will not be detailed in this paper, but are mentioned for the sake of completeness: In order to increase P_{out} for high-speed HBTs with a relatively low BV_{CEO}, V_{CE} can be improved using a cascode circuit configuration. A cascode PA consists of a stack of HBTs in CB configuration on top of a CE configuration which can thus reduce the output voltage clipping. Note that the number of stacked transistors is limited by the substrate breakdown voltage. Connecting cascodes in parallel further increases the output power and reduces the collector current clipping of the PA [3]. Use of a cascode topology with a low terminating base impedance and minimum voltage-current waveform-overlap extends the V_{CE} swing on the upper SiGe HBT in the cascode beyond its BV_{CBO}, boosting output power and power added efficiency (PAE). [4]

Another option for mm-wave power amplifier design is the use of the Class-E architecture which is an attractive proposition due to its high theoretical collector efficiency as well as higher allowable voltage swing owing to non-overlapping voltage and current waveforms. Specifically, in HBTs the voltage swing can be as high as BV_{CBO} as opposed to BV_{CEO} that sets the limit in linear amplifiers [5].

Finally, pulsed systems such as short-time (ultra-) wideband power amplifiers (UWB-PA) provide essential advantages over continuous wave (CW) PAs in terms of size, weight, and power dissipation for a given output power requirement [6]. These systems can be found in the fields of high-resolution imaging and sensing, precision position location, and wireless networking [7].

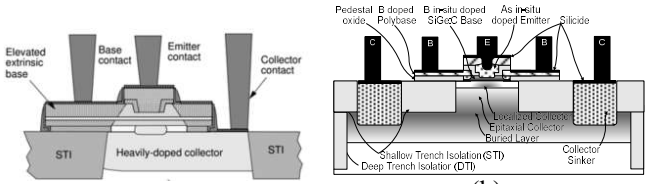
This paper is divided into two parts: First, we will explore the maximum collector-to-emitter breakdown voltage of HBTs under test. The device operates at its best RF-performance (V_{BE} at peak-f_T). Pulsed DC and AC measurements are carried out. Two different state-of-the-art architectures are investigated and their sensitivity to self-heating is explored. In the second part, the device degradation due to operation close to the safe-operating-area (SOA) is analyzed and modelled. After a short presentation of the implemented aging compact HICUM model, the impact of the degradation on circuit building blocks are illustrated.

II. PULSED MODE OPERATION AT BREAKDOWN VOLTAGE AND BEYOND

The DC output characteristics of a bipolar transistor is represented by its I_C (V_{CE}, for different constant V_{BE} values). When investigating these curves for high V_{CE}s, a 1st snapback (or flyback) behavior, i.e., the onset of a negative-differential-resistance (NDR) branch, is observed at medium V_{BE}; it is worth noting that the NDR branch is measured by keeping I_C constant while sweeping V_{BE} and measuring V_{CE} [8]. The 1st snapback is one of the critical borders (edges?) for the safe operating area (SOA), since under V_{CE}-controlled conditions the I_C would sharply and significantly increase beyond that point; at high currents a 2nd snapback occurs, after which a positive-differential-resistance (PDR) branch is restored. The well-known mechanisms described before is valid for medium V_{BE} values only. For high V_{BE}s, the measured I_C–V_{CE} curves show fully PDR behavior (i.e. the 1st snapback does not occur) and are purely limited by self-heating. The SOA is limited by BV_{CBO} at low V_{BE}, and by the pinch-in effect at low-to-medium V_{BE}s [9].

On the other hand, the V_{BE} region of interest is located at high V_{BE}s, where the device operates close to the peak transit frequency (f_T) or f_{MAX}. In order to analyze the impact of self-heating, pulsed measurements are an ideal tool for in-depth investigation. In addition, it provides crucial information for the UWB-PA design. In the present study, pulse measurements are carried out with the pulsed DC analyzer Keithley 4200-SCS in combination with the VNA Rohde & Schwarz ZVA67 (with ZVAX extension unit). The PMU allows to create pulses larger than 60 ns with minimum rise and fall times of 20 ns [10]. Measurements with sufficient accuracy were obtained using a time window between 60% and 90% of the DC pulse duration.

These measurements have been performed on two state-of-the-art technologies as presented in Fig. 1: Fig 1a shows a cross-sectional view of the HBT used here that were from a development lot of a new generation of the 130 nm BiCMOS technology, SG13G3 [11]. It shows an elevated extrinsic base (EEB) with a self-aligned emitter-base architecture created using the NSEG of the base. Its key features include: (i) partially mono-crystalline EEB regions are formed self-aligned to the emitter, facilitating low extrinsic base resistances R_{BX}; (ii) the formation of the high-speed HBT device within a single active area without shallow trench isolation (STI) between the emitter and the collector contact regions, resulting in low R_C and small collector-substrate junction areas. The HBTs feature peak f_T/f_{MAX} values of 470/650 GHz. The cross sectional view from Fig. 1b transistor shows the B55 technology from STMicroelectronics (ST). It presents the DPSA-SEG architecture, which is well-known for its very popular and fully self-aligned structure. The architecture exhibited state-of-the-art performances of 320 GHz f_T and 370 GHz f_{MAX} for the 55-nm SiGe BiCMOS [13].



(a) (b)

Fig. 1: Cross-section of a) EEB architecture SG13G3, b) the 55-nm Si/SiGe BiCMOS architecture

Although, it is not recommended for circuit applications due to transistor instability and reduced frequency performances, we have operated the transistors well beyond their SOA to gain a deeper understanding of the ultimate limit of these technologies and verify the accuracy of the electro-thermal model.

Results of DC pulsed measurements from both technologies are shown in Fig. 2.

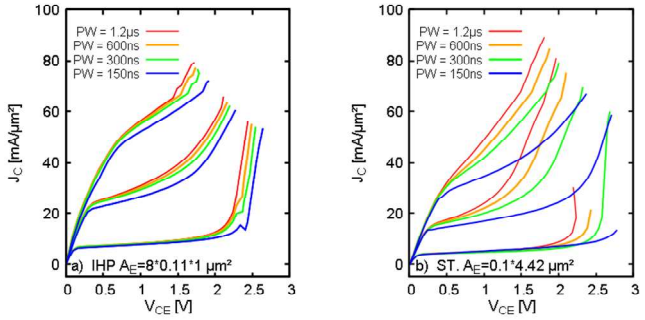


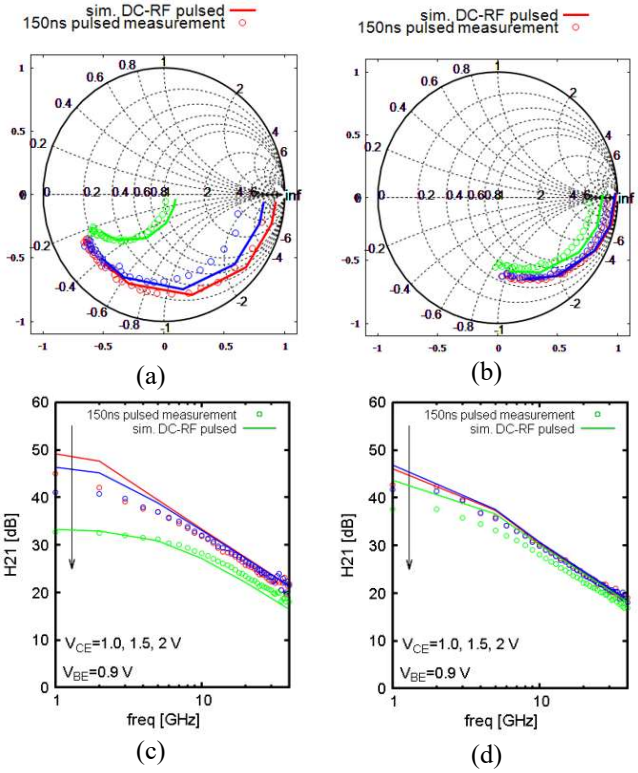
Fig. 2: Output characteristics for V_{BE} = 0.85, 0.9 and 0.95 V measured with various pulse widths from 150 ns up to 1.2 µs for an HBT with (a) A_E = 8*0.11 × 1.0 µm², and (b) A_E = 0.1 × 4.42 µm², duty cycle DC is 10%

We can observe that (i) under pulsed conditions, the transistor can operate well beyond the SOA (maximum allowed V_{CE} is 1.6 V for case (a) [11] and 1.5 V for case (b) [13]), (ii) a high impact of the pulse width on the collector current, which is directly linked to the dynamic self-heating, (iii) this impact is much more pronounced for the transistor presented in Fig. 2b compared to Fig. 2a.

Two main structural differences between both technologies, apart from the EEB in the case of the IHP technology, can be noted: (i) the fragmented emitter for IHP HBTs with 8 unit cells of 0.11 × 1.0 µm², (ii) the presence of the deep trench isolation schemes in the ST technology. Deep trenches are known to confine the heat flux resulting in a higher thermal resistance. Additionally, the dynamic behavior is altered as can be observed from Fig. 2 where, for a given V_{BE}, different pulse widths have been applied. The question now arises on how the transistor behaves for pulsed AC operation.

In Fig. 3, we show AC pulsed measured data, for a DC pulse width of 150ns and an RF pulse width of 50ns. The applied V_{BE} voltage is 0.9V while the V_{CE} varies between 1.0V, 1.5V and 2.0V. The results shown in Fig. 3 are quite unexpected: On the LHS of Fig. 3 (IHP), the small–signal parameters are much more sensitive compared to the figures of the RHS (ST). On the other hand, the pulsed DC voltages have a much higher impact on the collector current for the ST technology (RHS). These two

results seem to contradict each other and need more explanation. When we examine the collector current density at V_{BE}=0.9V, we recognize that for the IHP technology (LHS), J_C is higher (up to two times for a V_{CE}=2V). That implies, that even with a lower thermal resistance, due to the absence of deep trenches, the final device temperature is much higher making the small signal parameters more sensitive to a variation of the operating point (different V_{CES}), even under pulsed conditions. Here the minimum pulse widths is 150 ns and even for this short pulse width, self-heating is already noticeable (see also the pulsed DC curves at V_{BE}=0.9V in Fig. 2). In fact, the absence of DTI leads to a very small self-heating (thermal?) time constant. Hence, despite the short pulses, the pulsed measurements are not adequate to reduce self-heating in the case of the IHP technology. In the case of ST, the pulsed measurements can indeed reduce the self-heating, especially the part due to DTI, which has a much higher time constant compared to the intrinsic part. Using the HICUM L2 compact model, we estimate that the reduction of self-heating due to pulsed measurement is up to 50 % for the case of the ST devices. This analysis is confirmed by HICUM L2 compact model simulation. In order to achieve a quite good agreement with simulation, as shown in Fig. 3, the temperature dependence of R_{TH} requires particular attention for modeling, which underlines the dominance of the thermal effect.



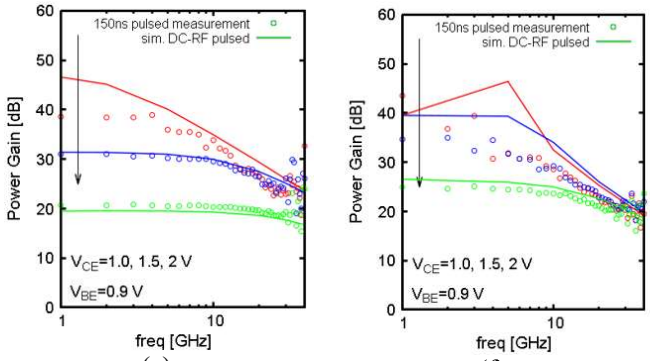
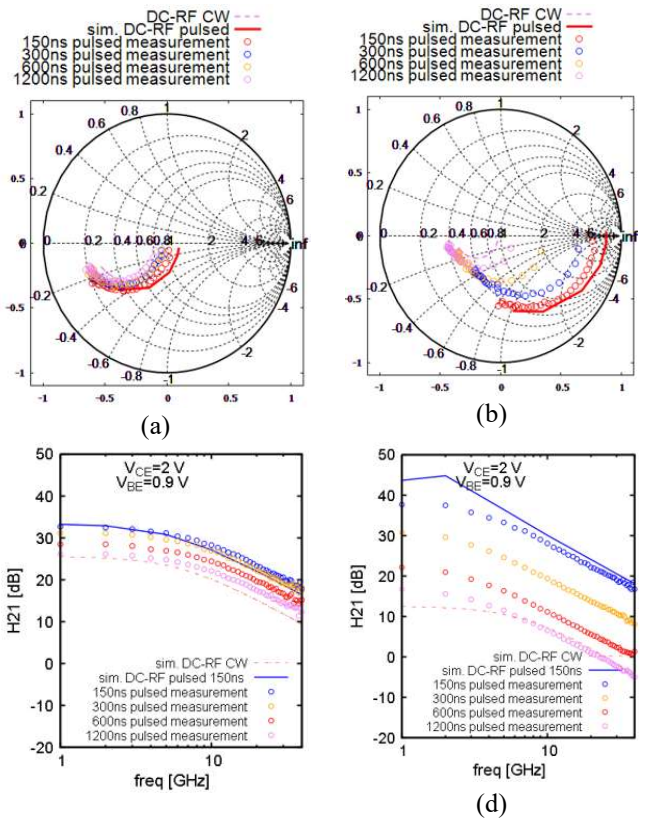


Fig. 3. Pulsed measured AC data, (a) S_{11}-IHP, (b) S_{11}-ST, (c) h_{21}-IHP, (d) h_{21}-ST, (e) Mason gain-IHP, (f) Mason gain-ST for an DC pulse width of 150ns and an RF pulse width of 50ns. The applied VBE voltage is 0.9V and VCE varies: VCE=1.0V (red), 1.5V (blue) and 2.0V (cyan), frequency varies from 1 to 40GHz, duty cycle DC is 10%, duty cycle RF is 3%

In Fig. 4, we present again the S_{11} and the small-signal current gain h_{21}, this time only for one operating point (beyond BV_{CE0}: V_{BE}=0.9V and V_{CE}=2V), but for different pulse widths. Here we observe that the variation in the small-signal parameters is much more pronounced in the case of the ST technology (Fig 4. b and d) compared to the IHP one (Fig. 4 a and c). We attribute this behavior again to the presence/absence of deep trenches. Without deep trenches (IHP) the heating is quite fast and the final steady thermal state is reached in a short time; whereas in the presences of deep trenches, a second/third time constant delays the heating mechanism. When comparing the results to simulation, we can observe that in both cases the results obtained using longer pulses tend to match with the DC-RF continuous wave simulation results.



(c)

Fig. 4. Pulsed measured AC data, (a) S_{11}-IHP, (b) S_{11}-ST, (c) h_{21}-IHP, (d) h_{21}-ST for V_{BE}=0.9V and V_{CE}=2V for different pulse width, duty cycle DC is 10%, duty cycle RF is 3%

In this section, we have demonstrated the benefit of operating the device under pulsed conditions that allows the devices to enter the Safe Operating Area and thus to deliver high output power density. The downside of this approach is that reliability issues that are related to temperature and avalanche mechanisms [14] may occur. We will investigate these issues in the following part of the paper.

III. RELIABILITY ANALYSIS: FROM DEVICE TO CIRCUIT

High base-collector voltage results in creation of electron-hole pairs (avalanche mechanism) where the holes may give rise to hot-carrier degradation (HCD). The underlying mechanism of HCD is trap generation at the emitter-base (EB) spacer oxide interface through Si-H bond-breaking followed by non-ideal base current degradation [15]. The schematic in Fig. 5 (a) illustrates the HBT structure in which HC damage is located near the E-B spacer which is followed by subsequent Si-H bond breakage at the [15-18] oxide interface and H-diffusion into the oxide (Fig. 5(b)).

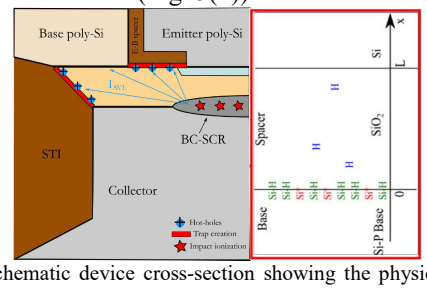


Fig. 5: (a) Schematic device cross-section showing the physical location of HCD, (b) H-diffusion scenario at the E-B spacer oxide interface.

A. Analytical model formulation

The rate of bond dissociation is governed by a chemical interaction between the carriers and the passivated Si-H bond through generation and annihilation of traps. The interface-trap density, $N_T(t)$, increases with the net rate of reaction and the bond dissociation rate can be calculated following reaction-diffusion theory [19] as follows,

$$\frac{dN_T}{dt} = K_F\left(N_F - N_T(t)\right) - K_R N_T(t) N_H(0,t) \qquad (1)$$

K_F is the rate constant of the forward reaction, *i.e.*, generation of traps, K_R is the rate constant of trap annihilation by hydrogen atoms, $N_H(x,t)$ is the volumetric density of hydrogen at distance x of the Si/SiO_2 interface and N_F is the total number of available bonds that can break.

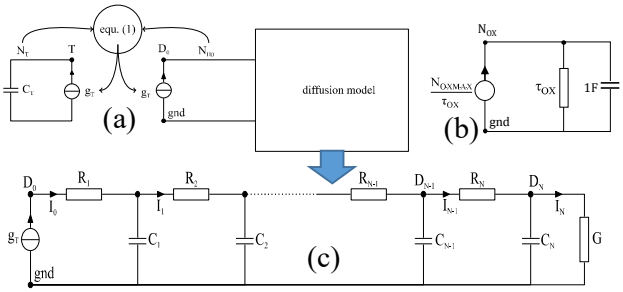


Fig. 6: Organization of the (a) R-D, (b) OT and (c) Diffusion modules of HICUM AL V3.01.

From a compact model point of view [20], the trap creation at the Si/SiO_2 interface (Fig. 5 (a)) can be represented by the change in a specific base current parameter, the peripheral B-E recombination saturation current, I_{REpS} [21-22]. As it has been made evident in earlier works [15, 21-22] that the region around the emitter periphery is solely impacted by HCD, the effect of degradation on the internal base-emitter current parameters can be neglected. In [21], we used TCAD simulations along with HICUM compact model simulations to correlate the increase of I_{REpS} with that of the trap density at the spacer interface (Fig. 6(a)) for a given emitter perimeter, P_E, through the following equation,

$$I_{REpS}(t) = \alpha P_E N_T(t) \qquad (2)$$

In addition to this setup, HICUM AL V3.01 employs an additional fictitious transistor node for the oxide trap generation through the total oxide trap density $N_{OX}(t)$ (Fig. 6 (b)) which is governed by an exponential stress time dependence similar to the implementation of bulk trap in [23]. Finally, in addition to trap generation and creation of H-atoms (Fig. 5 (a) and (b)) through Si-H bond dissociation, the H- diffusion is modeled by an N-stage RC ladder network terminated by a conductance G (Fig. 6 (c)) that represents the long-term diffusion scenario [21-22]. This R-C network considers all possible diffusion scenarios based on Fick's law of H-diffusion [24].

B. Device Aging Simulation

Following an initial HICUM model calibration against experimental data using foundry-generated model cards, HICUM AL V3.01 simulations were validated against aging-tests performed on SiGe NPN HBTs from Infineon Technologies [9], NPN SiGe HBTs [13] based on an advanced BICMOS 55nm technology from ST, as well as on the SG13S technology from IHP [12]. Note that, even though a particular type of stress condition was validated for all the different technologies, with the aging tests conducted at different times, only selected results from each are shown, simply to highlight the versatility of the HICUM AL V3.01 across technologies and aging conditions and not to intent a 1-to-1 comparison between the different technologies. Fig. 7 shows the evolution of I_{REpS} as a function of stress duration for the three technologies under study and corresponding HICUM AL V3.01 simulations, depicting very good accuracy and versatility of the model.

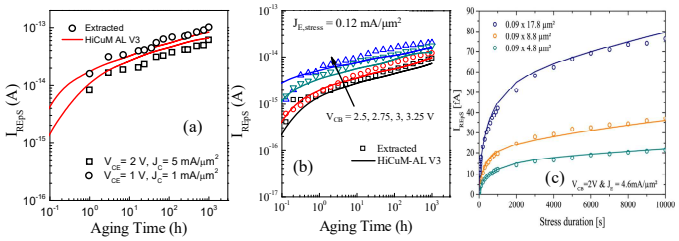


Fig. 7: Comparison between aging tests and HICUM-AL-V3.01 simulation: Evolution of excess base current at V_{BE}= 0.7 V for HBT technologies from (a) Infineon [25], (b) IHP [22] and (c) ST [13].

Next the model simulations were validated against dynamic mixed-mode aging tests conducted on two of the technologies under test in order to affirm time-invariance of the aging

compact model. Fig. 8 (a) shows the results for HBTs from IHP under a specific DC mixed-mode stress condition of $I_{E,stress}$ of 0.12 mA and a $V_{CB,stress}$ of 3V. Both V_{CB} and I_E were programmed to switch in an interval of 360s, between the initial ($V_{CB,stress}$ of 3V and $I_{E,stress}$ of 0.12 mA) and a high-current recovery phase ($V_{CB,stress}$ of 0V and a $I_{E,stress}$ of 5.2 mA at 3 times the current at peak-f_T). Significant recovery can be observed during the high-current phase ($V_{CB,stress}$ = 0 V), owing to the temperature-annealing effect during this phase. In contrast, for the results depicted in Fig. 8 (b) for ST technologies, a series of stress conditions were used that include $V_{CB,stress}$ bias switching between high and low states (without triggering the thermal/ annealing phase). The results show the evolution of the HiCuM parameter I_{rEpS}, an indicator of the trap generation at the E-B spacer oxide interface, depicting little to no recovery when the stress bias is lowered. This affirms that without annealing or some sort of temperature treatment (as done for Fig. 8(a)) HC induced damage do not show any recovery in SiGe HBTs. Due to the difference in spacer morphology and emitter dimension for both of these technologies, slightly different dynamics of trap generation and H-diffusion have been observed. However, despite the mismatch in current densities, geometries and H-diffusion scenarios, recovery is not observed for either technology without an annealing cycle.

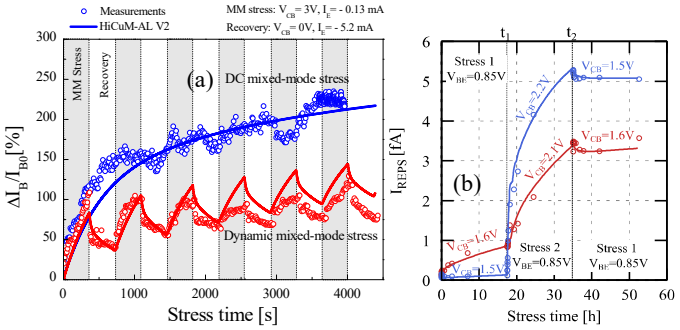


Fig. 8: Evolution of excess base current under dynamic mixed-mode stress conditions comparing the measurements (symbols) and HICUM-AL V3.01 (line) for the technologies from (a) IHP [12] and (b) ST [13].

C. Circuit Aging Simulation

To evaluate the electrical performances of four current mirror architectures (Fig. 9) under mixed-mode operating conditions circuit simulations have been performed for a maximum stress duration of 1000 h using HICUM AL V3.01 for a transient simulation time of 10 µs (with an accelerating factor, ATSF of 3.6×10^{11}) [15, 21]. The following analyses demonstrates how HICUM AL V3.01 can be used in circuit simulation in order to clearly identify the weakest circuit elements, thus allowing the designers to improve the circuit robustness and performances.

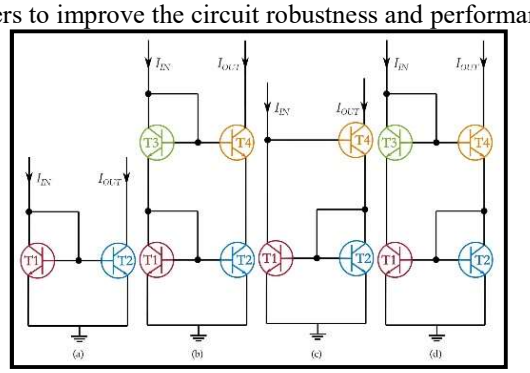


Fig. 9: Schematic of (a) the simple, (b) the cascode, (c) the Wilson and (d) the balanced Wilson current mirrors.

To assess the robustness of the current mirror configurations in Fig. 9, the output voltage is set to 3 V while the input current is kept constant at a value of 100 µA. The transistor operating points for each current mirror configuration are shown in Fig. 10 (a). It can be observed that the transistor T2 from the simple current mirror operates under strong avalanche conditions, with an equivalent V_{CB} of 2.25 V. Moreover, the output transistors (T4) of the cascode, Wilson and balanced Wilson also exhibit a large V_{CB} of 1.5 V and a V_{CE} of 2.25 V, well beyond the conventional BV_{CEO}. This particular operating condition for the current mirror configurations likely leads to mixed-mode operating stress induced degradation due to the activation of the impact-ionization mechanism for several transistors. From Fig. 10 (b), it can be observed from the I_{REpS}s of different transistors that only four transistors suffer from hot-carrier degradation: the transistor T_2 of the simple current mirror and the transistors T_4 of the three other configurations. However, even if the transistor is significantly impacted by HCD under mixed-mode stress, circuit electronic functions are not influenced by HCD, as the transfer current ratio does not evolve over the stress duration.

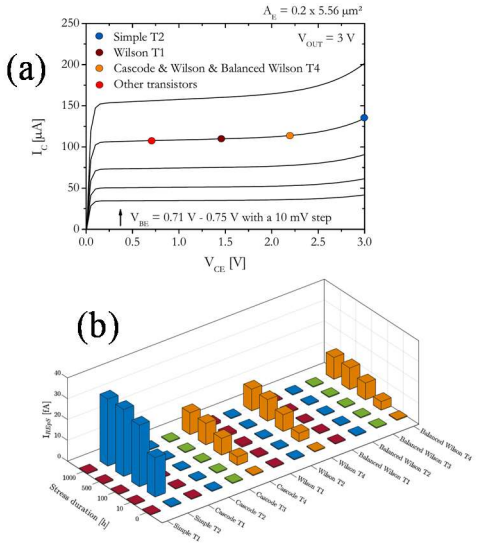


Fig. 10: (a) I_C - V_{CE} characteristics highlighting the operating conditions for each current mirror configuration and (b) evolution of I_{REpS} as a function of stress duration for different transistors of the current mirror configurations at I_{IN}= 100 µA, V_{OUT}= 3 V.

D. Aging Tests on a broadband amplifier

Following the circuit simulation study in the preceding section, HICUM-AL v3.01 has been validated against dynamic aging test results on an actual test circuit, a broadband amplifier [26], fabricated by IHP Microelectronics. As depicted in Fig. 11, the circuit consists of 11 high-speed SiGe HBT from IHP's SG13S technology, with differential inputs (InP and InN) and outputs (OutP and OutN), along with three DC supplies, I_{CM} (common mode), V_{CCi} (input), and V_{CCo} (output).

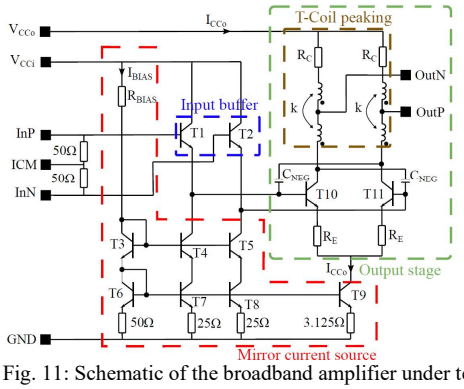


Fig. 11: Schematic of the broadband amplifier under test.

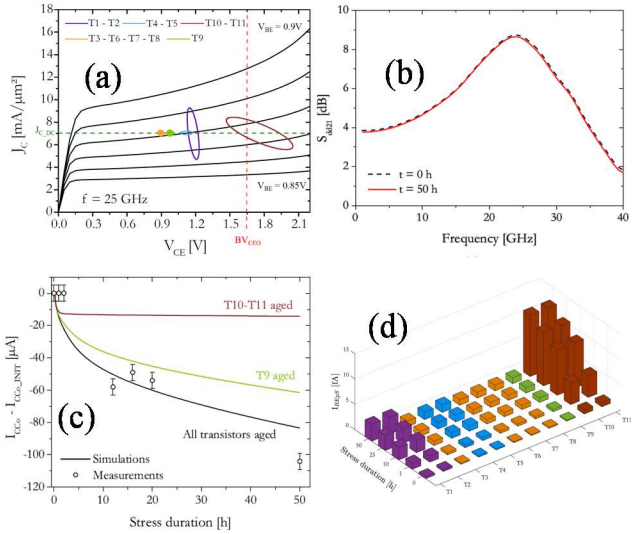


Fig. 12: (a) $J_C - V_{CE}$ characteristics highlighting the operating conditions of different transistors, (b) evolution of differential gain after 50 h of aging test, (c) evolution of output supply current showing measurement (symbols) and simulations (lines), (d) evolution of model-extracted I_{REpS} for the 11 transistors.

A dynamic aging stress test is performed on the test structure by applying an input RF power of -15 dBm at I_{CM} = 3 V, V_{CCi} = 3.3 V, V_{CCo} = 3.7 V and T_{AMB} = 25°C. The corresponding operating conditions of the 11 transistors are summarized in Fig. 12 (a). Note that, all transistors, excepted T10 and T11, are biased below their B_{VCEO}s, so as not to activate HCD for the other transistors, whereas both self-heating and weak avalanche may occur. On the other hand, a larger degradation of T10 and T11 is expected due to their biasing beyond B_{VCE0}. As observed from Fig. 12 (b), the differential gain S_{dd21}, exhibits negligible variation (0.06 dB) after 50 hours of RF stress, which can be attributed to equipment calibration shift over time. Thus, the circuit figures of merit are not altered by HCD. However, a degradation of the output supply current I_{CCo} of 100 µA has been measured (symbols in fig. 12 (c)), after 50 hours of RF stress. To identify the source of this degradation, Fig. 12 (d) shows the evolution of the I_{REpS} for different transistors. To complement this analysis, first, the black curve in Fig. 12 (c) was obtained by turning the aging flags on for all transistors that shows a total of 80 µA reduction in the output supply current compared that closely matches the results obtained from aging tests (symbols), thus validating the accuracy of the aging compact model on circuit level. Next, in order to systematically locate the circuit elements most susceptible to hot-carrier degradation, the aging flag was only activated for T10 and T11, i.e. transistors with the highest I_{REpS} in Fig. 12 (d), thus obtaining the brown curve in Fig. 12 (c), reflecting only 10 µA deviation in the output current during the stress duration. Finally, as inferred by the analysis in section C that output stages are principally affected by HCD, the aging flag was turned on for T9 only. The corresponding simulation result is depicted by the green curve in Fig. 12 (c) where a 60 µA reduction is observed in the output supply current, close to the case where all transistors are aged. This indicates that the main contribution for the variation of I_{CCo} comes from the impact of hot-carrier degradation on T9 which leads to a reduction of its current gain [27].

IV. Conclusion

The search for high output power density in the SiGe HBT power amplifier leads to operate the transistor at high collector-emitter voltage, often close or beyond the save operating-area. Biasing state-of-the-art SiGe HBTs at peak f_T or beyond provokes noticeable self-heating and the SOA is thermally limited. Under pulsed operation (DC and AC), these limits can be exceeded, but small-signal parameters are very sensitive to the applied pulse width. From a technological point of view, we observed that deep trench isolation has a huge negative impact at high current densities and medium to high V_{CE}. The resulting device degradation when operating the transistor at high I_C and/or V_{CE} does not necessarily entail a degradation of circuit performance. A study of different current mirror configurations has shown that despite the fact of device degradation due to HCD, the circuit electronic functions are not altered. However, a similar study on a broadband amplifier shows a significant evolution of the output supply current whereas the differential gain is not affected by the aging.

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