
Compact Modeling and Parameter Extraction Strategies for InP Double Heterojunction Bipolar Transistor

Chhandak Mukherjee¹, Marina Deng¹, Cristell Maneux¹,
Colombo Bolognesi², Virginie Nodjiadjim³

¹IMS Laboratory, UMR CNRS 5218, University of Bordeaux, France

²ETH Zurich, Switzerland

³III-V Lab, jointly between Nokia, Thales and CEA-LETI, France

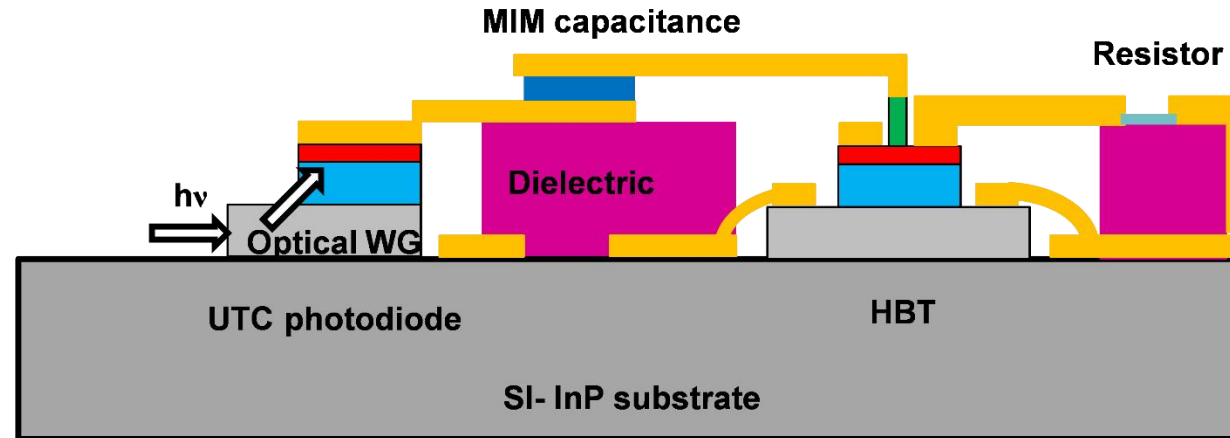
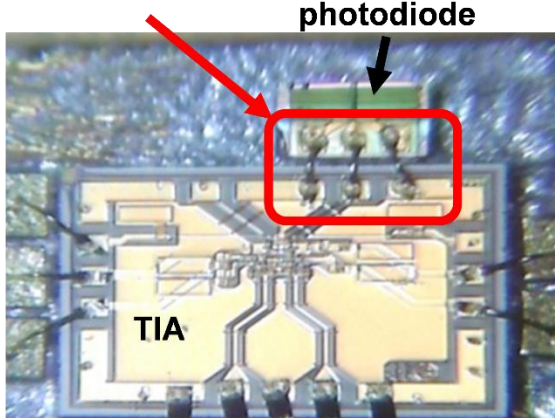
chhandak.mukherjee@ims-bordeaux.fr

Outline

- Context
- Parameter extraction flow
 - HiCuM compact model organization
 - Scaling equations
 - Parameters extracted at Low/Medium injection
 - Parameters extracted at High injection
 - Thermal parameters
- Scalable Model validation for two III-V DHBT technologies
- Extrapolated model simulation for high-frequency on-wafer TRL measurements
- Predictive model simulation: extrapolation of device performances to scaled node

Context

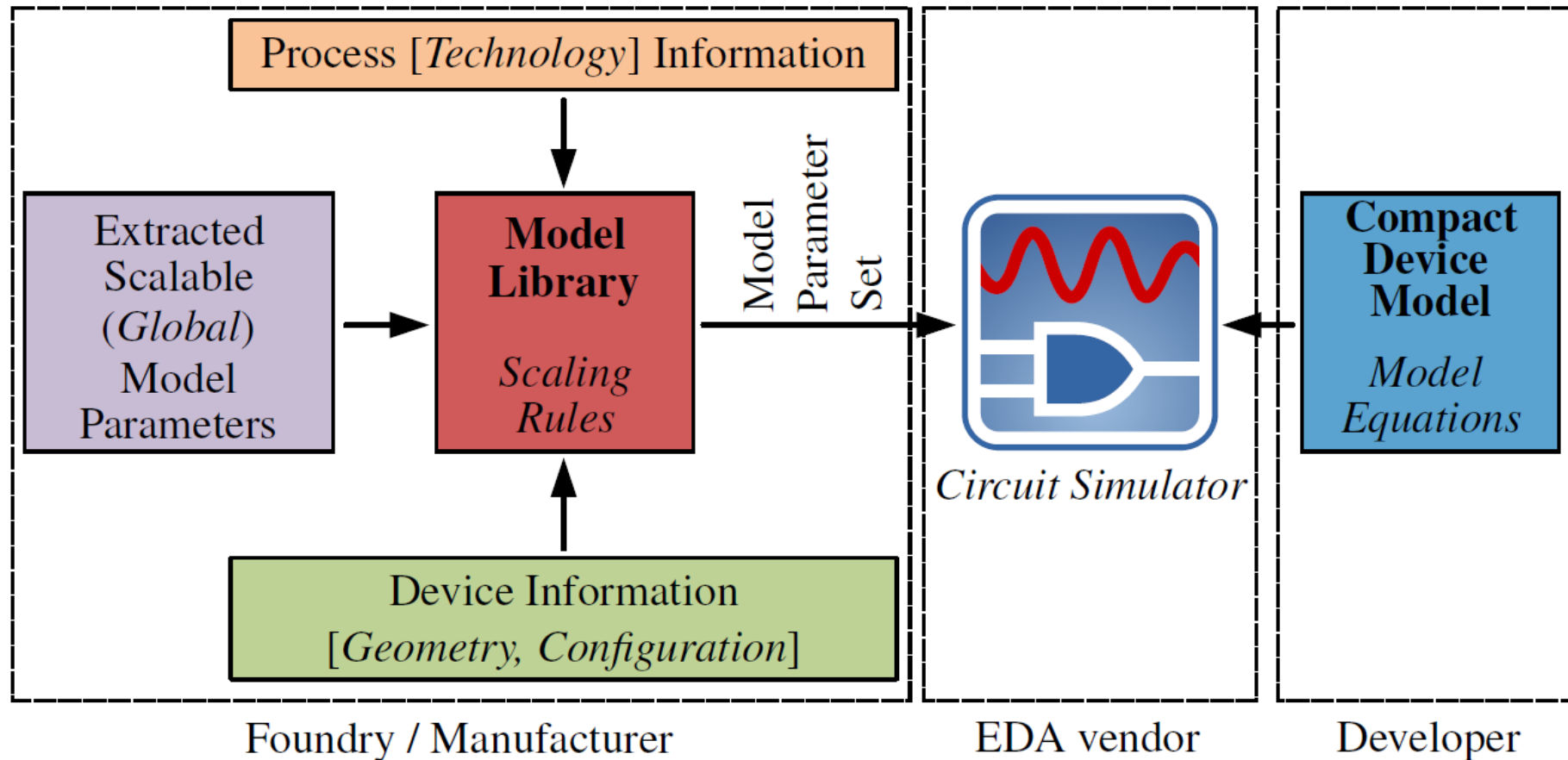
Pads&interconnects



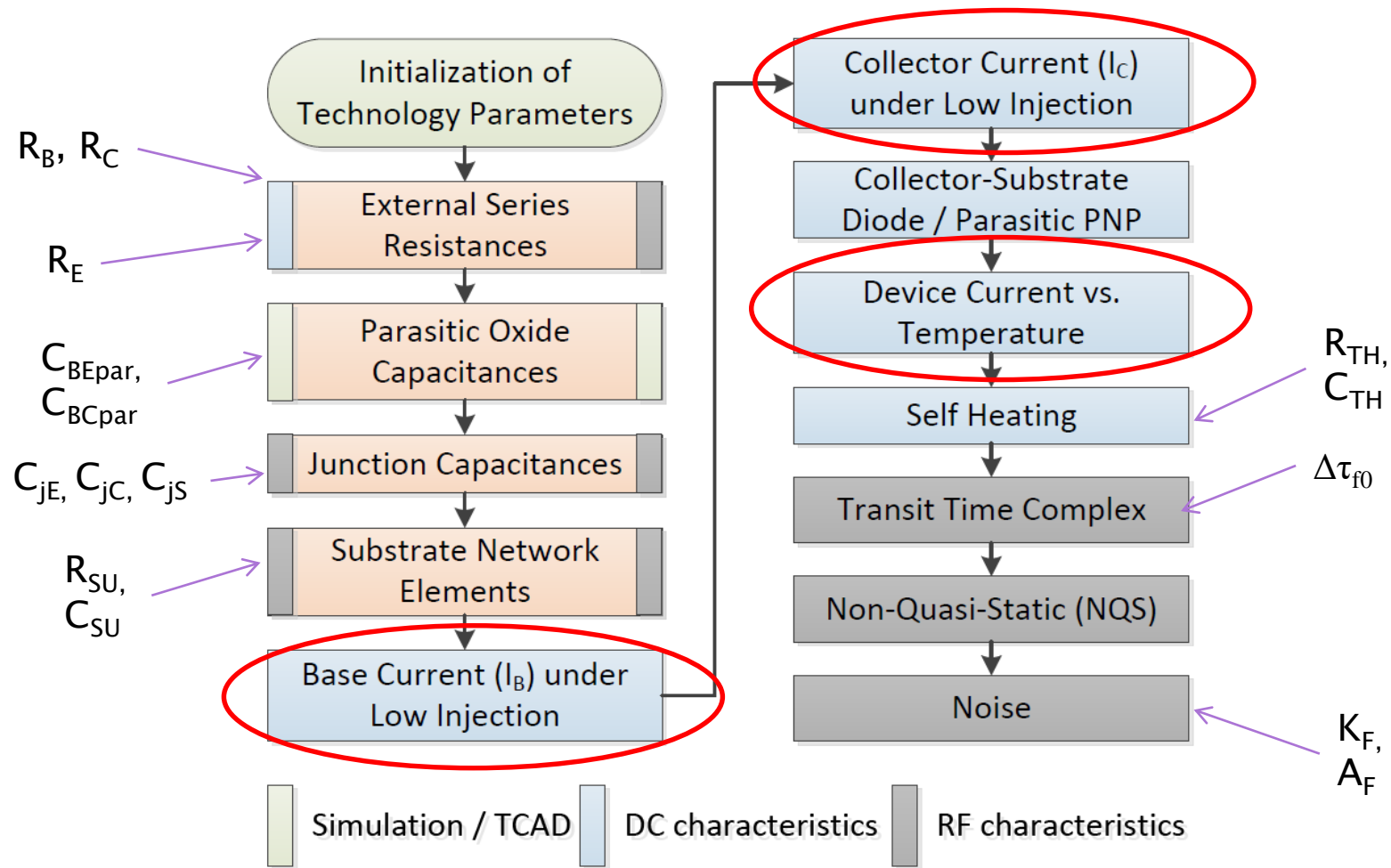
- Monolithic integrated optoelectronic technology
 - III-V DHBTs on InP substrate (amplifier)
 - InP UTC photodiodes (photodetector/optical generation)
- Challenges
 - Optimized epitaxial design
 - Minimize distance and propagation losses
 - Mutual thermal coupling/thermal failure
 - Interconnect modeling at HF
 - Multiphysics simulator (EDA compatible)

Compact Models

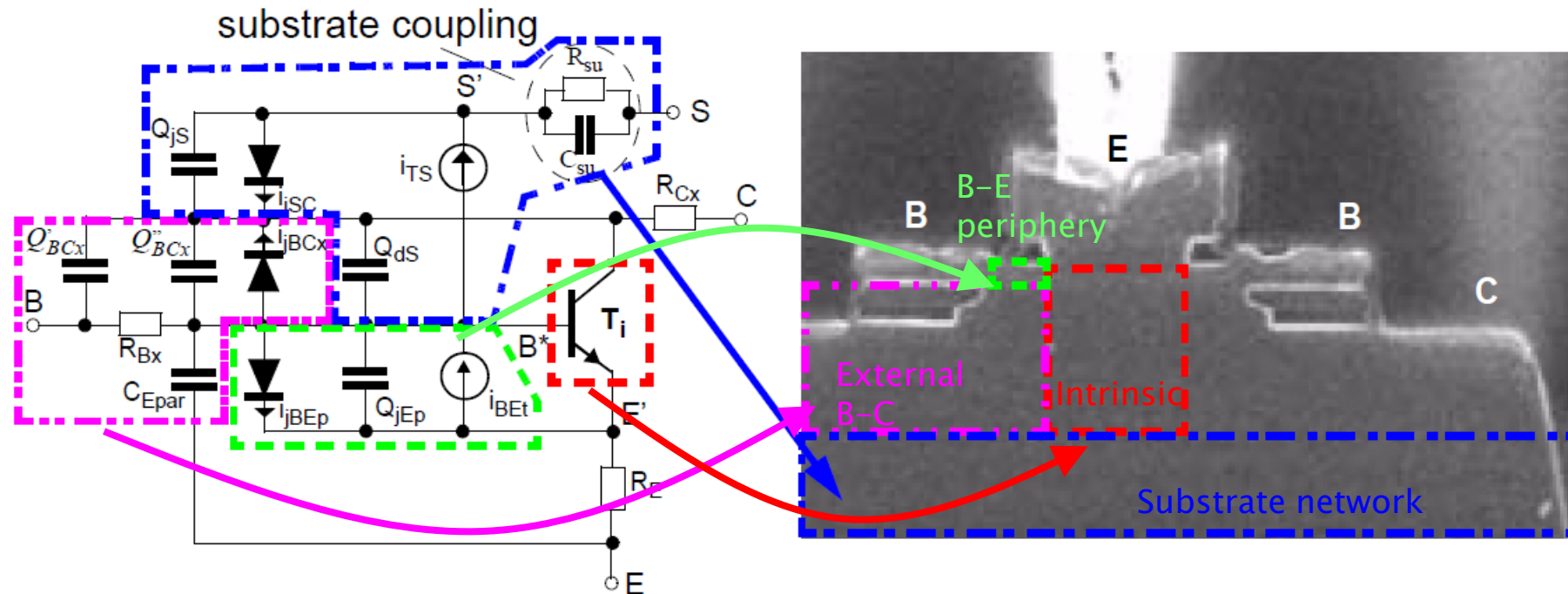
Electronic Design Flow



Model Parameter Extraction Flow

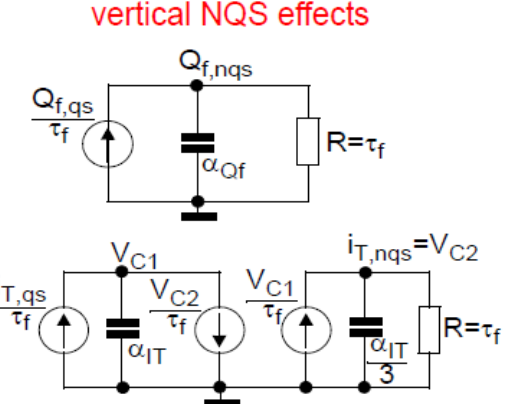
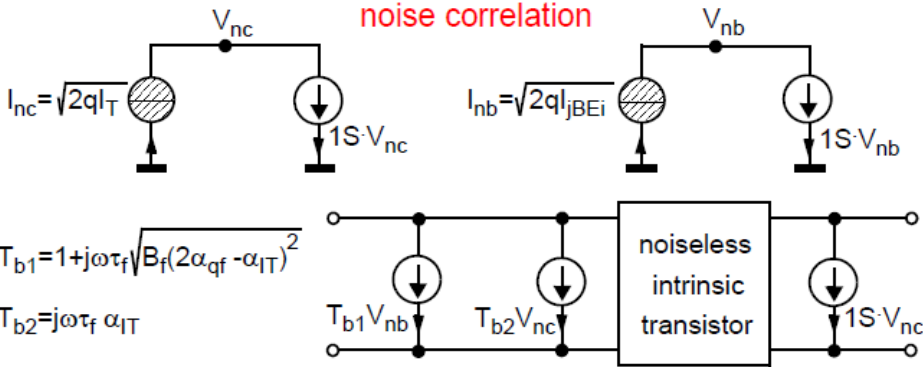
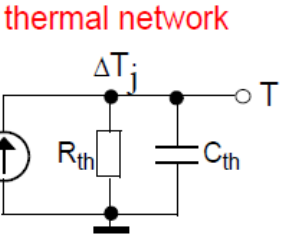
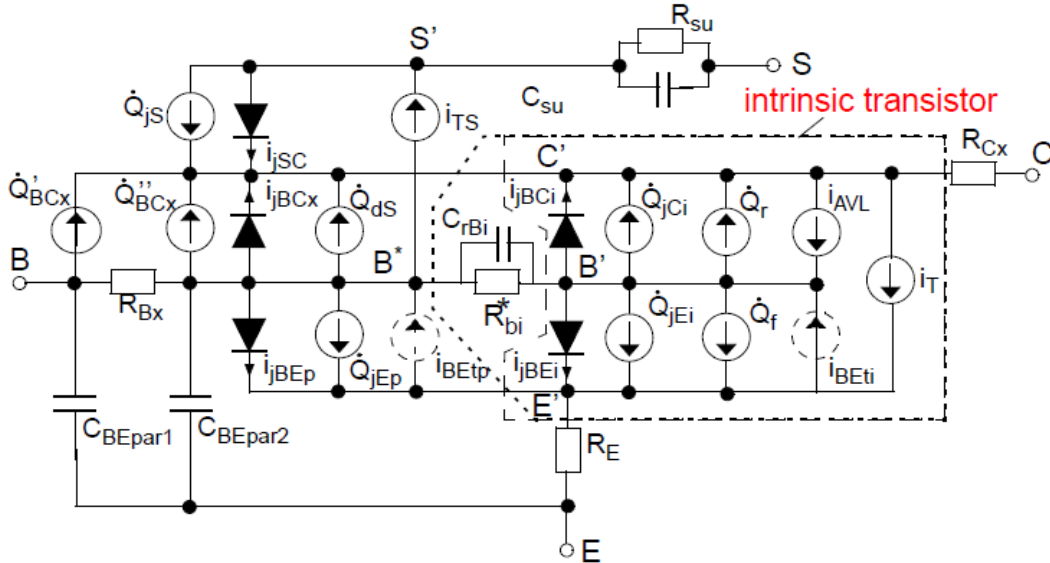


HiCuM Compact model for HBTs



- Captures **Dynamic** behavior of bipolar transistors
- Accurately modelling of **charge storage** in intrinsic and extrinsic device
- 60 parameters for 2D transistor (**Powerful but Complex** parameter extraction)
- At high current: strong correlation between model parameters
- Scaling friendly: custom spice libraries for implementing **scaling rules**

HiCuM : Complete Equivalent Circuit



*M. Schröter and A. Chakravorty, "Compact Hierarchical Bipolar Transistor Modeling With HiCuM" International Series on Advances in Solid State Electronics and Technology, November 2010

Geometry Scaling Strategy

- Capacitance scaling (vs Area and Perimeter)

$$C_j = C_{jA} A + C_{jP} P \quad (C_{jA} \text{ and } C_{jP} \text{ are physics based model parameters})$$

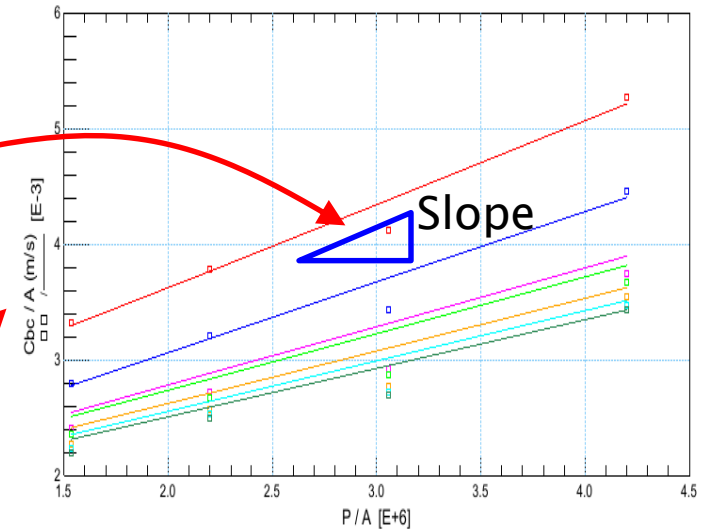
- Rewriting in a more suitable form:

$$\frac{C_j}{A} = C_{jA} + C_{jP} \frac{P}{A}$$

- Parameters can be extracted graphically

$$\frac{C_j}{A} = C_{jA} + C_{jP} \frac{P}{A}$$

Y intercept

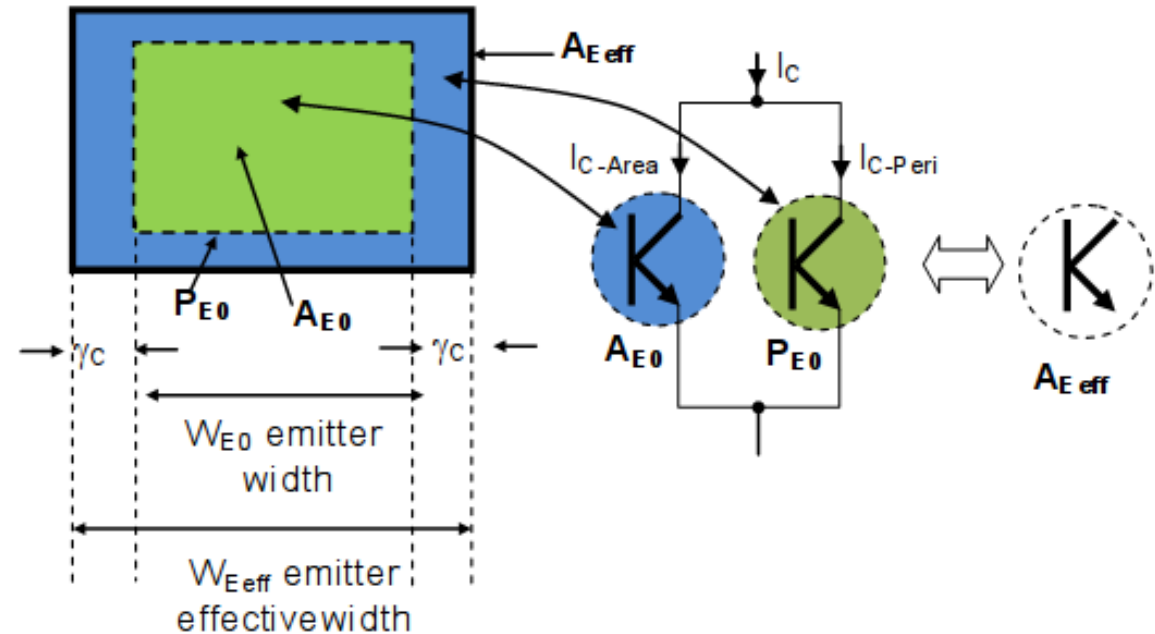


Parameter Scaling Equations

- Current scaling (vs Area and Perimeter)

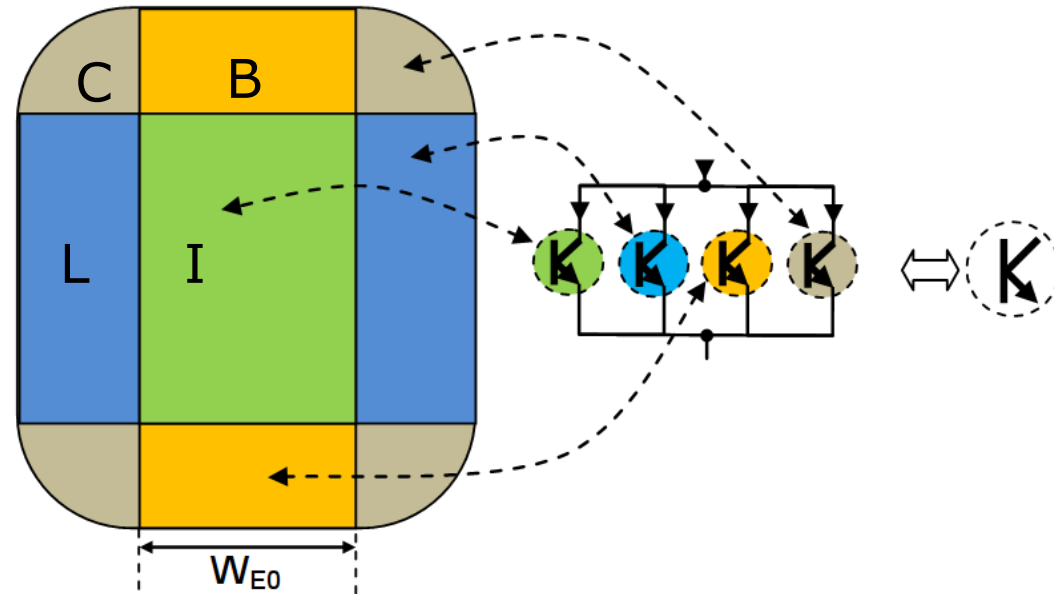
$$I_C = I_{CA} A_{E0} + I_{CP} P_{E0} \qquad I_C = I_{CA} A_{E0} \left(1 + \frac{I_{CP} P_{E0}}{I_{CA} A_{E0}} \right)$$

$$I_C = I_{CA} A_{E0} \left(1 + \gamma_C \frac{P_{E0}}{A_{E0}} \right) = I_{CA} A_{Eeff}$$



Parameter Scaling Equations [contd.]

- Generalized concept: Every parameter can be represented by four components (B, C, I, L)



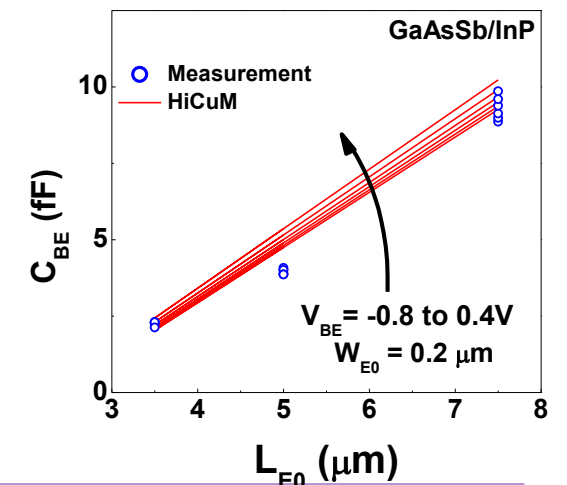
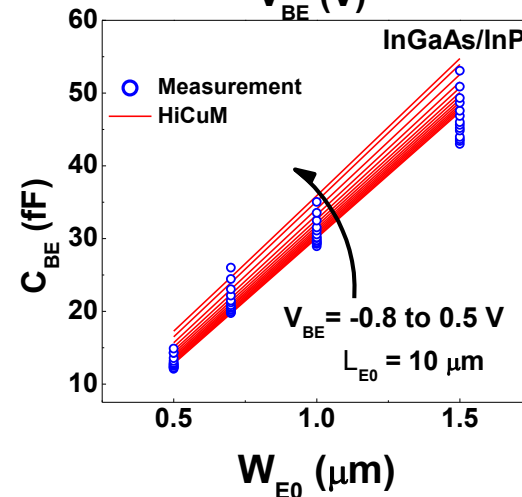
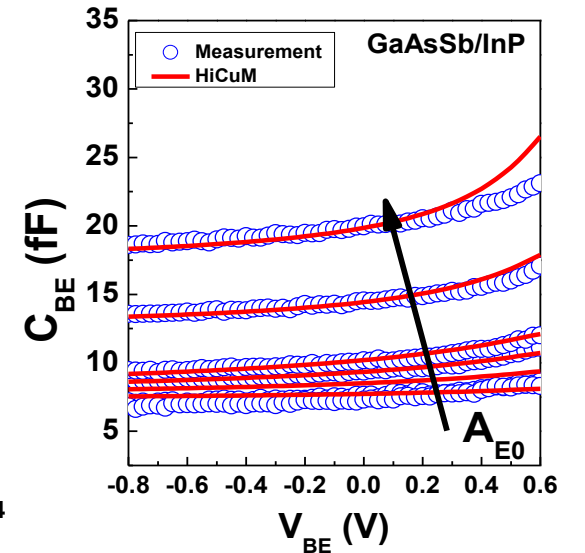
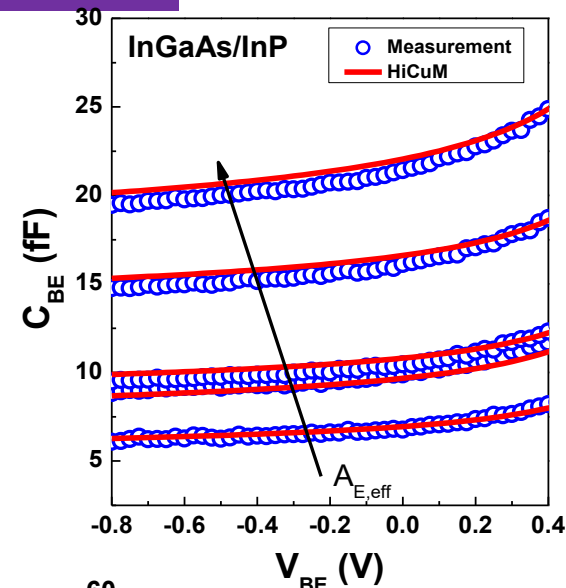
- Before model parameter extraction, some technological parameters are pre-calculated/declared (zero-bias hole charge, area and perimeter dimensions, design rules and process layout information)

Parameter Extraction: C_{BE}

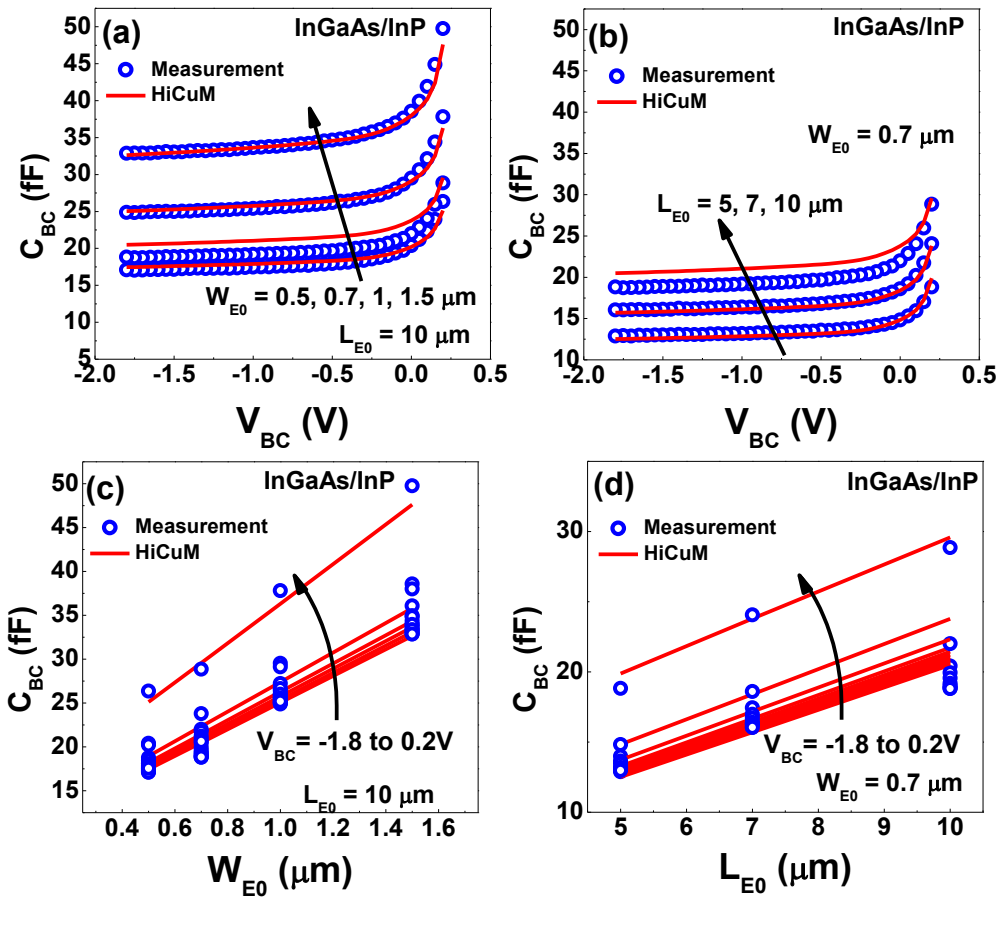
AVAILABLE DEVICE GEOMETRIES FOR THE III-V DHBTs

III-V HBT Technology	Drawn Emitter Length, L_{E0} (μm)	Drawn Emitter Width, W_{E0} (μm)
InGaAs/InP Type-I DHBT	5	0.5, 0.7, 1.5
	7	0.7
	10	0.5, 0.7, 1, 1.5
GaAsSb/InP Type-II DHBT	3.5	0.2
	5	0.2, 0.3
	7.5	0.2, 0.3

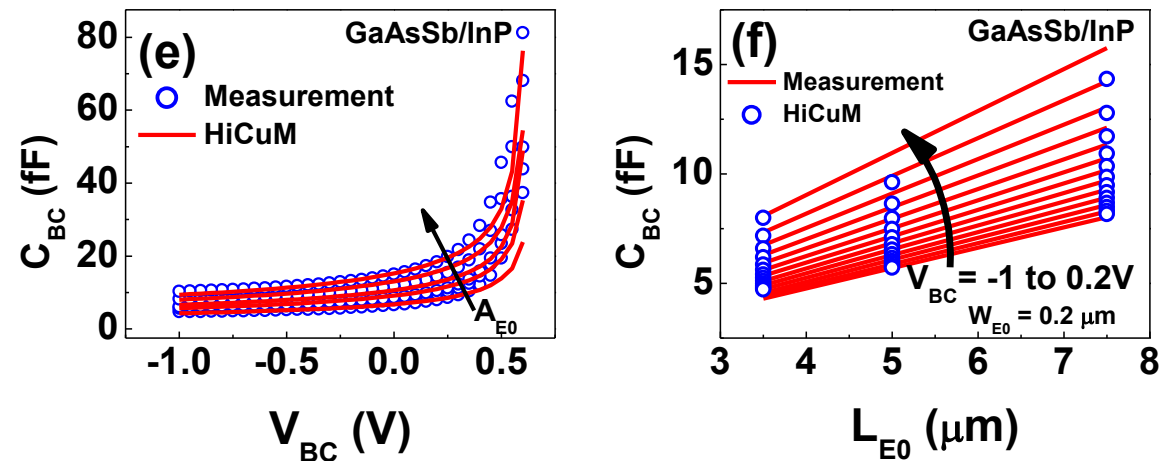
- Parameters related to **low-injection** conditions are first extracted
- Junction capacitance extraction from Cold S-parameter measurements (junction bias $< 0.5\text{V}$)
- De-embedded Y-parameters for C_{BE} extraction
- Intrinsic and peripheral contributions



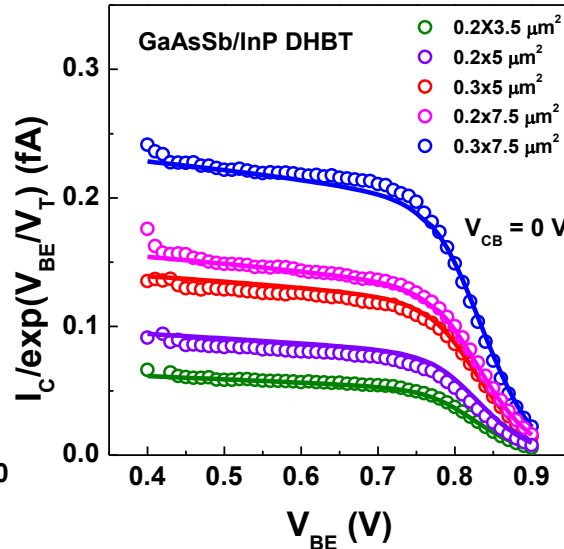
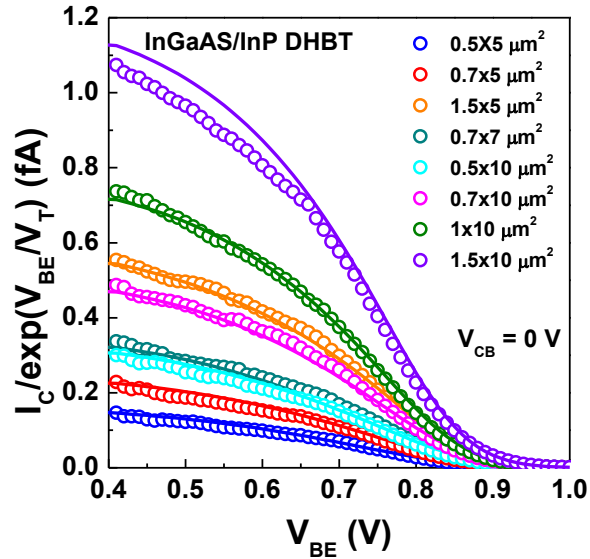
Parameter Extraction: C_{BC}



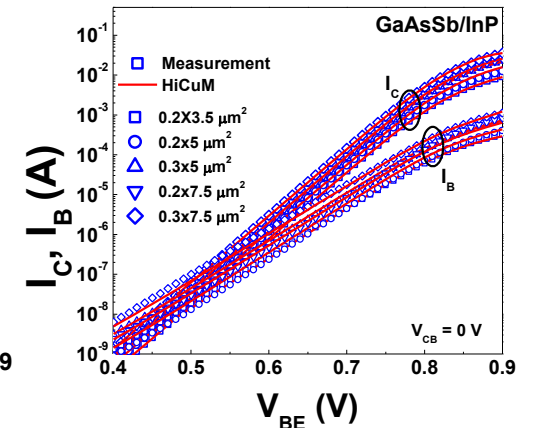
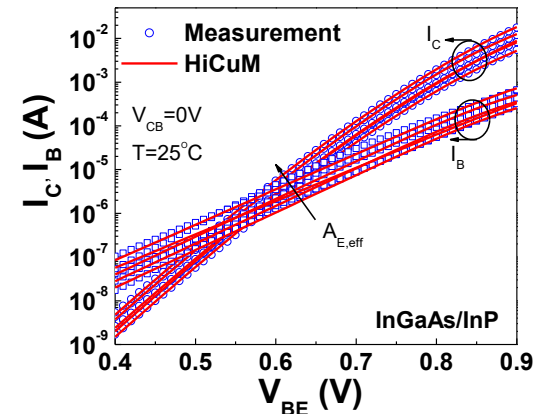
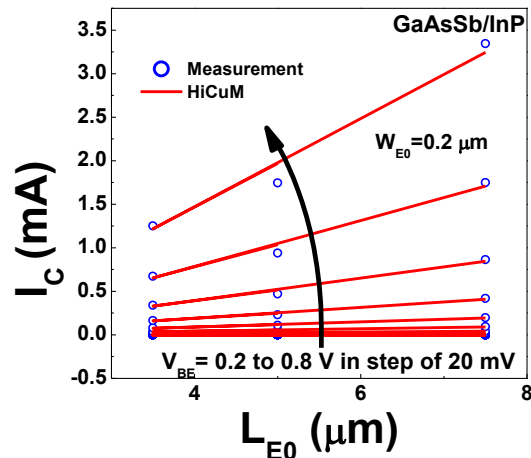
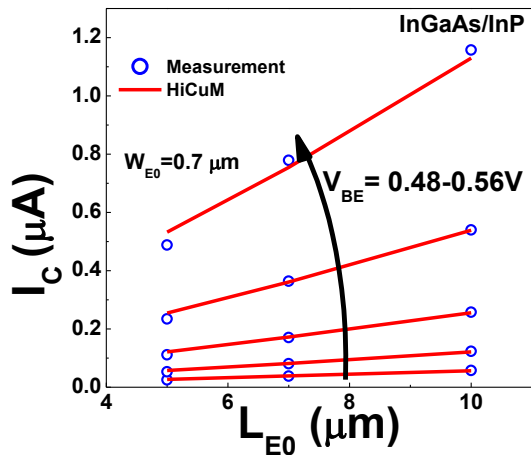
- Cold-S parameter measurements and de-embedding for $V_{BE}=0$ and a V_{CB} sweep
- Separation of intrinsic and peripheral contributions (e.g. fixing W_E and varying L_E)
- Two DHBT technologies under study



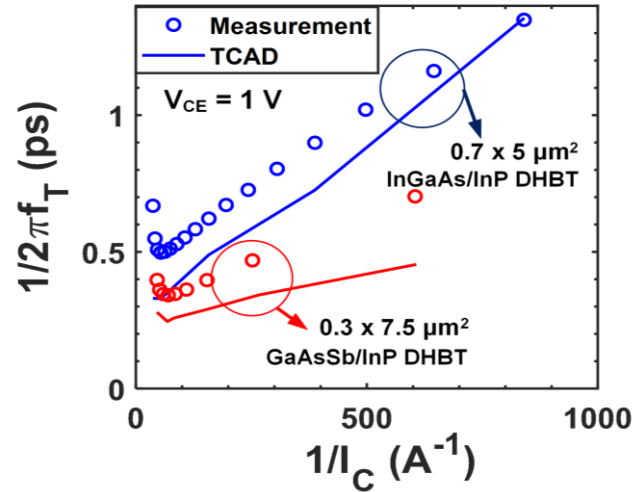
Parameter Extraction: I_C , Gummel



- Scalable extraction of the collector current at low/medium injection at $V_{BC} = 0$ V (effect of B-C junction is minimized)
- Scaling: $I_C = I_{CA} A_{E0} + I_{CP} P_{E0}$



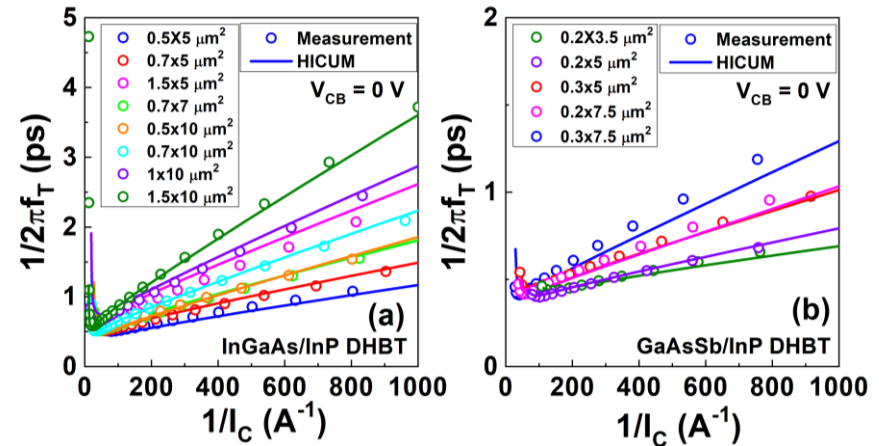
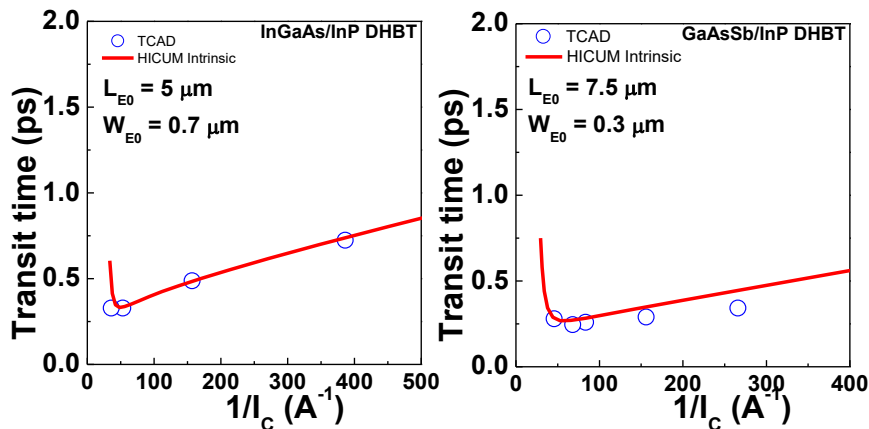
Parameter Extraction: τ_f



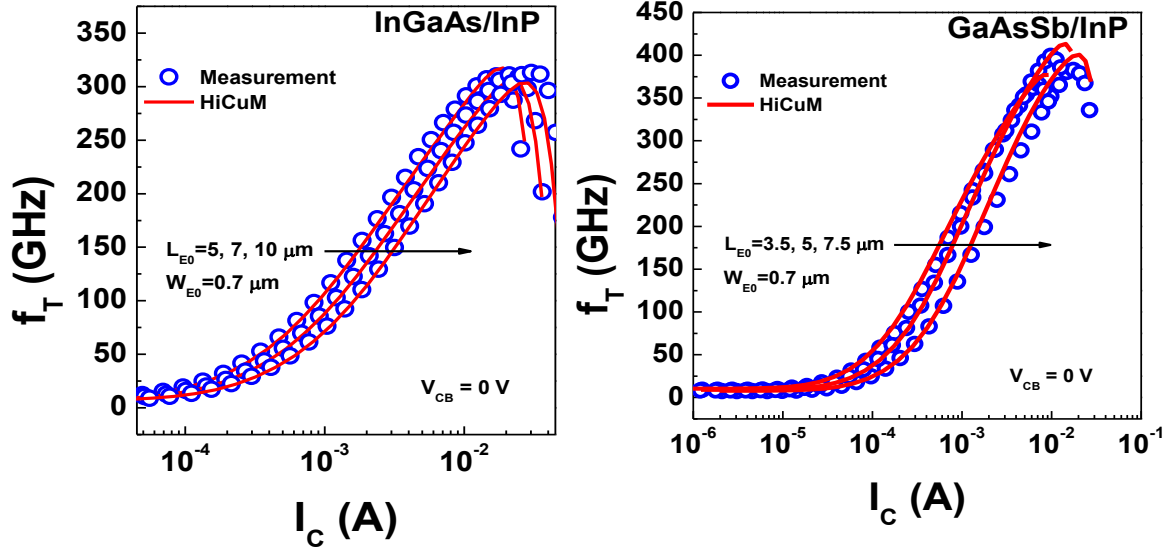
- Transit time at $V_{BC}=0V$ using the extracted low-injection parameters

$$\tau_f = \frac{1}{2\pi f_T} - \frac{C_{BE} + C_{BC}}{g_m} - (R_{Cx} + R_E)C_{JC}$$

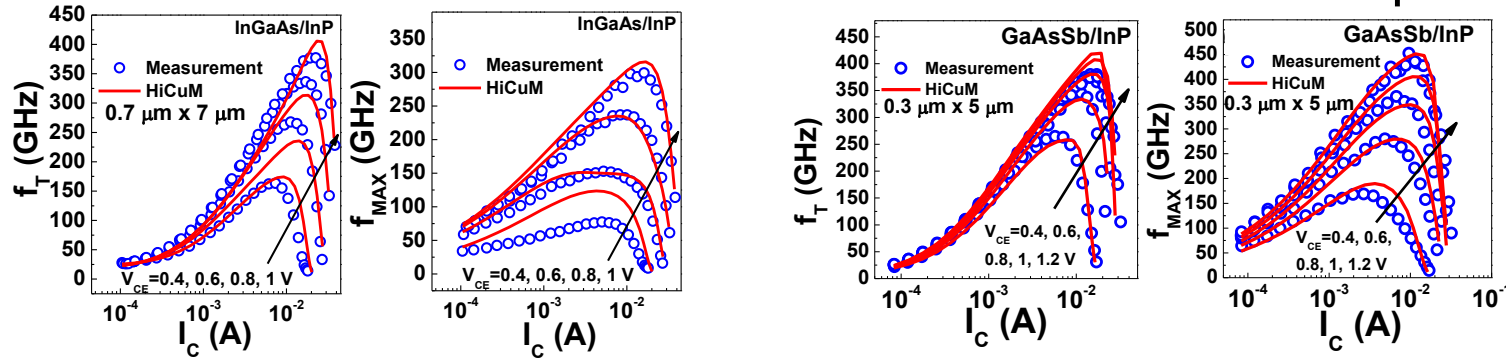
- Comparison with TCAD, discrepancies arise due to extrinsic contribution (R_{Cx} , R_E)



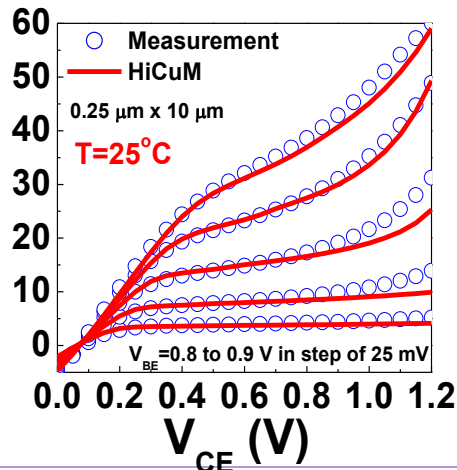
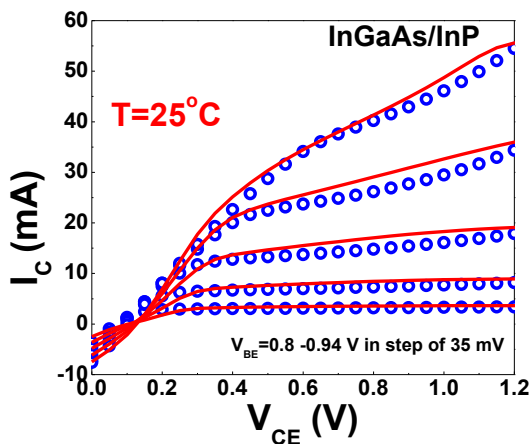
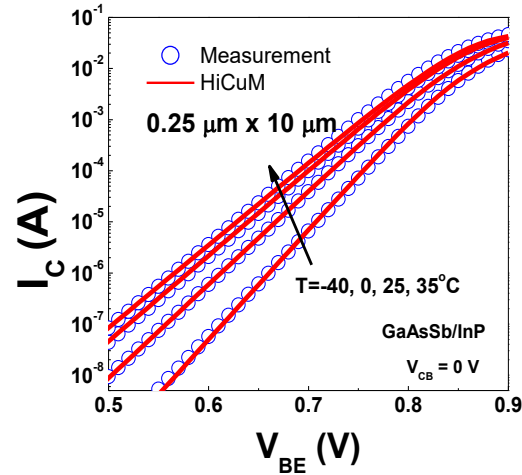
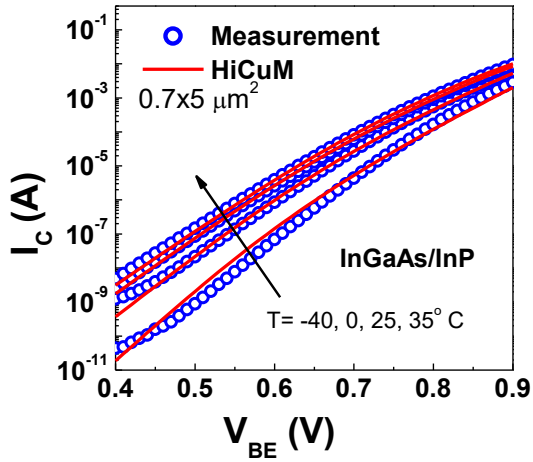
Parameter Extraction: f_T , f_{MAX}



- f_T and f_{MAX} are optimized at low/medium current first through model parameter extraction including the zero bias transit time, B-C junction capacitance, base-width modulation, carrier velocity in B-C SCR
- At high current densities, the excess transit time is modeled through high-current parameters



T-dependence, High current parameters



- Temperature dependence of model parameters (T-exponent 'ZETA')

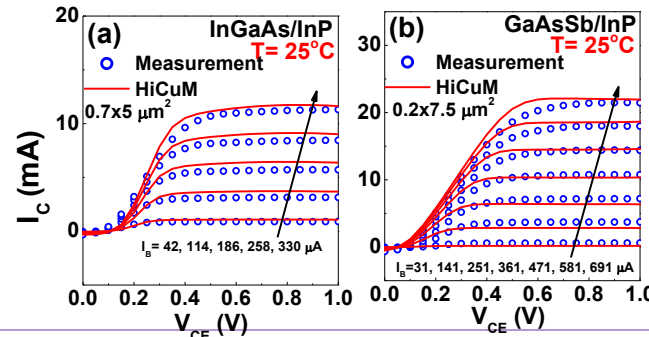
$$c_{10}(T) = c_{10}(T_0) \left(\frac{T}{T_0} \right)^{ZETA_{CT}} \exp \left[\frac{V_{GB}}{V_T} \left(\frac{T}{T_0} - 1 \right) \right]$$

$$Q_{p0}(T) = Q_{p0}(T_0) \left[2 - \left(\frac{V_{DEi}(T)}{V_{DEi}(T_0)} \right)^{Z_{Ei}} \right] \quad I_{BEIS}(T) = I_{BEIS}(T_0) \left(\frac{T}{T_0} \right)^{ZETA_{BET}} \exp \left[\frac{V_{GE}}{V_T} \left(\frac{T}{T_0} - 1 \right) \right]$$

- Thermal resistance extraction

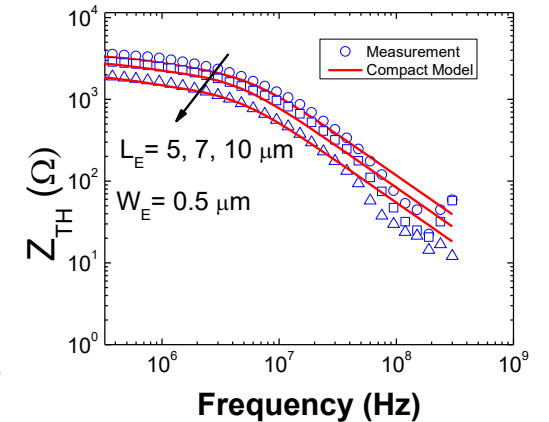
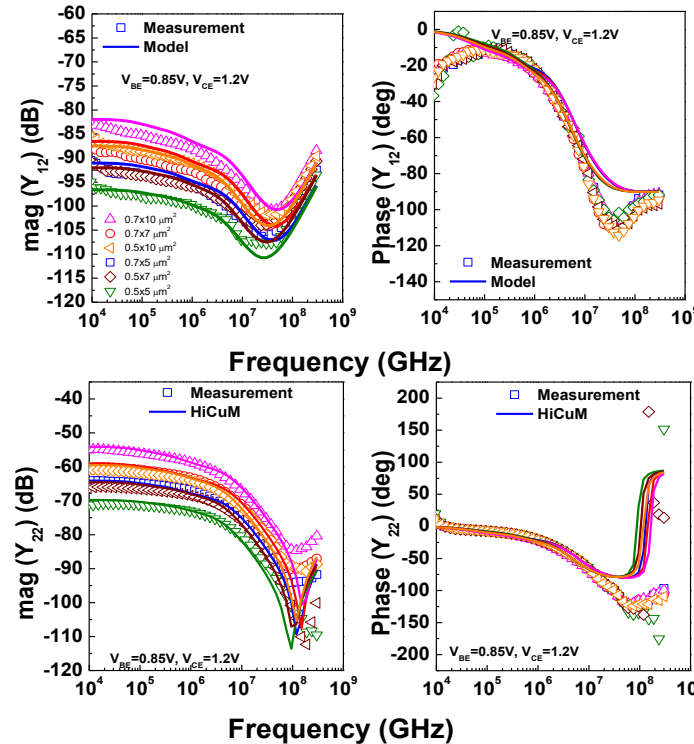
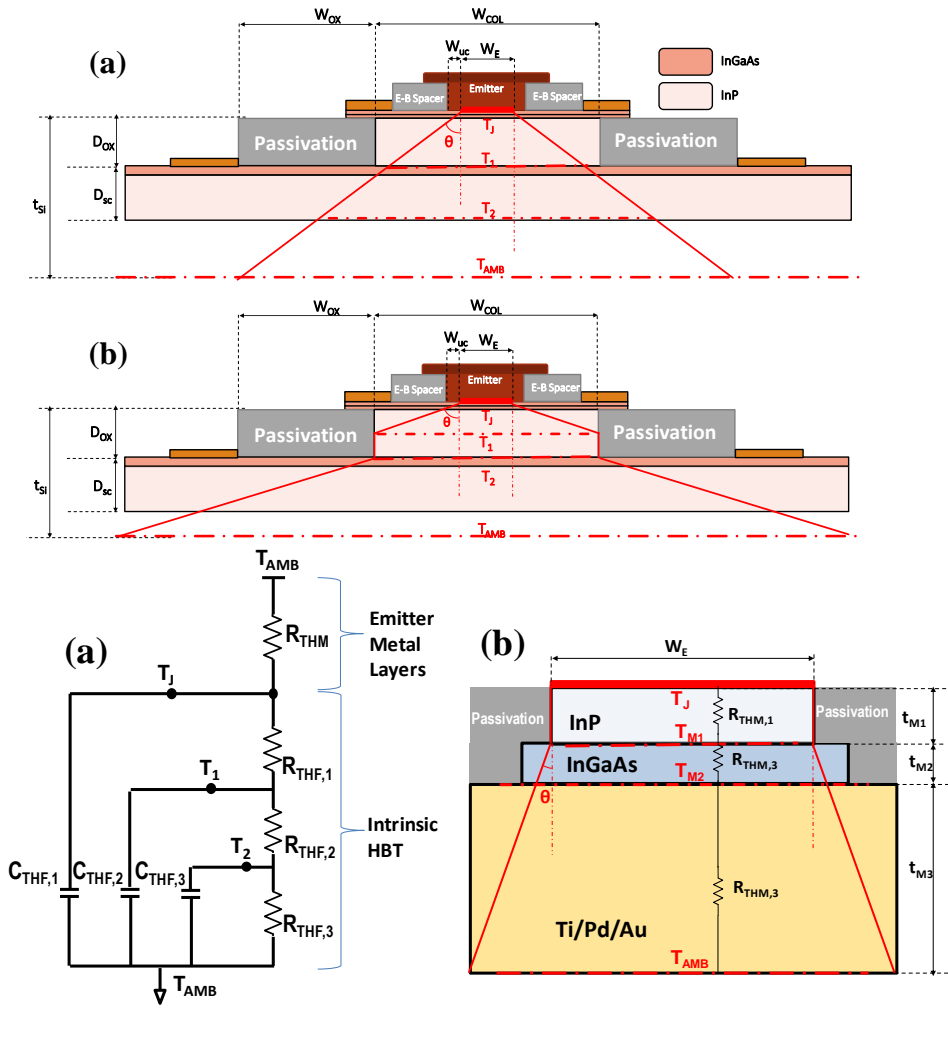
$$R_{TH}(T_{DEV}) = R_{TH}(T_{NOM}) \exp \left[ZETA_{ARTH} \left(\frac{T_{DEV}}{T_{NOM}} \right) \right] (1 + ALR_{TH} (T_{DEV} - T_{NOM}))$$

Intersection method: $R_{TH} = (T_1 - T_2) / (V_{CE2} I_{C2} - V_{CE1} I_{C1})$



Parameter Extraction: Z_{TH}

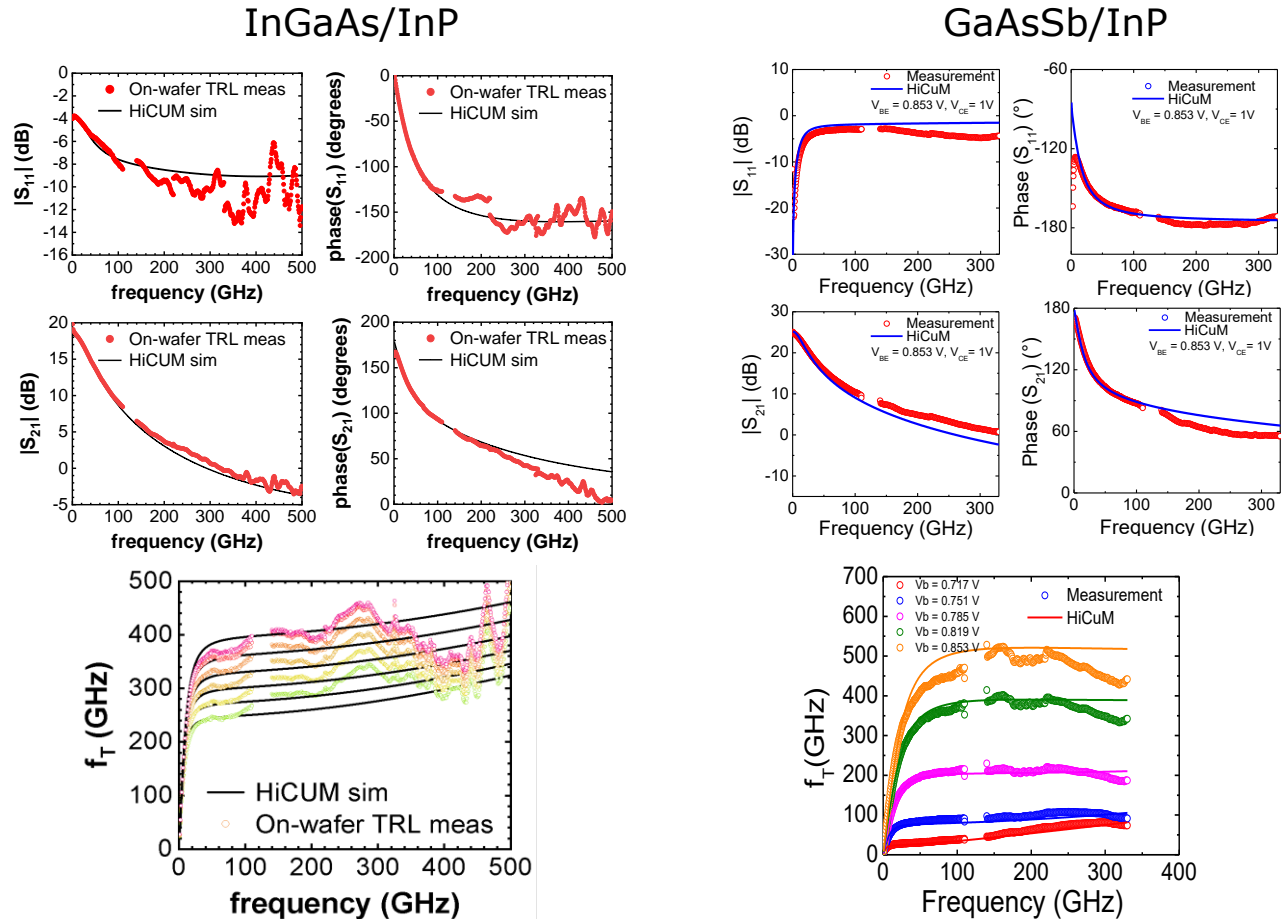
- Preliminary extraction of R_{TH} using intersection method
- Low-frequency S-parameters for Z_{TH} extraction
- Scalable model for Z_{TH} integrated with HiCuM



*C. Mukherjee et al. "Scalable Modeling of Thermal Impedance in III-V DHBTs targeting Terahertz Applications," IEEE Trans Electron Dev. vol. 66, no. 5, pp. 2125-2131, May 2019.

C. Mukherjee et al. "Towards Monolithic Indium Phosphide (InP)-Based Electronic Photonic Technologies for beyond 5G Communication Systems," Applied Sciences, vol. 11, no. 5, p. 2393, Mar. 2021

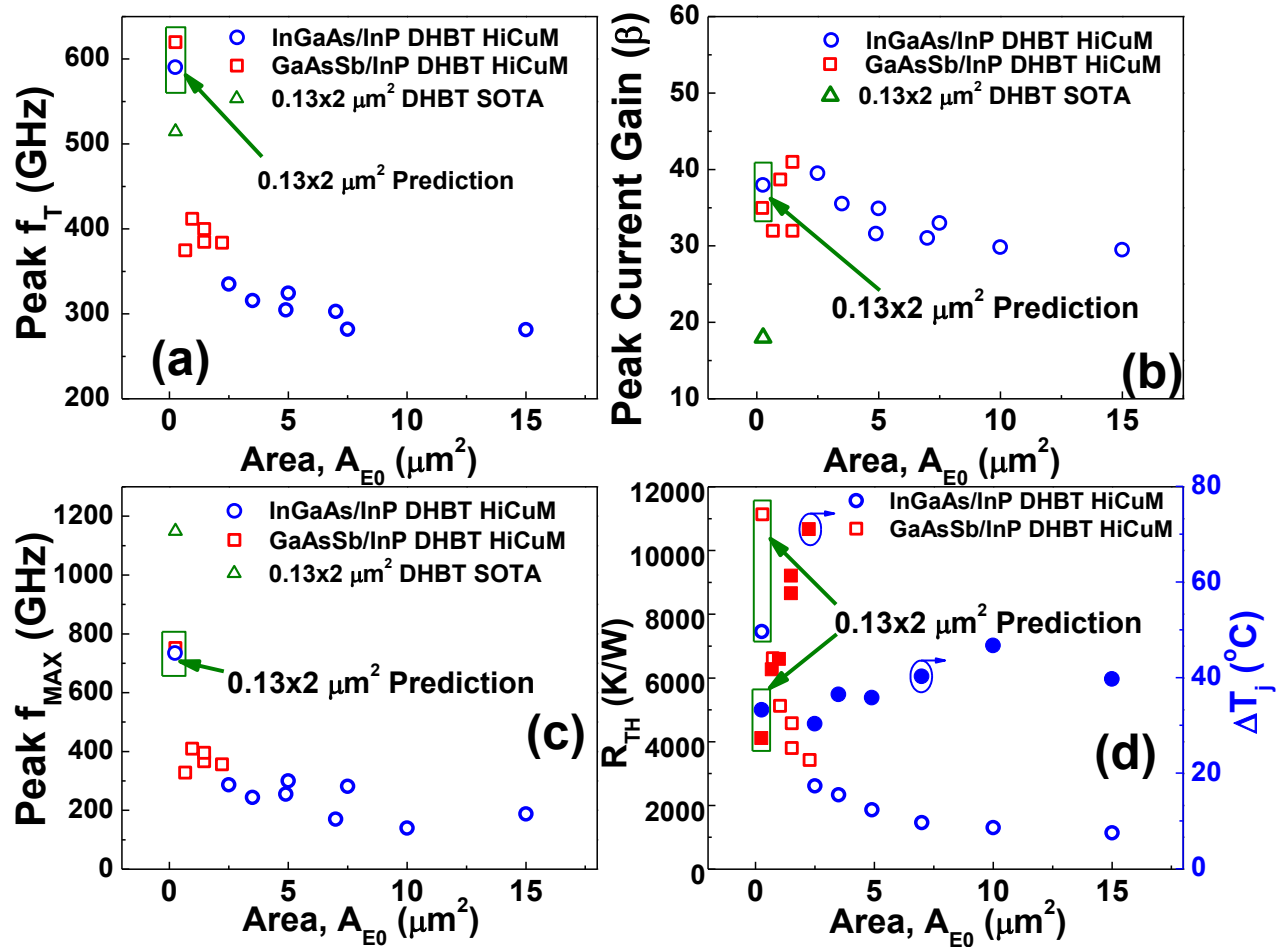
High Frequency Characterization



- Extrapolation of Scalable model card to beyond 110 GHz on-wafer TRL S-parameters for both technologies
- Transistors are biased at peak f_T conditions
- Good-band continuity and model accuracy up to 500 GHz
- Further steps: EM simulation

*M. Deng et al. "Design of On-Wafer TRL Calibration Kit for InP Technologies Characterization up to 500 GHz," *IEEE Trans Electron Dev.* 2020 doi: 10.1109/TED.2020.3033834
M. Deng et al. "InP DHBT characterization up to 500 GHz and compact model validation towards THz circuit design," *BCICTS 2021 (Submitted)*

Performance Figures of merit



- Figures of merit of III-V DHBT: (a) f_T , (b) β , (c) f_{MAX} and (d) R_{TH} , ΔT_j
- Predictive results suggests improvements over the state-of-the-art (higher f_T , lower f_{MAX} , balanced f_T/f_{MAX}) in scaled geometry
- Reliability issue prediction: quite high R_{TH} ; compensated by stable junction temperature
- Further: scaling through process optimization