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# Impact of Hot Carrier Degradation on the Performances of Current Mirrors based on a 55 nm BiCMOS Integrated Circuit Technology

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**Abstract**— This paper presents reliability assessment of basic integrated circuits designed for analog and RF applications based on extensive circuit simulations using the aging compact model, HiCuM-AL v3.0, dedicated to SiGe HBTs. The physic-based aging compact model implemented within HiCuM model is based on trap generation-annihilation mechanisms as well as the Fick hydrogen diffusion law. The model has been validated against results from HBT aging tests under various stress conditions followed by aging model parameter extraction. Due to its extensive use in integrated circuit blocks, different current mirror configurations subjected to mixed-mode stress conditions are studied and analyzed in order to quantify the impact of HC degradation on individual HBTs as well as on overall circuit performances.

**Keywords**—SiGe HBT, Compact model, aging laws, circuit aging, current mirrors.

## I. INTRODUCTION

The continuous miniaturization of electronic devices, such as SiGe heterojunction bipolar transistors (HBTs) [1], has led to a significant reduction in their safe-operating-areas (SOA), thus compelling the designers to limit circuit output power in terms of collector-emitter breakdown voltage ( $BV_{CEO}$ ) values. As a consequence, modern transistors these days operate close to the SOA edges where impact ionization is unavoidable leading to hot-carrier degradation (HCD). A complete characterization and modeling of this failure mechanism and its impact on the device as well as on the circuit reliability is recommended following the methodology proposed in [2]. Accurate, physics-based and scalable modeling of the degradation phenomena is required for predictive circuit aging simulation [3]. With that in mind, our previous works [4-5] have developed a physics-based scaled formulation for HCD in SiGe HBTs and implemented within the HiCuM compact model [6]. In this work, the latest version of this model, HiCuM AL V3.0 has been used for model parameter extraction on a 55nm BiCMOS technology from STMicroelectronics [7] that has been widely characterized from a reliability point of view in [5], [7-8]. Model scalability has been validated against aging test results from a wide range of devices under various stress conditions. The calibrated model is then further used for investigating simple, cascode, Wilson and balanced Wilson configurations of a current mirror circuit under mixed mode operating conditions. Overall circuit degradations have been studied for the different configurations and critical transistor elements most prone to failure are identified in order to assess circuit robustness. The rest of this paper is organized as follows: section II details the aging compact model formulation and device level model validation, section III describes the four current mirror configurations and their individual features, section IV presents the circuit aging simulation results under mixed-mode stress and performance comparison between the configurations, followed by the conclusions.

## II. PHYSICS-BASED AGING COMPACT MODEL

### A. Analytical model formulation

The rate of bond dissociation is governed by a chemical interaction between the carriers and the passivated Si-H bond through generation and annihilation of traps. The interface-trap density,  $N_T(t)$ , increases with the net rate of reaction and the bond dissociation rate can be calculated following reaction-diffusion theory [9] as follows,

$$\frac{dN_T}{dt} = K_F(N_F - N_T(t)) - K_R N_T(t) N_H(0, t) \quad (1)$$

$K_F$  is the rate constant of the forward reaction, *i.e.*, generation of traps,  $K_R$  is the rate constant of trap annihilation by hydrogen atoms,  $N_H(x, t)$  is the volumetric density of hydrogen at distance  $x$  of the Si/SiO<sub>2</sub> interface and  $N_F$  is the total number of available bonds that can break.

An extraction procedure for  $K_F$ ,  $K_R$  and  $N_F$  has been detailed in [5]. Moreover, an expression of  $K_F$  has been formulated as a function of the avalanche current density,  $J_{AVL}$  and stress voltage,  $V_{CB}$  as

$$K_F = g_{rate} J_{AVL} \exp(\mu F V_{CBi}) \quad (2)$$

where  $g_{rate}$  is the fraction of the avalanche current density and  $\mu F$  is an exponential factor which governs the acceleration of hot-carriers due to the electric field. On the other hand, the factors governing trap annealing depend on the number of hydrogen atoms available at the vicinity of the interface as well as on trap annihilation rate  $K_R$ , which is generally governed by an Arrhenius law as expressed by [5],

$$K_R = K_{R0} \exp\left(-\frac{E_a R}{k T_j}\right) \quad (3)$$

where  $T_j$  is the device junction temperature.

### B. Compact model for H-Diffusion Network

In addition to (1) that describes trap generation and creation of H-atoms through Si-H bond dissociation, the H-diffusion dynamics needs to be accurately described in order to estimate the number of hydrogen atoms remaining at the Si/SiO<sub>2</sub> interface. Free hydrogen atoms diffuse away from the EB spacer oxide interface and are primarily stored within the spacer oxide [5]. Depending on the diffusion coefficient,  $D_H$ , of the material, hydrogen atoms could diffuse further beyond the spacer, through the emitter poly-Si. To consider all possible diffusion scenarios based on Fick's law of diffusion [10], an N-stage RC ladder network has been adopted in [4-5] which is terminated by a conductance G that represents the long-term diffusion scenario in poly-Si (Fig. 1).

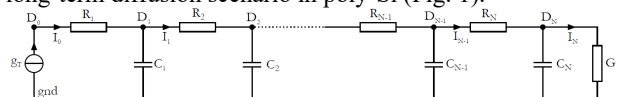


Fig. 1: RC ladder network for hydrogen diffusion modeling.

For all practical purposes, we have considered  $N=3$  for the current technology where individual cell elements are represented by the recursive formulation,

$$C_n = C_H \frac{\alpha_C^{n-1} - \alpha_C^n}{1 - \alpha_C^n}, R_n = R_H \frac{\alpha_R^{n-1} - \alpha_R^n}{1 - \alpha_R^n} \quad (4)$$

where  $C_H$  represents the storage capacity of hydrogen atoms and  $R_H$  represents the barrier to normal lattice diffusion [5],  $\alpha_C$  and  $\alpha_R$  are the recursive factors for the capacitances and the resistances, respectively.

### C. Scalable formulations

From a compact model point of view [6], the trap creation at the Si/SiO<sub>2</sub> interface can be represented by the change in a specific base current parameter, the peripheral B-E recombination saturation current,  $I_{REpS}$  [4, 7, 11]. As it has been made evident in earlier works [5] that the region around the emitter periphery is solely impacted by HCD, the effect of degradation on the internal base-emitter current parameters can be neglected. In [5], we used TCAD simulations along with HiCuM compact model simulations to correlate the increase of  $I_{REpS}$  with that of the trap density at the spacer interface (Fig. 2(a)) for a given geometry through the following equation,

$$I_{REpS}(t) = \alpha P_E N_T(t) \quad (5)$$

Note that the model formulation has been thoroughly made scalable through scaling laws of the degradation mechanism [5, 7] as well as using  $J_{REpS}$  which is  $I_{REpS}$  normalized with the dimensions of emitter perimeter,  $P_E$ . Moreover, the interface area,  $A_{SPACER}$ , largely depends on the emitter perimeter which is consistent with the location of the region where the degradation takes place (Fig. 2(b)).

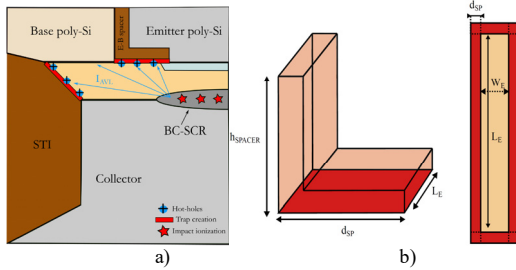


Fig. 2: (a) Schematic device cross-section showing the physical location of HCD, (b) side and top views of emitter-base spacer of the 55 nm technology.

Additionally, from the definition of  $C_H$ , a scalable formulation can be obtained in terms of the H-diffusion volume ( $V_{DIFF}$ ) and the interface trap generation surface ( $A_{SPACER}$ ). In turn,  $R_H$  is represented in terms of  $C_H$  and  $D_H$  ( $=D_0 \exp(-E_a/kT)$ ), the diffusion constant of hydrogen in a given material,

$$C_H = \frac{V_{DIFF}}{A_{SPACER}}, R_H = \frac{C_H}{D_H} \quad (6)$$

### D. Model Validation on 55 nm BiCMOS Technology

The aging compact model (HiCuM AL V3.0) has been validated for various stress conditions over a wide range of HBT geometries. The comparison between the measurements (symbols) and the simulations (lines) is depicted in figure 3 for two chosen stress conditions. Very good model accuracy can be observed across different operating conditions and geometries validating the scaled formulation of the compact model. Table I summarizes the essential extracted aging model parameters.

TABLE I: AGING PARAMETERS FOR 0.55 NM BICMOS TECHNOLOGY

Parameter	$\alpha$ (A)	$D_0$ ( $\mu\text{m}^2/\text{s}$ )	$E_a$ (eV)	$\mu F$ ( $\text{V}^{-1}$ )	$g_{rate}$ ( $\mu\text{m}^2\text{A}^{-1}\text{s}^{-1}$ )	$K_{R0}$ ( $\mu\text{m}^3/\text{s}$ )	$E_{aR}$ (eV)
Values	$1.25 \times 10^{-19}$	0.464	0.48	2	0.84	2.05	0.56

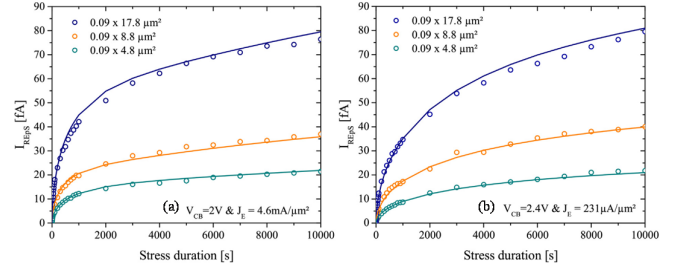


Fig. 3: HiCuM-AL V3.0 simulations (lines) vs measurement (symbols) for various device geometries under two mixed mode stress conditions.

## III. CURRENT MIRROR CONFIGURATIONS

One of the most basic building block used in analog and RF circuits is the current mirror employed as a biasing element or an active load for amplifier stages [12]. The structure commonly provides an output current,  $I_{OUT}$ , proportional to a reference input current,  $I_{IN}$ . The basic figure of merit describing the operation of a current mirror is the transfer current ratio described by  $\eta = I_{OUT}/I_{IN}$ .

This study is based on four simulated current mirror configurations: simple, cascode, Wilson and balanced Wilson, depicted in Fig. 4. Each transistor, T1, T2, T3 and T4, features the same emitter dimensions of  $0.2 \times 5.56 \mu\text{m}^2$ .

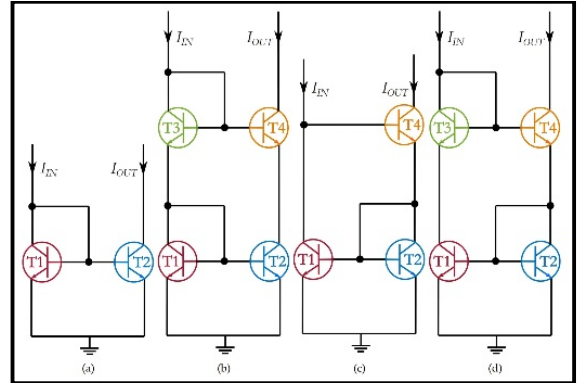


Fig. 4: Schematic of (a) the simple, (b) the cascode, (c) the Wilson and (d) the balanced Wilson current mirrors.

### A. Simple current mirror

The simplest form of a current mirror consists of two transistors as presented in fig. 4(a). The transistor T<sub>1</sub> is diode connected implying that the base-collector junction is off. Both transistors are assumed to operate in the forward-active region with infinite output resistances. The current gain error for this configuration is only due to the base current of transistors T<sub>1</sub> and T<sub>2</sub>, which, thereby, causes a variation of the output current compared to the input current.

### B. Cascode current mirror

The cascode current mirror presented in fig. 4 (b) features a very high output resistance. This current mirror architecture is based on a stack of two simple current mirrors (T<sub>1</sub> being associated with T<sub>2</sub> and T<sub>3</sub> being associated with T<sub>4</sub>). To improve matching, emitter resistances can be added at the bottom of the structure.

### C. Wilson current mirror

The Wilson current mirror presented in fig. 4 (c) overcomes some limitations of the cascode current mirror. Indeed, this circuit uses a negative feedback through  $T_2$  device which reduces the base current of  $T_1$ . Consequently, the current gain error arising from a finite  $\beta$  is reduced compared to the cascode architecture. However, a mismatch between  $T_1$  and  $T_2$  collector-emitter voltages appears which increases the gain error between the input current and the output current.

### D. Balanced Wilson current mirror

The balanced Wilson current mirror presented in fig. 4 (d) is an improved version of the Wilson structure. In the case of balanced Wilson current mirror, the use of the symmetrical cascode transistors balances out the collector-emitter voltages of  $T_1$  and  $T_2$  removing any mismatch between  $T_1$  and  $T_2$  arising from Early effect in  $T_1$  transistor. Also, the current gain is no longer dependent on the imbalance between the two voltages which largely extends the linear operating range of the circuit.

## IV. CIRCUIT RELIABILITY ANALYSIS

The electrical performances of each current mirror architecture are evaluated under standard operating conditions (*i.e.* without the activation of the aging compact model) based on the study proposed in [13] for MOS based current mirrors. The reliability analysis of each current mirror configuration is performed for a maximum stress duration of 1000 h using a transient simulation time of 10  $\mu$ s ( $ATSF = 3.6 \times 10^{11}$ ) [4, 5]. The aging compact model, HiCuM-AL V3.0, is activated for each transistor by settling the aging flag model parameter to 1. Two particular criteria are chosen to assess the robustness of the current mirrors: the  $I_{REPS}$  parameter which is the only aging compact model parameter sensitive to hot-carrier degradation and  $dI_{OUT}$  which illustrates the output current variation compared to its initial value (at  $t=0$ s).

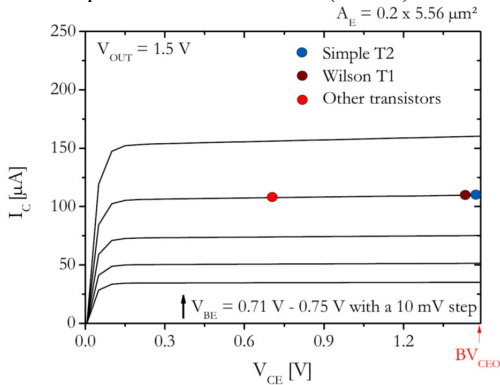


Fig. 5:  $I_C$  vs  $V_{CE}$  characteristics highlighting the operating conditions for each current mirror configuration at  $V_{OUT} = 1.5$  V and  $I_{IN} = 100$   $\mu$ A.

### A. Standard operating condition

First, the reliability of each configuration is evaluated under standard operating conditions with  $I_{IN} = 100$   $\mu$ A and  $V_{OUT} = 1.5$  V. The corresponding transistor operating conditions for each current mirror configuration is reported in Fig. 5. From this plot, it can be observed that only two transistors operate close to the edges of the safe-operating-area: T2 from the simple current mirror source and T1 from the Wilson one. Consequently, the weak avalanche mechanism is activated for both transistors due to their operations close to  $BV_{CEO}$ . For the same operating condition, the evolution of  $I_{REPS}$  parameter of each transistor for each current mirror configuration is presented in Fig. 6 as a function of the stress duration. In

accordance with the theory, no increase of the recombination current can be observed for diode mounted transistors since the impact-ionization mechanism has not been activated. An increase of  $I_{REPS}$  up to 1 fA can be highlighted for the transistor  $T_2$  of the simple current mirror. In fact, due to its operation close to  $BV_{CEO}$  (see Fig. 5), the impact-ionization mechanism is activated for this transistor, resulting in a negative base current. On the contrary, for the Wilson current mirror, an increase of  $I_{REPS}$  up to 0.9 fA leads to a positive shift of the output current due to a positive base current for this operating condition.

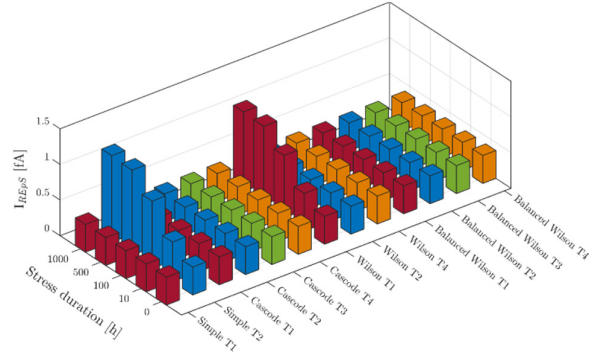


Fig. 6: Evolution of  $I_{REPS}$  with stress duration for different transistors and current mirror configurations at  $I_{IN} = 100$   $\mu$ A and  $V_{OUT} = 1.5$  V.

### B. Mixed-mode operating condition

To assess the robustness of the current mirror configurations, the output voltage is set to 3 V while the input current is kept constant at a value of 100  $\mu$ A. The corresponding transistor operating conditions for each current mirror configuration is reported in Fig. 7. It can be observed that the transistor T2 from the simple current mirror operates under strong avalanche conditions, with an equivalent  $V_{CB}$  of 2.25 V. Moreover, the output transistor ( $T_4$ ) of the cascode, Wilson and balanced Wilson also exhibits a large  $V_{CB}$  of 1.5 V and a  $V_{CE}$  of 2.25 V, well beyond the conventional  $BV_{CEO}$ . This particular operating condition for the current mirror configurations likely leads to mixed-mode operation induced degradation due to the activation of the impact-ionization mechanism for several transistors.

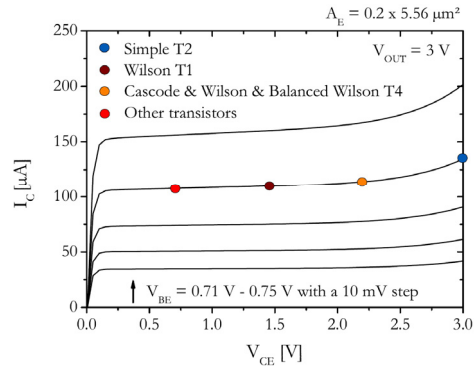


Fig. 7:  $I_C$  vs  $V_{CE}$  characteristics highlighting the operating conditions for each current mirror configuration at  $V_{OUT} = 3$  V and  $I_{IN} = 100$   $\mu$ A.

For each operating condition, the evolution of  $I_{REPS}$  is presented in Fig. 8, as a function of the stress duration under the same operating condition. It can be observed that only four transistors suffer from hot-carrier degradation: the transistor  $T_2$  of the simple current mirror and the transistors  $T_4$  of the three other configurations. This result is consistent with the applied bias conditions (Fig. 7). Due to their large  $V_{CB}$  values,



all the transistors operate under avalanche conditions resulting in a negative base current. In the case of the simple current mirror, the  $I_{REPs}$  parameter reaches a value of 30 fA which, in turn, increases the base current. However, even if the transistor is significantly impacted by HCD under mixed-mode stress, circuit electronic functions are not influenced by HCD, as the transfer current ratio does not evolve over the stress duration (Fig. 9). For the three other configurations, cascode, Wilson and balanced Wilson, the increase of  $I_{REPs}$  is limited to 10 fA for the T4 transistors due to a reduced  $V_{CB}$  value. Once more, the large degradation of the base current induced by hot-carrier degradation does not impact the electronic functionality of the current mirror.

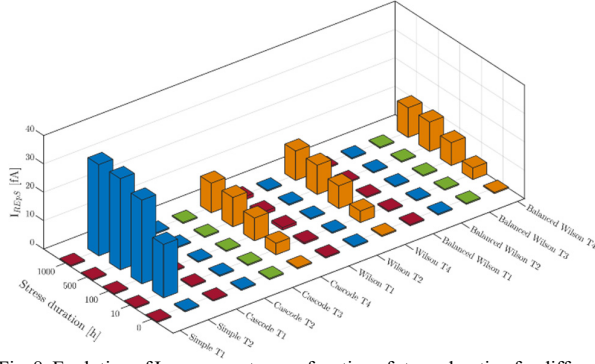


Fig. 8: Evolution of  $I_{REPs}$  parameter as a function of stress duration for different transistors of the current mirror configurations at  $I_{IN} = 100 \mu A$ ,  $V_{OUT} = 3 V$ .

From these results, it can be concluded that the activation of hot-carrier degradation does have an impact at transistor level depending on their operating conditions but the degradation has a rather weak effect on the transfer current ratio of the current mirrors since its variation is less than 1%.

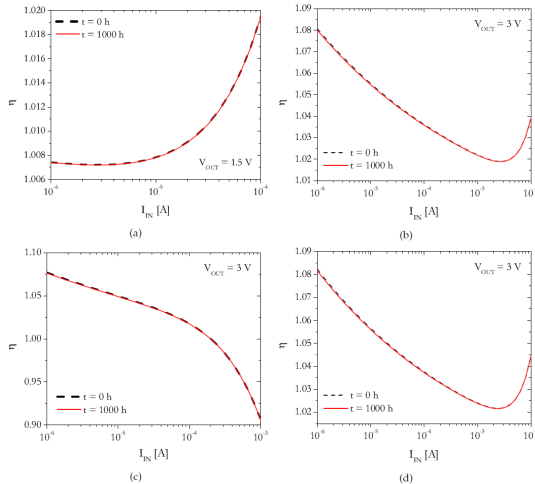


Fig. 9: Transfer current ratio evolution with the input current at  $t = 0 h$  and  $t = 1000 h$  for the (a) simple, (b) cascode, (c) Wilson and (d) balanced Wilson current mirrors.

### C. Analysis according to Injection levels

Fig. 9 presents the evolution of the transfer current ratio according to the input current at  $V_{OUT} = 1.5 V$  for the simple current mirror, Fig. 9(a) and at  $V_{OUT} = 3 V$  for the three other configurations, Figs. 9(b), 9(c) and 9(d). Conforming to its architecture, a limited output voltage of 1.5 V for the simple current mirror is chosen to ensure an equivalent operating condition for each transistor. From the simulation results, a maximum degradation of 0.001 for the transfer current ratio at

relatively low injection levels (between  $1 \mu A$  to  $100 \mu A$ ) can be observed while no variation is visible beyond these. These outcomes are consistent with the results presented in [14] where a larger degradation of the transfer current ratio was exhibited at low current densities. Nevertheless, despite the increase of the recombination current, the induced degradation is minimal and does not affect the circuit function. This is mainly due to the fact that the current mirrors are usually designed to be independent of the transistor current gain.

## V. CONCLUSION

In this paper we have demonstrated a scalable physics-based aging compact model for circuit simulation to study the performances of different configurations of current mirror circuits based on an industrial 55nm SiGe BiCMOS technology. Circuit aging simulation show that the four current mirror configurations exhibit very good robustness with a maximum variation of less than 1% for the transfer current ratio even after 1000 h of stress regardless of the operating condition within the stable operation regime. The relative degradations of different transistors in the different circuits are compared to identify the elements are more prone to degradation. The demonstrated approach is indispensable for advanced integrated circuit design optimization, leveraging a reliability-aware design flow, especially for significantly improving IC design time and costs.

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