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InP DHBT characterization up to 500 GHz and compact model validation towards THz circuit design

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Abstract—We report on-wafer characterization results up to 500 GHz on a $0.4 \times 5 \mu\text{m}^2$ InP/InGaAs DHBT. The measurements were performed using an on-wafer Thru-Reflect-Line (TRL) calibration kit especially developed in this technology. The resulting measurements allowed to validate both the RF performance of the $0.4\text{-}\mu\text{m}$ InP/InGaAs DHBT fabricated by III-V Lab, featuring 390/600 GHz f_t/f_{max} , and the HiCuM compact model towards future circuit design at submillimeter-wave frequencies thanks to 90% typical yield reached in this technology.

Keywords— Indium-Phosphide (InP), InP/InGaAs, Double heterojunction bipolar transistor (DHBT), on-wafer characterization, millimeter-wave, sub-millimeter-wave

I. INTRODUCTION

Nowadays, the multiplication of communication services, such as remote work, e-learning, e-healthcare and intensification of social relations supported by massive data transmission, pushes to develop the whole value chain from component to circuit, including the compact modeling of components, in order to increase transmission network capacities with Tb/s/channel objective [1].

The Indium Phosphide (InP) double heterojunction bipolar transistor (DHBT) has become a promising candidate for terahertz (THz) integrated circuit design, by combining both maximum oscillation frequencies (f_{max}) above 0.8 THz and common-emitter breakdown voltage above 4.2 V [2]-[5].

Nevertheless, to ensure such high RF potential, the accurate RF characterization of these THz transistors is crucial to confirm the high cut-off frequencies as well as to precisely extract and validate the device compact model, thus enabling millimeter and sub-millimeter-wave IC design. On-wafer measurements are particularly difficult beyond 110 GHz, as discussed in [6] and [7], since unwanted parasitic effects become predominant, which are not totally removed by calibration and de-embedding techniques, and may mask the intrinsic behavior of the nanoscale device. Above 110 GHz, two strategies may be adopted and combined in order to perform accurate on-wafer device measurements at submillimeter-wave frequencies: i) optimizing the test structures' design in order to minimize the unwanted parasitics, ii) developing on-wafer calibration standards on the same substrate as the device to characterize. In this paper, we demonstrate that these strategies proved their efficiency for the characterization and compact modelling of an InP DHBT up to 500 GHz.

II. SUB-MILLIMETER WAVE CHARACTERIZATION STRATEGY

A. Technology Overview

The transistor vertical structure was grown by IntelliEPI on a $3''$ semi-insulated InP substrate using Solid Source Molecular Beam Epitaxy. It includes a 40-nm InP emitter and a 28-nm highly C-doped. The highly doped level of this layer ($\sim 8 \times 10^{19} \text{cm}^{-3}$) leads to a low sheet resistance of $750 \Omega/\square$. The 130-nm thick collector is composed of a non-intentionally doped spacer, 20-nm thick highly doped InP region and a low doped InP layer ($< 2.10^{16} \text{cm}^{-3}$) to obtain a high breakdown voltage. An In-rich and highly doped InGaAs cap emitter layer is used in order to minimize the emitter contact resistivity ($< 3 \Omega \cdot \mu\text{m}^2$).

The transistors were fabricated using a wet-etch triple mesa technology including a self-aligned base-emitter metallization process similar to the one described in [5]. The emitter contact has a rectangular shape and a width of 0.4- or 0.5- μm . In comparison with previous transistor design [8], the base contact (W_B) is reduced from 0.3- to 0.2- μm for some devices in order to minimize the base-collector capacitance. The transistor size is much more compact thanks the reduction of the distance between the base mesa and the collector contact as well as the minimization of the collector contact width. This allows to reduce parasitic elements such as collector access resistance, base-collector capacitance and emitter-collector capacitance. Figure 1 shows a scanning electron microphotograph of a $0.4\text{-}\mu\text{m}$ emitter width DHBT before interconnection level, presenting an innovative rectangular emitter shape compared to conventional previous one. The typical fabrication yield of the $0.4\text{-}\mu\text{m}$ InP DHBT is above 90%.

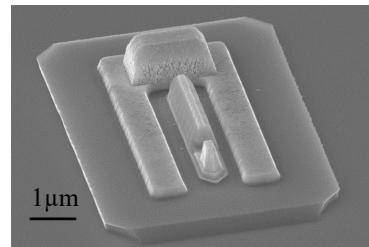


Fig. 1. SEM of $0.4 \times 4\text{-}\mu\text{m}^2$ InP DHBT before interconnection level

B. On-wafer Calibration Kit Design

The on-wafer calibration kit was designed so as to apply the Thru-Reflect-Line (TRL) method, well known to be efficient for accurate S-parameter measurements beyond 110 GHz on both

silicon and InP heterojunction transistors characterization [9]-[13]. Well-known for its robustness and traceability, the TRL method, based on only three standards, is also easy to implement, since two transmission line, one Thru and one Line, need to be designed, as well as a symmetrical Reflect, either open or short-type. The only known parameters are the delays of the Thru and Line standards. In the III-V Lab InP process, 50 ohm coplanar waveguide (CPW) transmission lines were used for Thru and Lines standards, and one Pad-Open standard as the Reflect. As depicted in Fig. 2, the TRL calibration standards were located in the periphery of the chip.

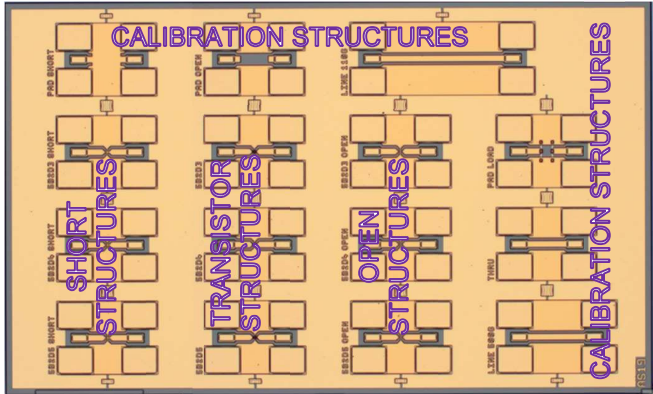


Fig. 2. Photography of the chip with all the test structures

A continuous ground plane was implemented as recommended in [12] and [13] with the support of electromagnetic simulation so as to minimize the coupling between the RF probes and the substrate. Then, all the ground pads of each test structure are connected together through this continuous ground plane.

This on-wafer TRL calibration kit was used to perform S-parameter measurements from 1 to 500 GHz using four benches: 1-110 GHz, 140-220 GHz (*G*-band), 220-330 GHz (*J*-band) and 325-500 GHz. The ground-signal-ground RF pads were designed with a 50-100 μm probing pitch in order to be compatible with the different sets of RF probes in each measurement band.

C. De-embedding Test Structures Design And Characterization results

The transistor under test presented an emitter width of 0.4 μm and an emitter length of 5 μm . This geometry was selected for its high cut-off frequencies, with a f_T/f_{max} couple of 390/600 GHz extracted at low frequencies, while maintaining a common-emitter breakdown voltage superior to 4.5 V.

The test structures associated to the transistor, as well as the dedicated open and short, are shown in Fig. 3. The CPW pads and access lines that connect the transistor are similar to the calibration structures. Consequently, the reference plane after calibration could be set along the access line as close as possible to the transistor terminals, as depicted in Fig. 3-b. The remaining interconnection parasitic effects were then removed using the short-open de-embedding.

Furthermore, the validity of the short-open de-embedding method rely on a lumped equivalent electrical circuit of the open

and the short structures (see Fig. 4). To verify the frequency independence of the Open capacitances and Short inductances, these de-embedding test structures were measured up to 500 GHz, using on-wafer TRL calibration. The resulting capacitances and inductances were extracted using respectively Y and Z parameters (see Fig. 5). The open capacitances showed a relatively constant value in the overall 1-500 GHz measurement band, with no resonance in the highest frequency range and a good band continuity. The short measurements were quite difficult to carry out, especially in *J*-band. This was due to a high sensitivity to the contact in addition to the fact that the TRL calibration was made with the Pad-Open as Reflect, reducing the calibration accuracy for short measurements [14]. However, an average constant value among the 1 to 500 GHz measurement range can be observed for the computed inductances. The validity of the Short-Open de-embedding method to apply to the transistor's measurement was then verified up to 500 GHz.

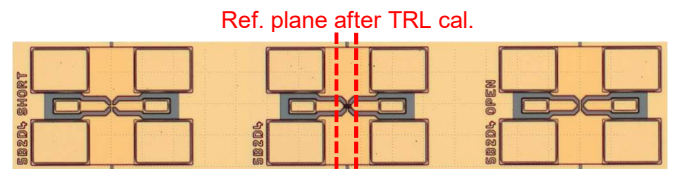


Fig. 3. Photography of the transistor (center) and its dedicated de-embedding Open (right) and Short (left) test structures

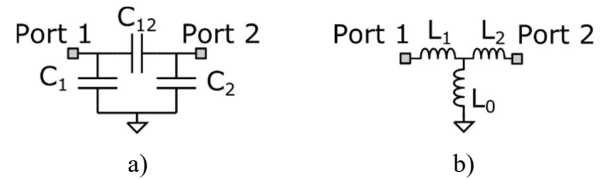


Fig. 4. Equivalent electrical circuit of the (a) Open and (b) Short de-embedding test structures

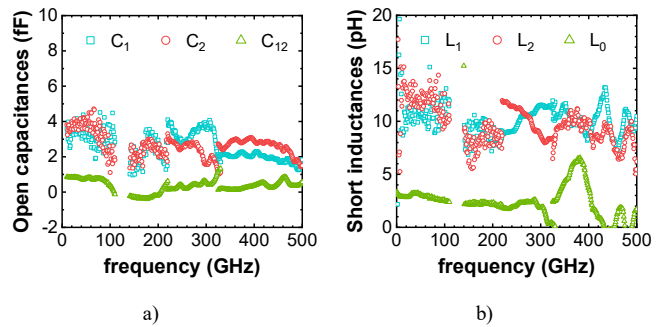


Fig. 5. Measured (a) Open capacitances and (b) Short inductances up to 500 GHz

III. RESULTS AND DISCUSSION

A. Compact Model Validation

DC characterizations and HiCuM compact model simulation were performed on several device dimensions (0.5 and 0.7 μm emitter widths and emitter lengths of 5, 7 and 10 μm). We employed a dedicated geometry scalable parameter extraction flow leveraging a macro model containing the scaling laws for

all HiCuM Level2.0 (L2) parameters related to emitter dimensions. In particular, all model parameters are split into their contributions from the intrinsic device and the periphery, as a function of the dimensions of the emitter window. The model parameter process starts with the declaration of technological parameter values such as sheet resistances, zero-bias hole charge, area and perimeter dimensions as well as given design rules and process layout information [8]. The subsequent steps are extraction of low-injection parameters (from junction capacitances, base and collector currents at low to medium bias, zero-bias transit time), and eventually parameters correlated with high-current effects (self-heating, temperature dependence and bias-dependent transit time) are extracted.

1. DC Characteristics

Fig. 6 shows the (a) Gummel and (b) output characteristics of the smallest geometry characterized depicting a comparison between the HiCuM compact model and the on-wafer DC measurements. A good model accuracy has been observed for all geometries under study, affirming the model scalability.

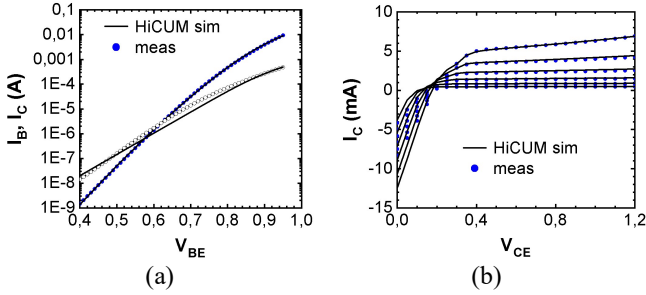


Fig. 6. I-V measurements and simulation: (a) Gummel plot; (b) Output characteristic. DUT geometry: $W_E=0.5\mu\text{m}$, $L_E=5\mu\text{m}$, $W_B=0.3\mu\text{m}$,

2. Junction Capacitance Extraction

Fig. 7 shows the extracted junction capacitances at low to medium injection in comparison with HiCuM simulation for the base-collector (Fig. 7 (a)) and base-emitter (Fig. 7(b)) junction capacitances for 3 emitter lengths ($L_E=5, 7, 10\mu\text{m}$) for an emitter width of $0.5\mu\text{m}$. Again good model scalability has been observed. The extracted model parameter set has been further exploited for validation of measurements up to 500 GHz.

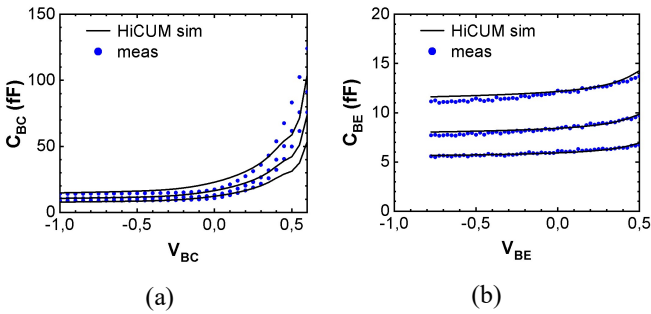


Fig. 7. Junction capacitances' measurements and simulation: (a) C_{BC} versus V_{BC} ; (b) C_{BE} versus V_{BE} . Transistor geometries: $W_E=0.5\mu\text{m}$, $L_E=5, 7, 10\mu\text{m}$, $W_B=0.3\mu\text{m}$

3. S-parameter measurement and simulation up to 500 GHz

The HiCuM compact model was simulated and compared to the InP DHBT measurements up to 500 GHz after on-wafer TRL calibration and Short-Open de-embedding. The transistor under test was biased at peak f_T/f_{max} , that is at $V_{CE}=1.6\text{V}$ and $V_{BE}=0.94\text{V}$. A pretty good agreement was obtained in the overall 1-500 GHz frequency range. The deviation from the model is particularly observed above 325 GHz up to 500 GHz for all S-parameters. In the last band, indeed the transistor shows less gain while the on-wafer measurement setup is subject to significant losses in the connectors despite the maximum applied RF power.

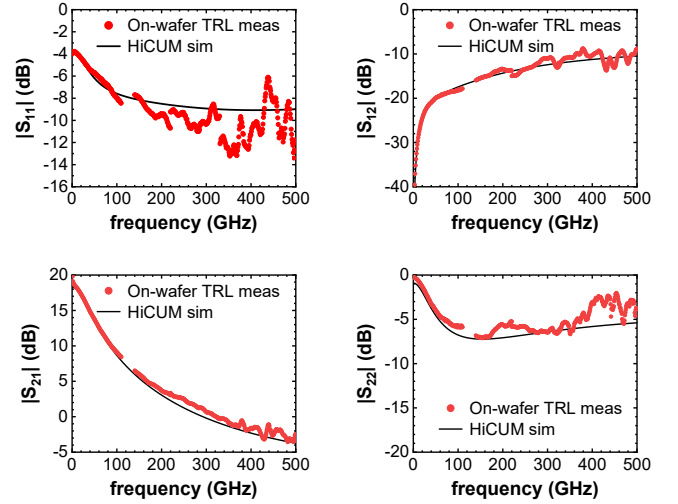


Fig. 8. InP DHBT S-parameter measurement and simulation in magnitude up to 500 GHz – Transistor geometry: $W_E=0.4\mu\text{m}$, $L_E=5\mu\text{m}$, $W_B=0.2\mu\text{m}$

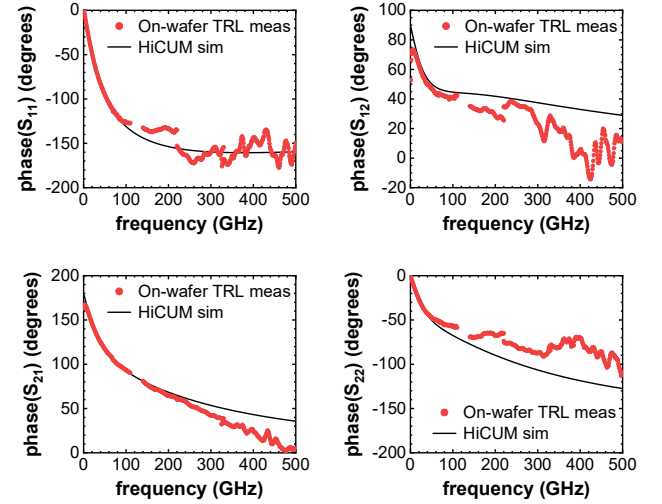


Fig. 9. InP DHBT S-parameter measurement and simulation in phase up to 500 GHz – Transistor geometry: $W_E=0.4\mu\text{m}$, $L_E=5\mu\text{m}$, $W_B=0.2\mu\text{m}$

B. RF Performance FoM extraction of InP DHBT up to 500 GHz

The HiCuM compact model was simulated again under multiple bias points and compared with the corresponding

measurements up to 500 GHz. The transistor was biased at a fixed $V_{CE}=1.6$ V and the base voltage was swept from 890 to 940 mV. The H_{21} current gain and unilateral Mason gain were computed for both measured and simulated data, as well as their gain-bandwidth product so as to extract the transit frequency, f_T , and the maximum oscillation frequency, f_{max} .

The expected 390/600 GHz f_T/f_{max} was then confirmed by the measurements up to 500 GHz for f_T and up to 400 GHz for f_{max} . This validates this InP DHBT technology as a promising candidate for THz MMIC design. Also, the satisfying agreement between the model and the measurement demonstrates the capability of the HiCuM compact model to fairly reproduce the transistor's behavior up to submillimeter-wave frequency range. Nevertheless, improvements still need to be done regarding the measurements' accuracy beyond 300 GHz, eventually by using EM simulation for a better understanding of the measurement artefacts or/and for further test structures optimization.

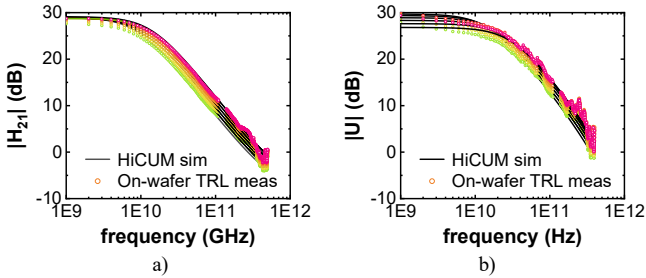


Fig. 10. InP DHBT gain curves: a) H_{21} current gain, b) Mason gain

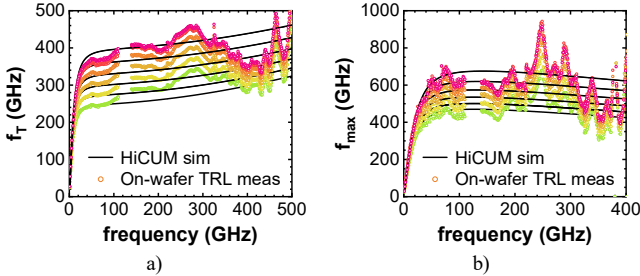


Fig. 11. InP DHBT gain-bandwidth product: a) transit frequency, b) maximum oscillation frequency f_{max}

IV. CONCLUSION AND PERSPECTIVES

In this paper, on-wafer characterization of InP DHBT was achieved up to 500 GHz, using on-wafer TRL calibration and optimized test structures layout to minimize any parasitic effects due to the interconnects to the device and coupling between RF probes and substrate which strongly impacts the measurement accuracy at millimeter and sub-millimeter-wave frequency ranges. The validity of the lumped Short-Open de-embedding method was verified up to 500 GHz. This permitted accurate and reliable transistor measurements for both validation of the InP DHBT RF performances, featuring 390/600 GHz f_T/f_{max} , and validation of the HiCuM compact model of InP DHBT up to 500 GHz, required to envisage successful first-pass THz MMIC design.

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