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# Parasitic Capacitances in transformerless power supply for DBD

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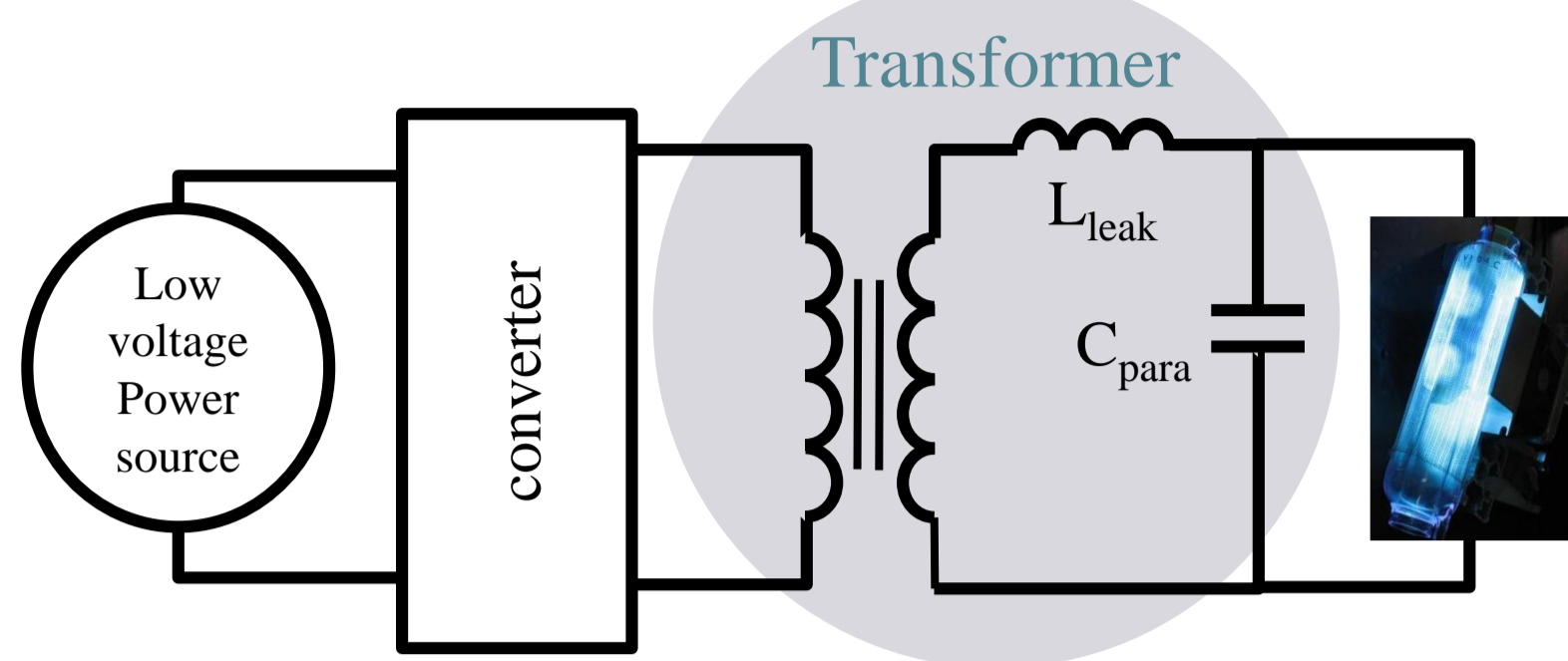
2 rue Camichel, 31071 TOULOUSE cedex 7, FRANCE.



## Context and experimental setup

### Traditional High voltage power supply for DBD :

- Voltage applied to obtain breakdown > 4 kV
- Traditional semiconductors sustain 1.7 kV max

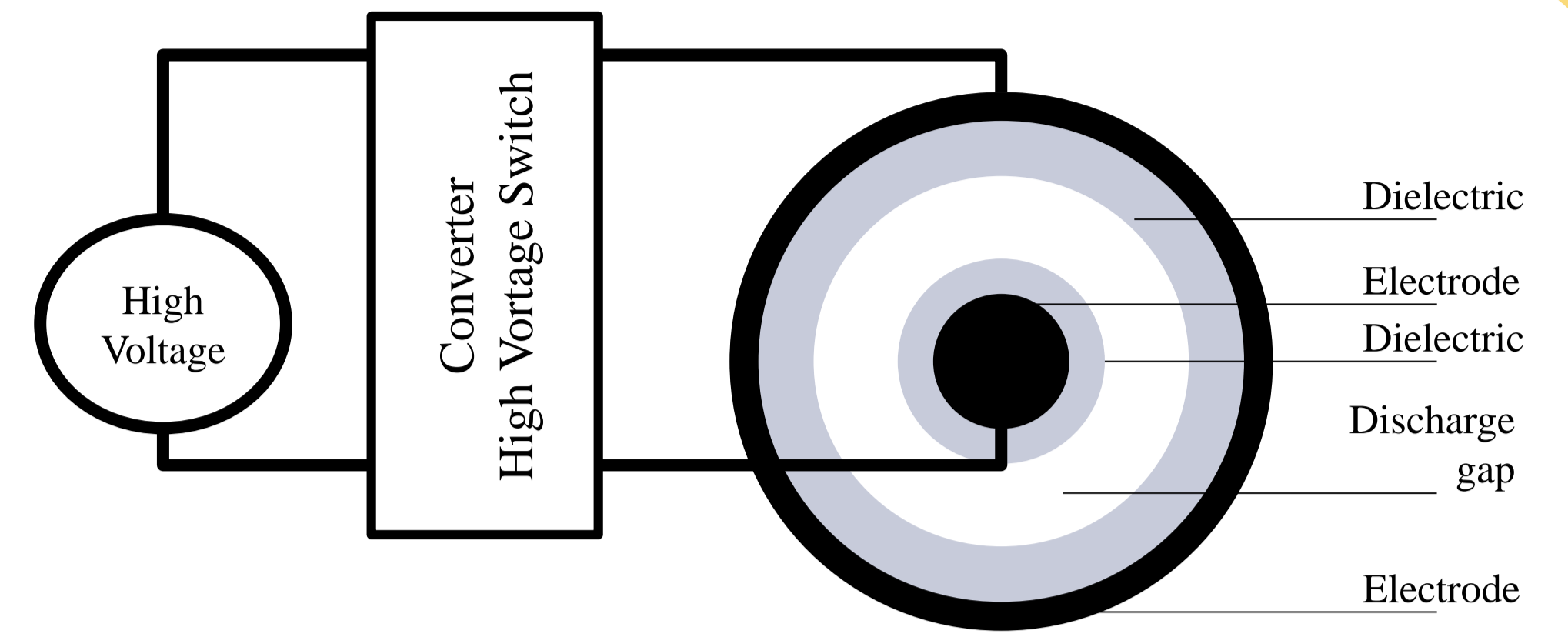
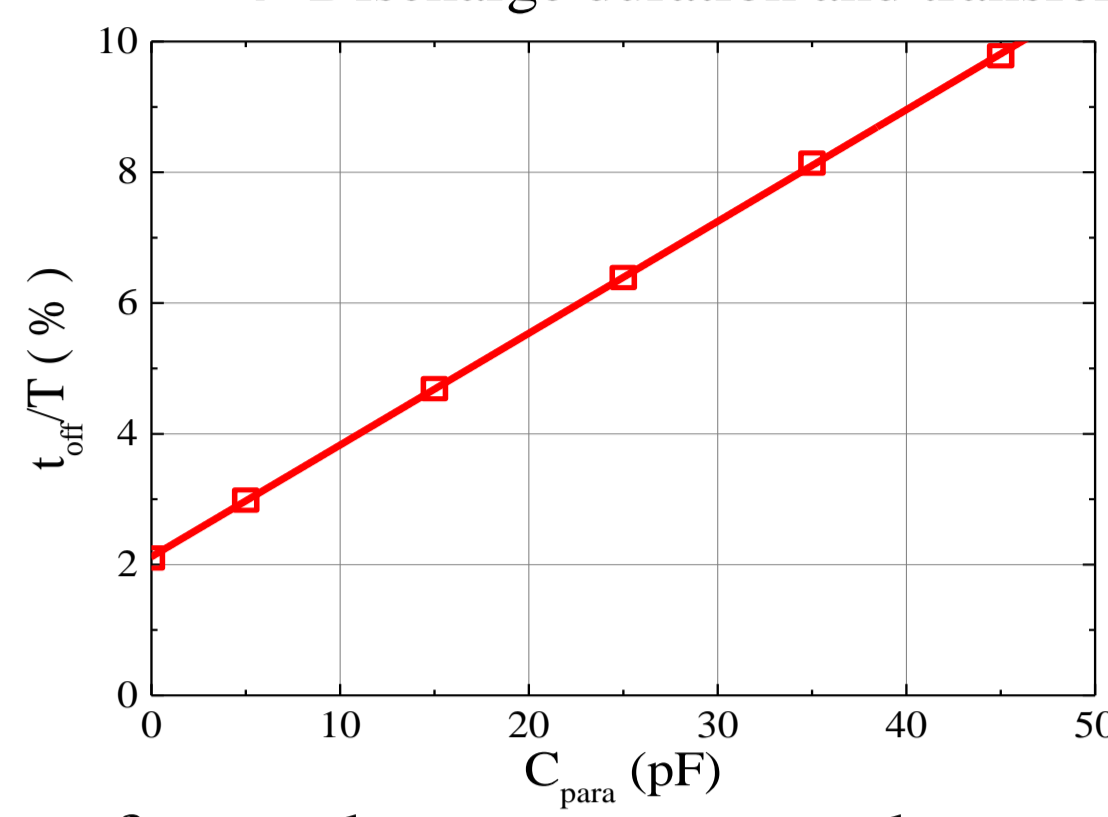


### Or resonance power supply

- No transformer
- Fixed frequency

### Transformer:

- ⊗ Amplifies the voltage → low voltage switch
  - ⊗ Parasitic elements ( $L_{leak}$  and  $C_{para}$ )
    - ⊗ Overlap of converter's switches ( $L_{leak}$ )
    - ⊗ Current leak in parallel  $C_{para}$  capacitance
- Discharge duration and transferred power ↘

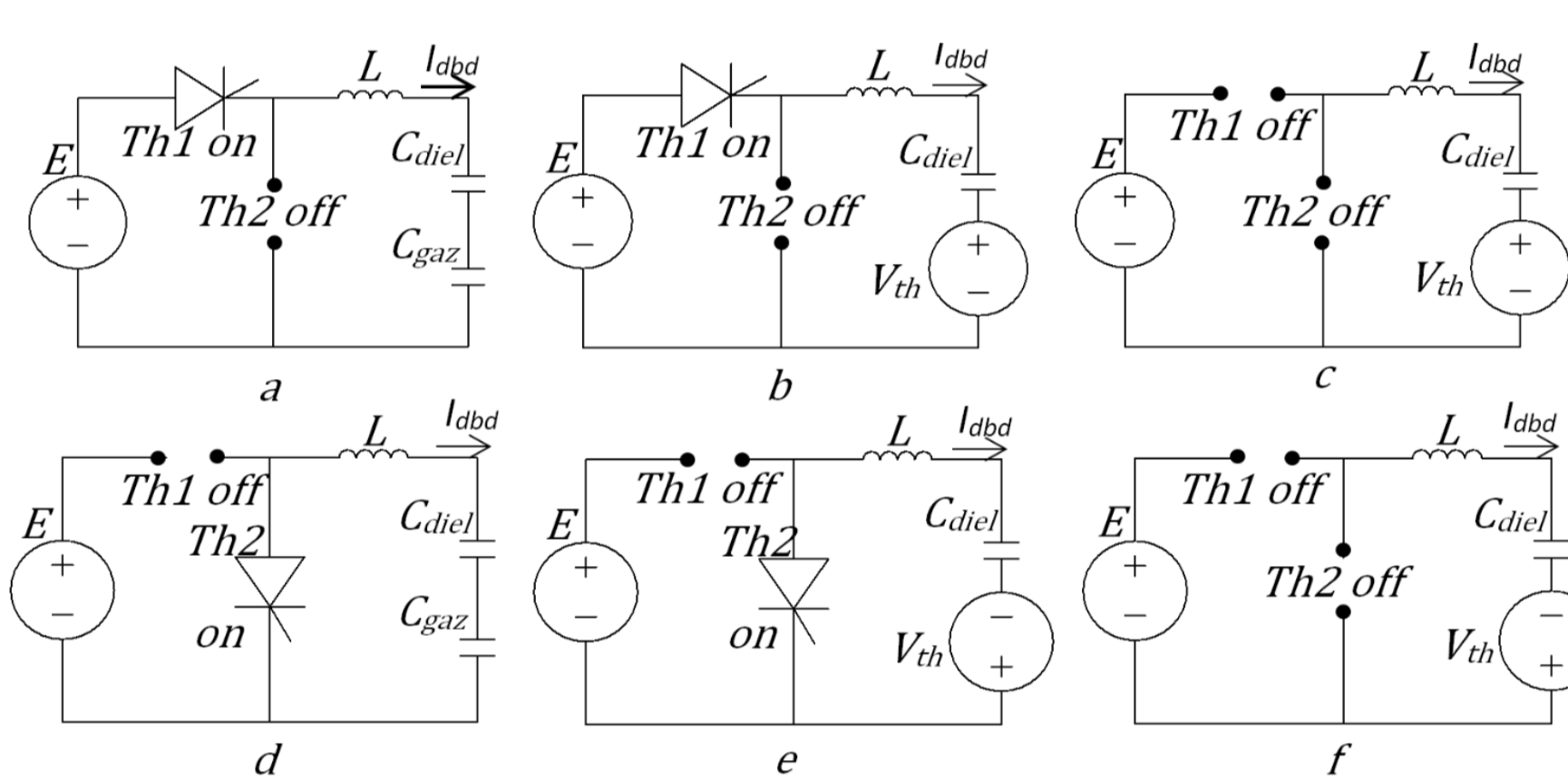
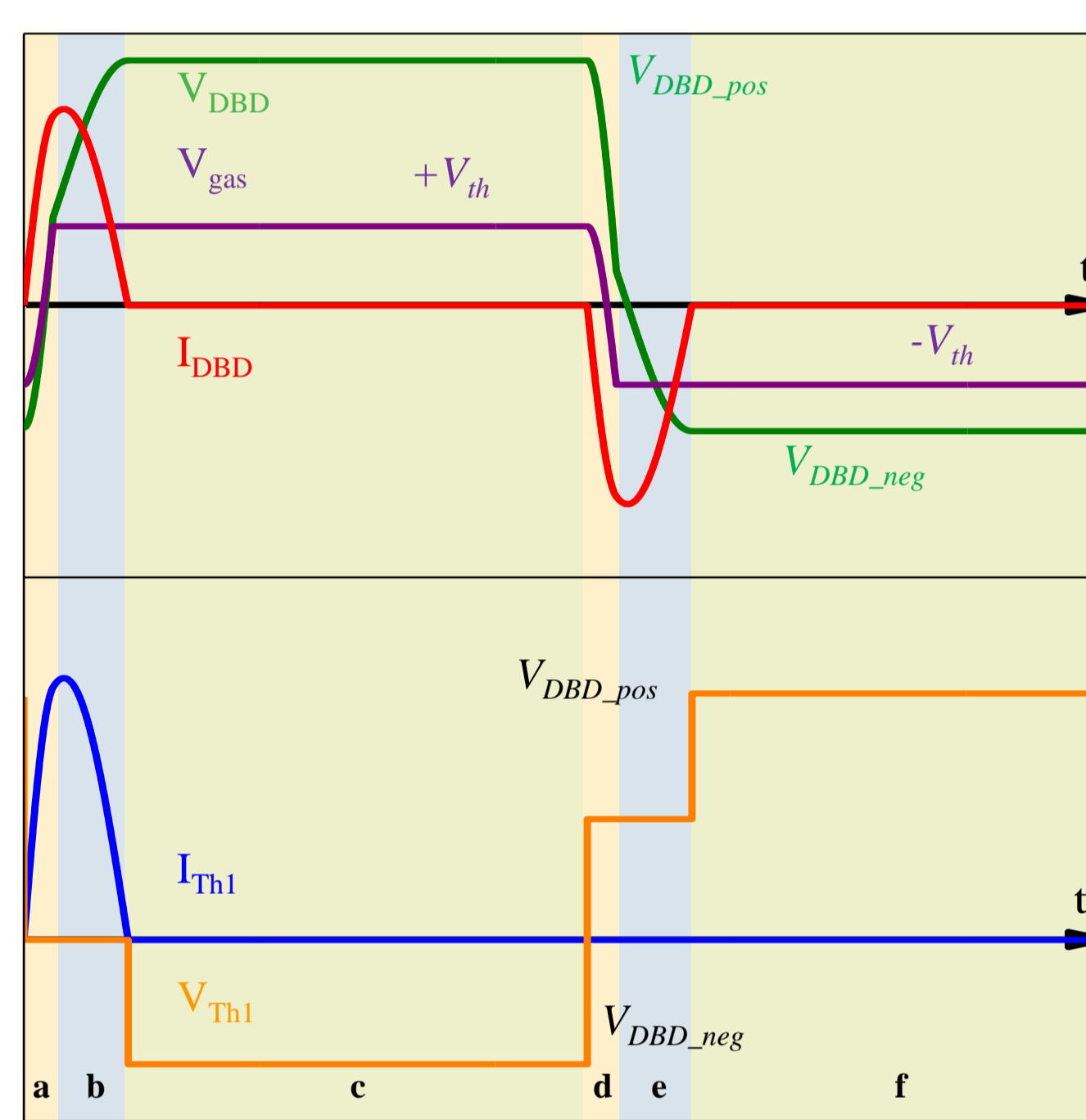
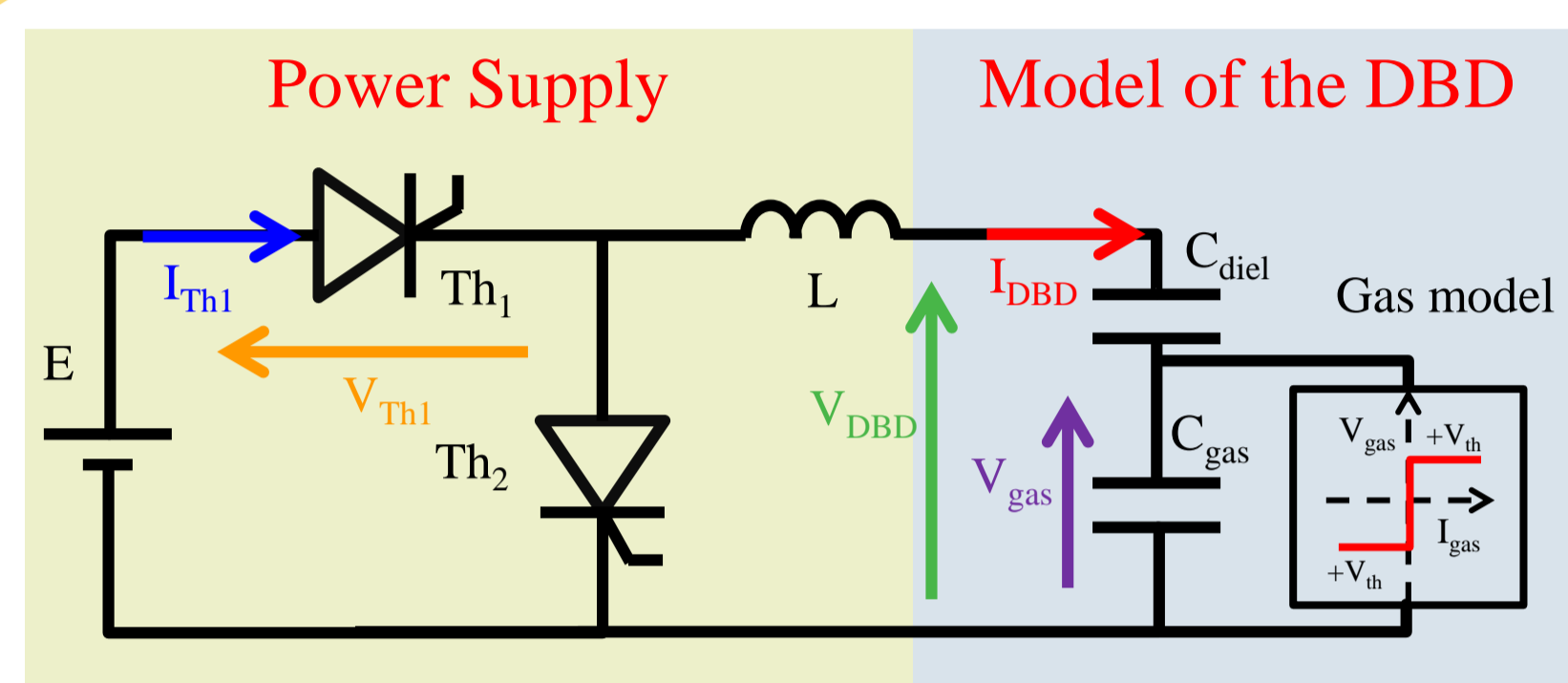


### DBD lamp:

- Length : 115 mm
- Gap : 20 mm –Xe-Cl – Pressure : 120 mBar
- $P_{nom}=100$  W
- Breakdown voltage  $\approx 1,5$  kV
- $C_{gas}=28$  pF -  $C_{diel}=85$  pF

- Transformerless power supply
- Test NEW High Voltage SIC MOSFET > 10 kV

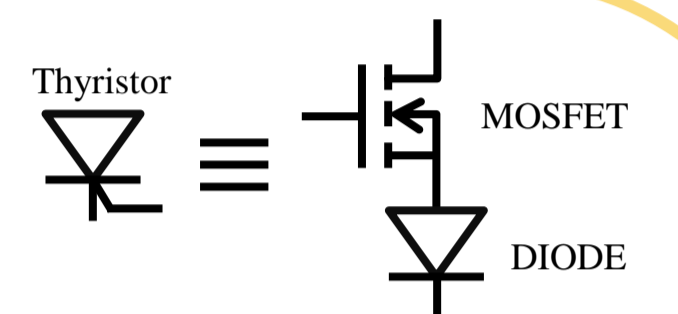
## Power supply : Operating Principle



- Use just 2 High Voltage Thyristors
- Second half period: Electrical charges stocked on the dielectric are used to re-ignite the discharge

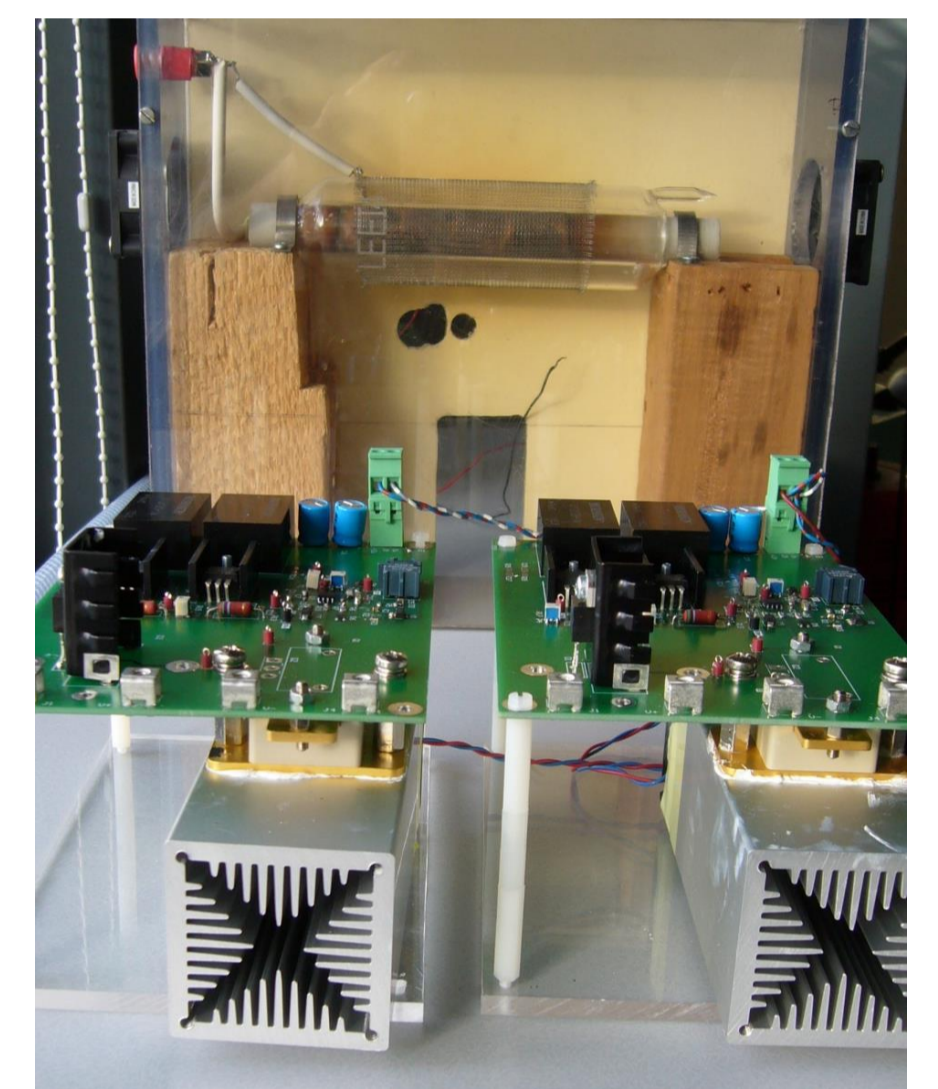
## High Voltage Switch

- Frequency up to 100 kHz
- Synthesized thyristor
- MOSFET sustains:  $V_{DBD\_pos} \approx$  several kV
- DIODE sustains:  $V_{DBD\_neg} < 1.5$  kV

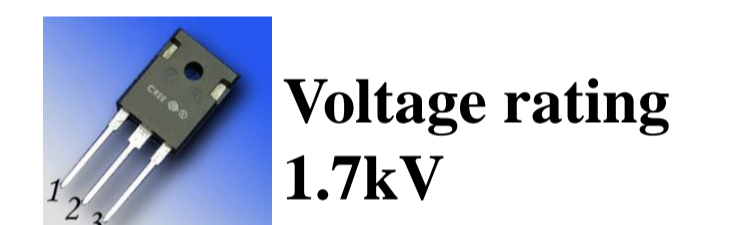
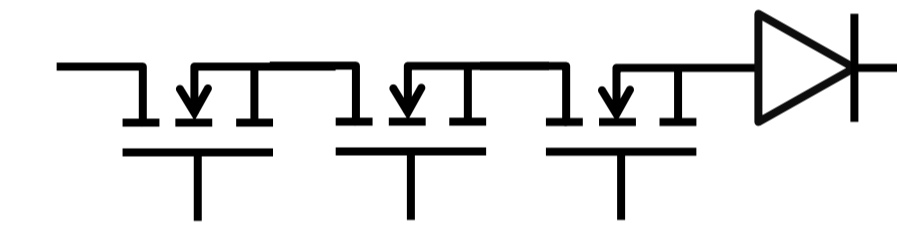


- "Low" voltage DIODE
- MOSFET:

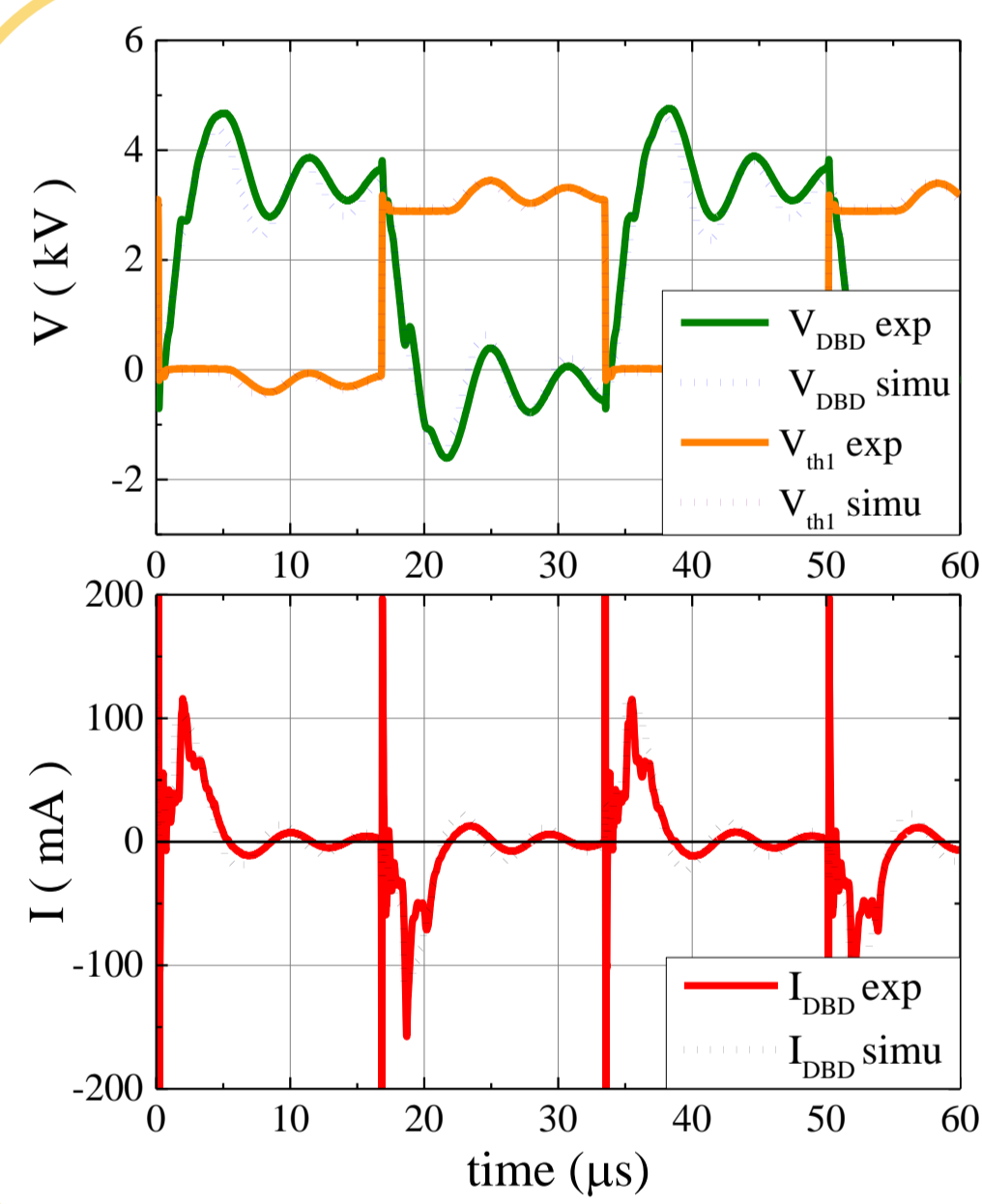
- High voltage SIC MOSFET



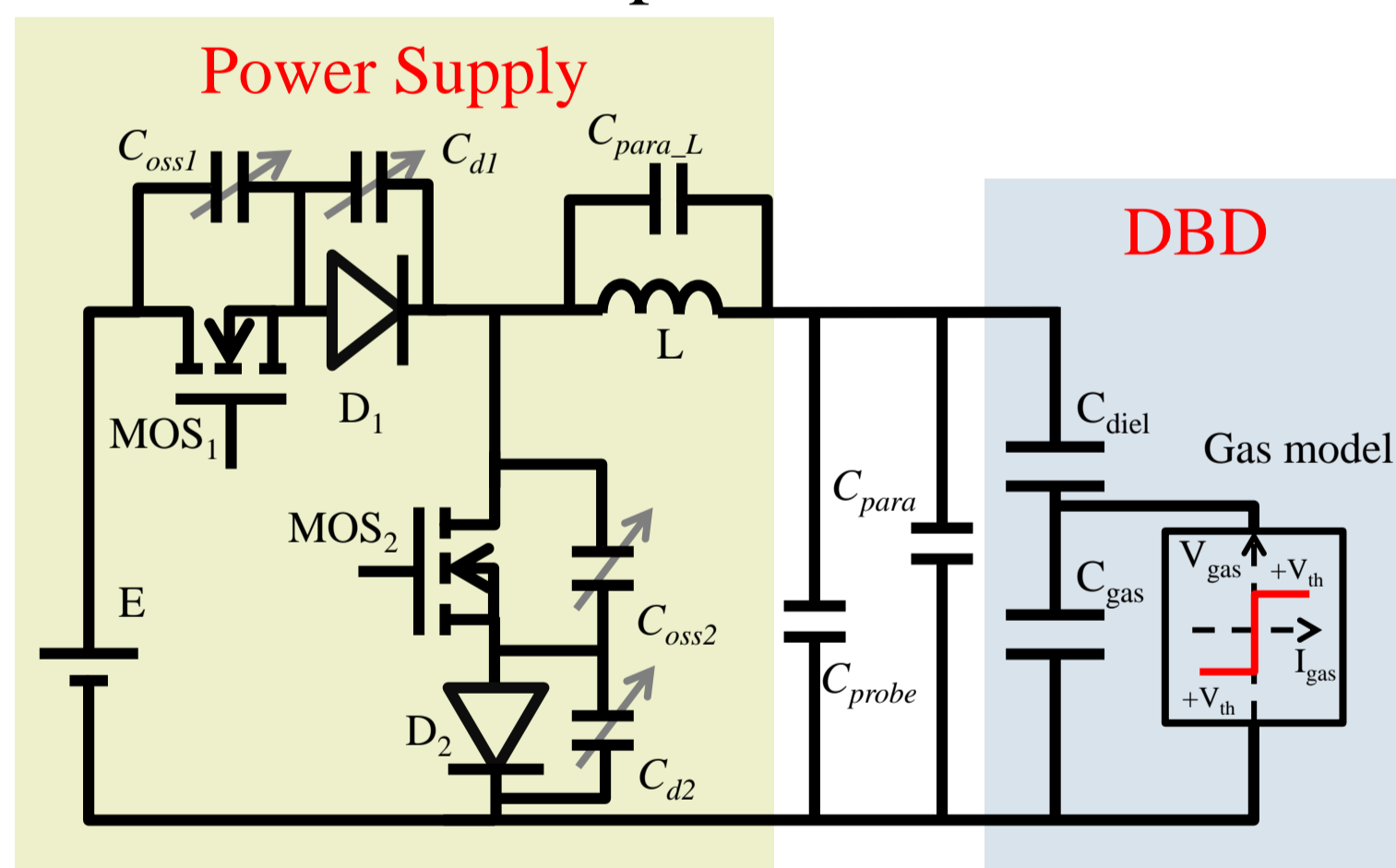
- "Low" voltage switches in series



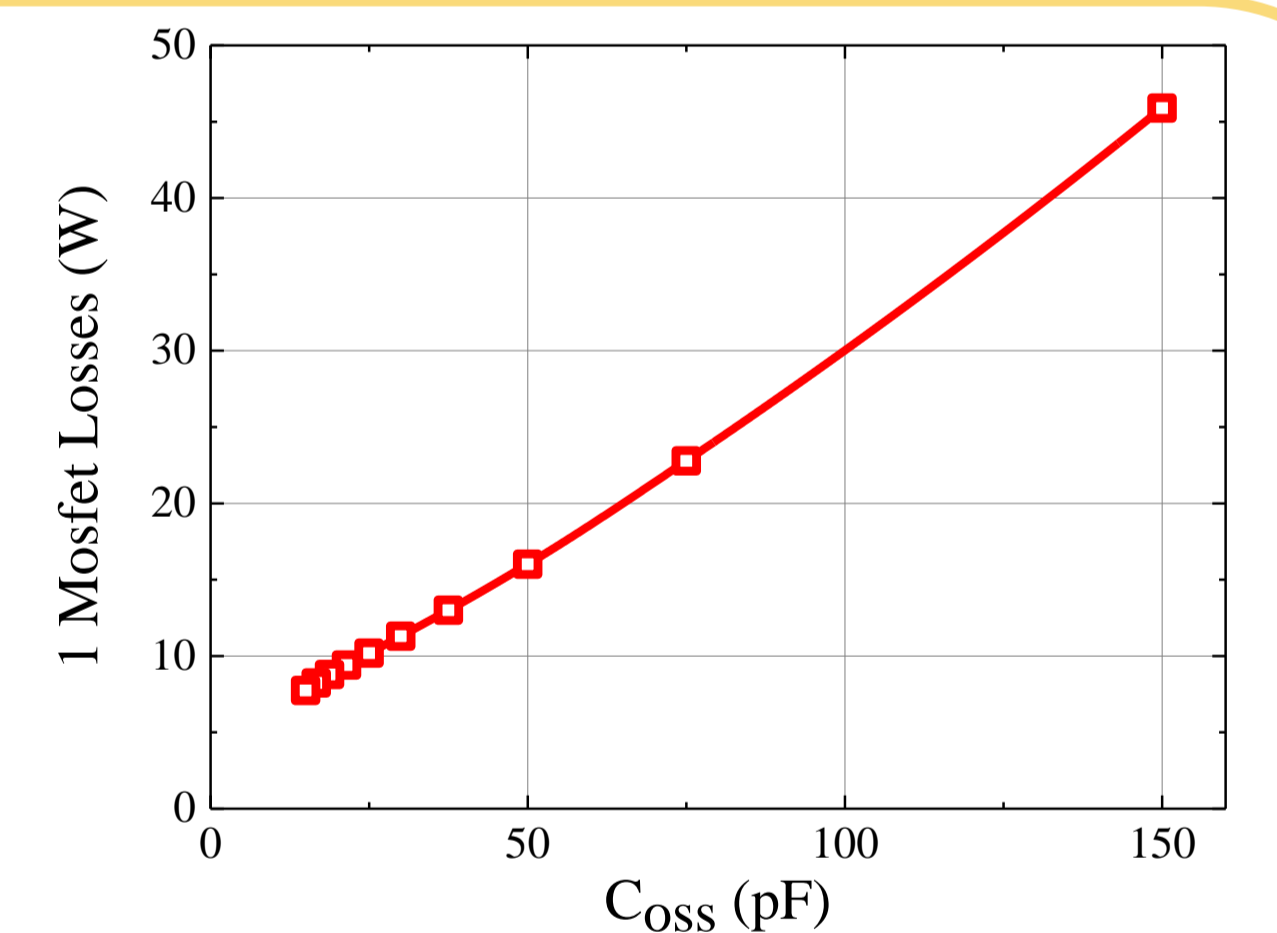
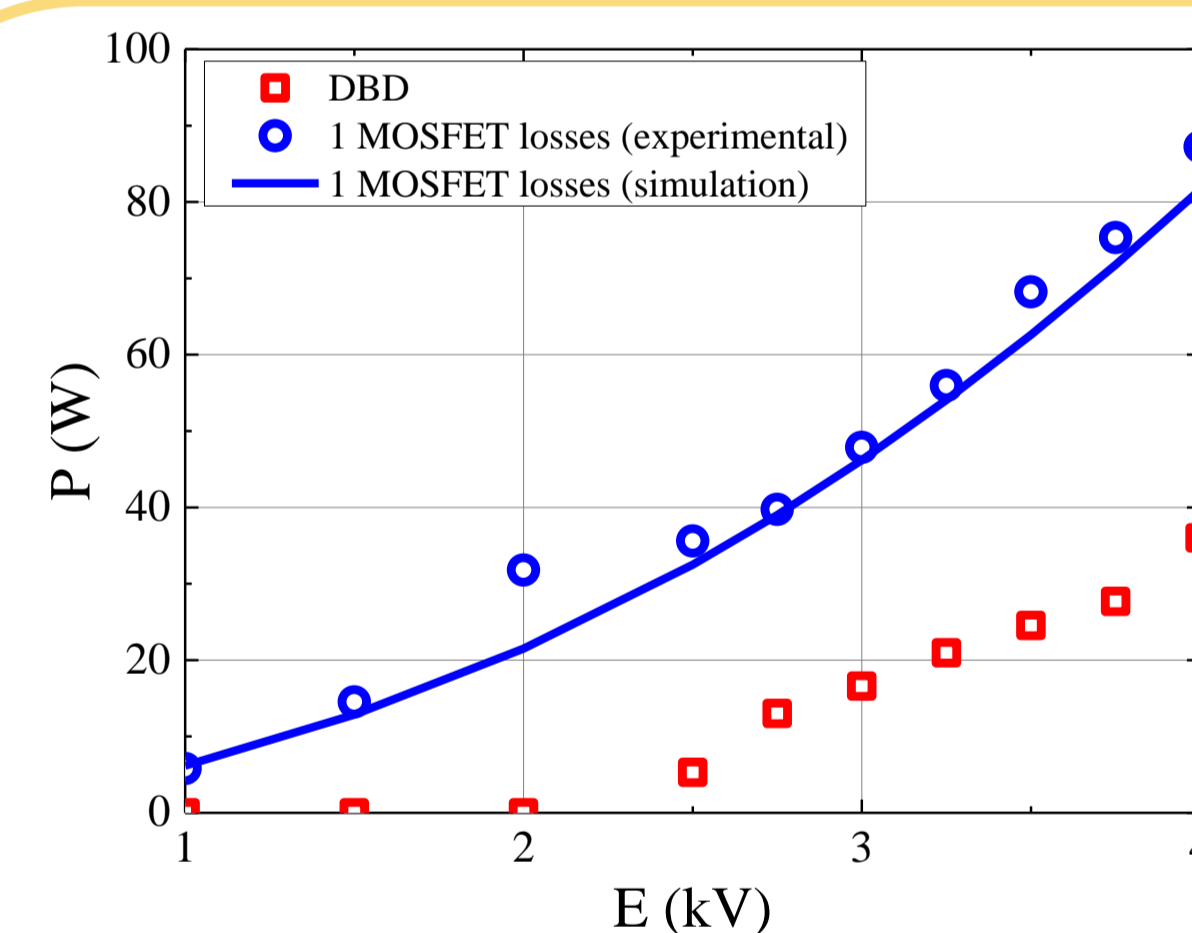
## 10 kV SIC experimental Validation



- DBD ignition with control of pulses energy
- Oscillations
- Parasitic capacitances



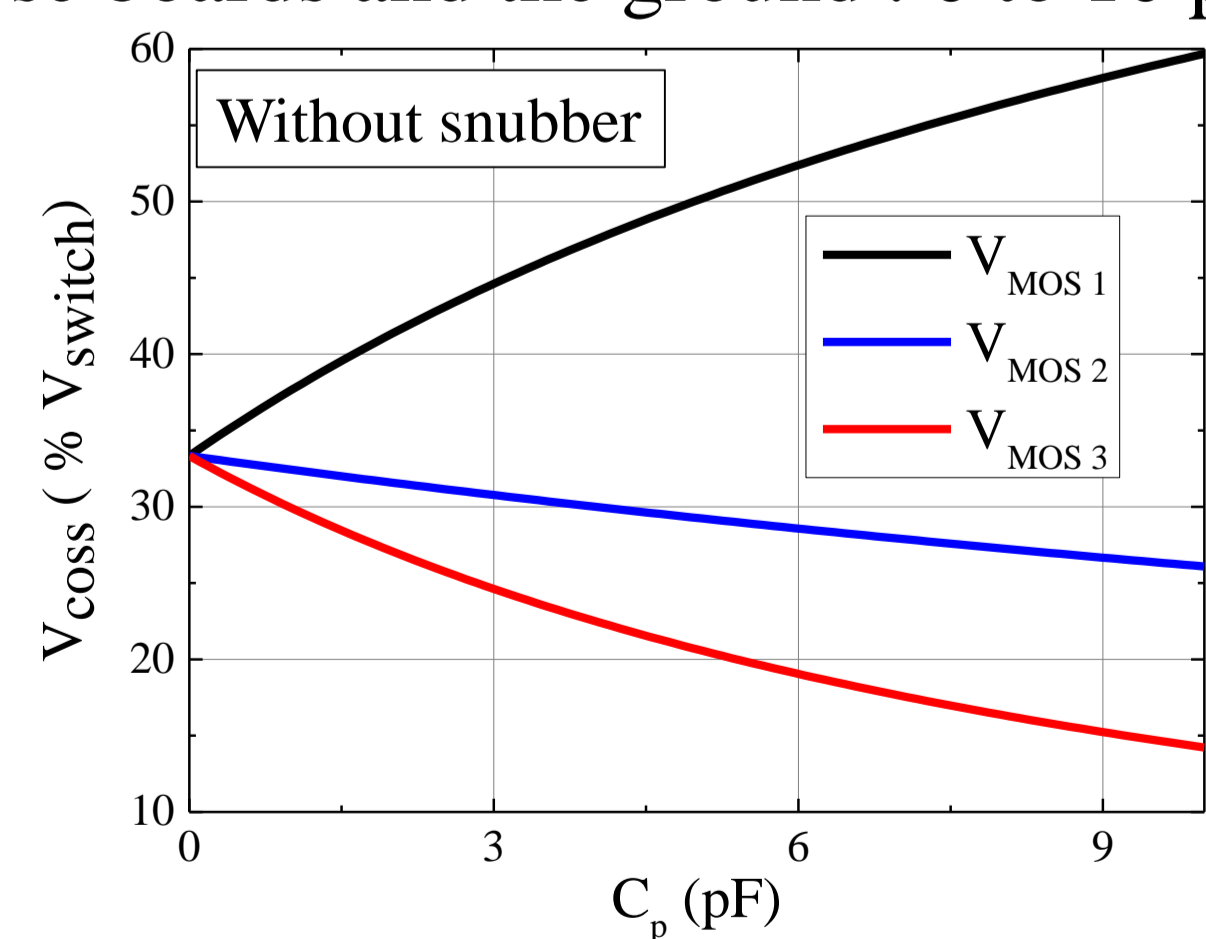
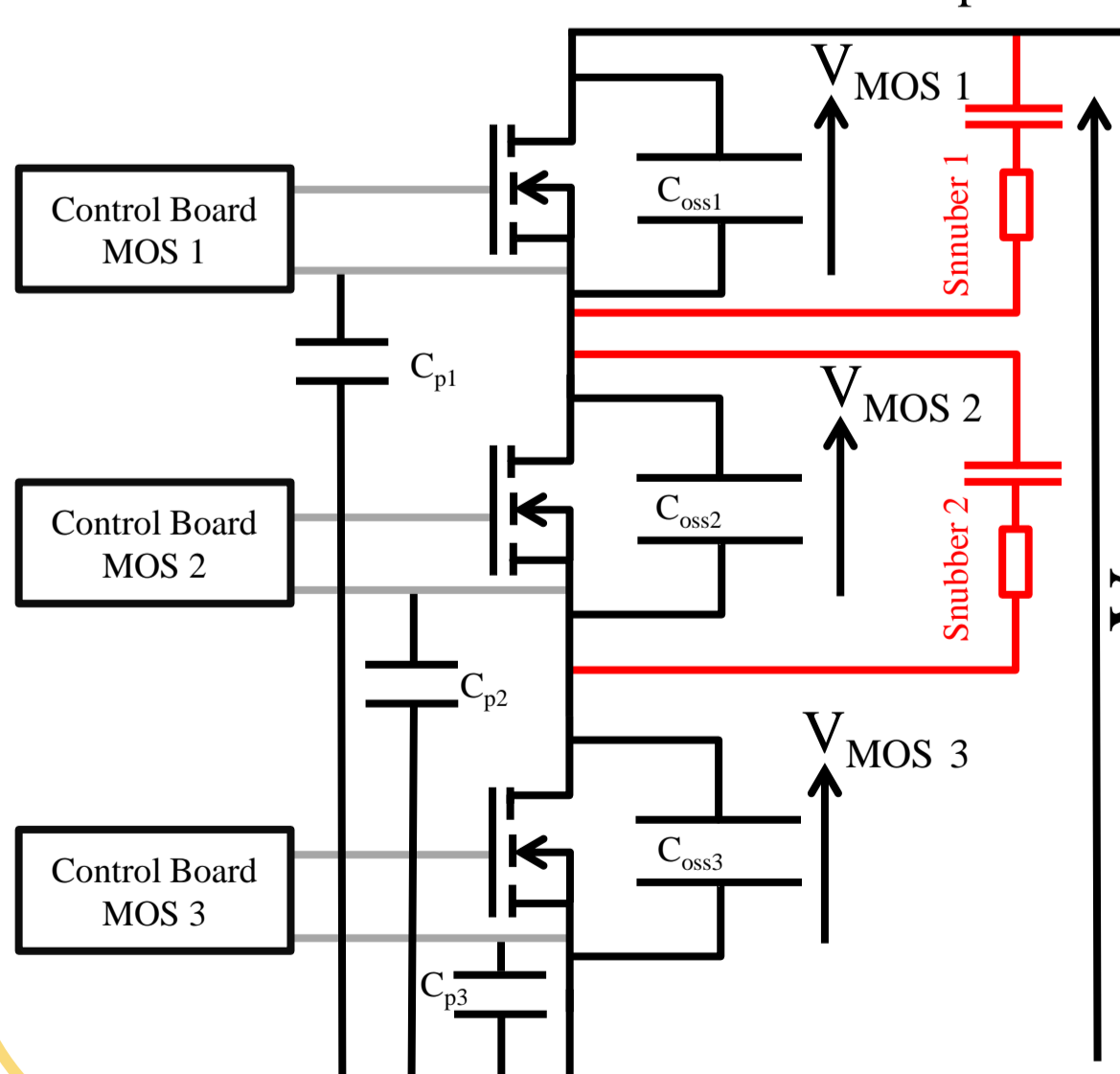
## Parasitic capacitance of the MOSFETS



- Intrinsic parasitic capacitance  $C_{oss}$  of the MOSFET sustain  $V_{DBD\_pos}$
- MOSFET turn-ON →  $E_{C_{oss}} = \frac{1}{2} \cdot C_{oss} \cdot V_{DBD\_pos}^2$  dissipated in the MOSFET
- USE LOW  $C_{oss}$  MOSFET in series.

## Parasitic capacitance and MOSFETS in series

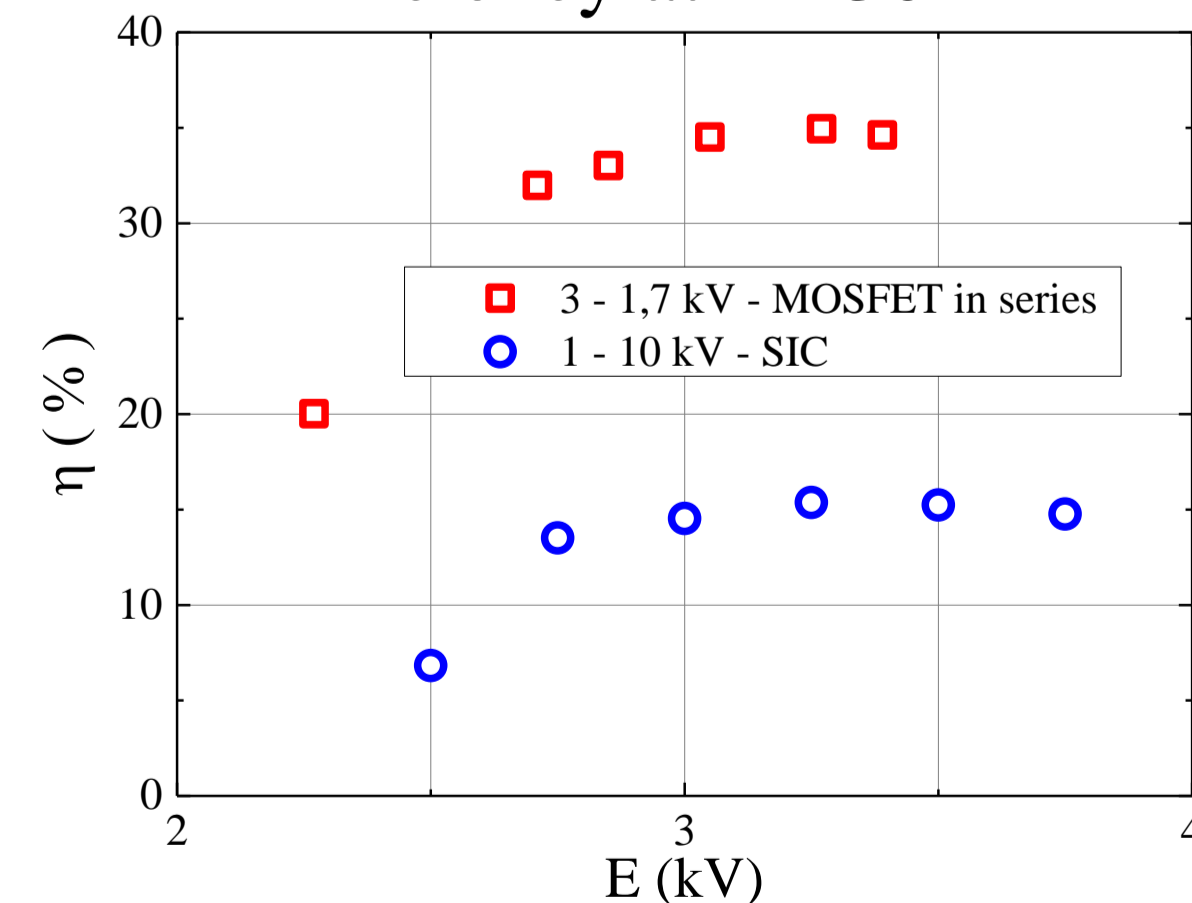
- Isolated boards for the control of each MOSFET
- Parasitic capacitance  $C_p$  between these boards and the ground : 0 to 10 pF



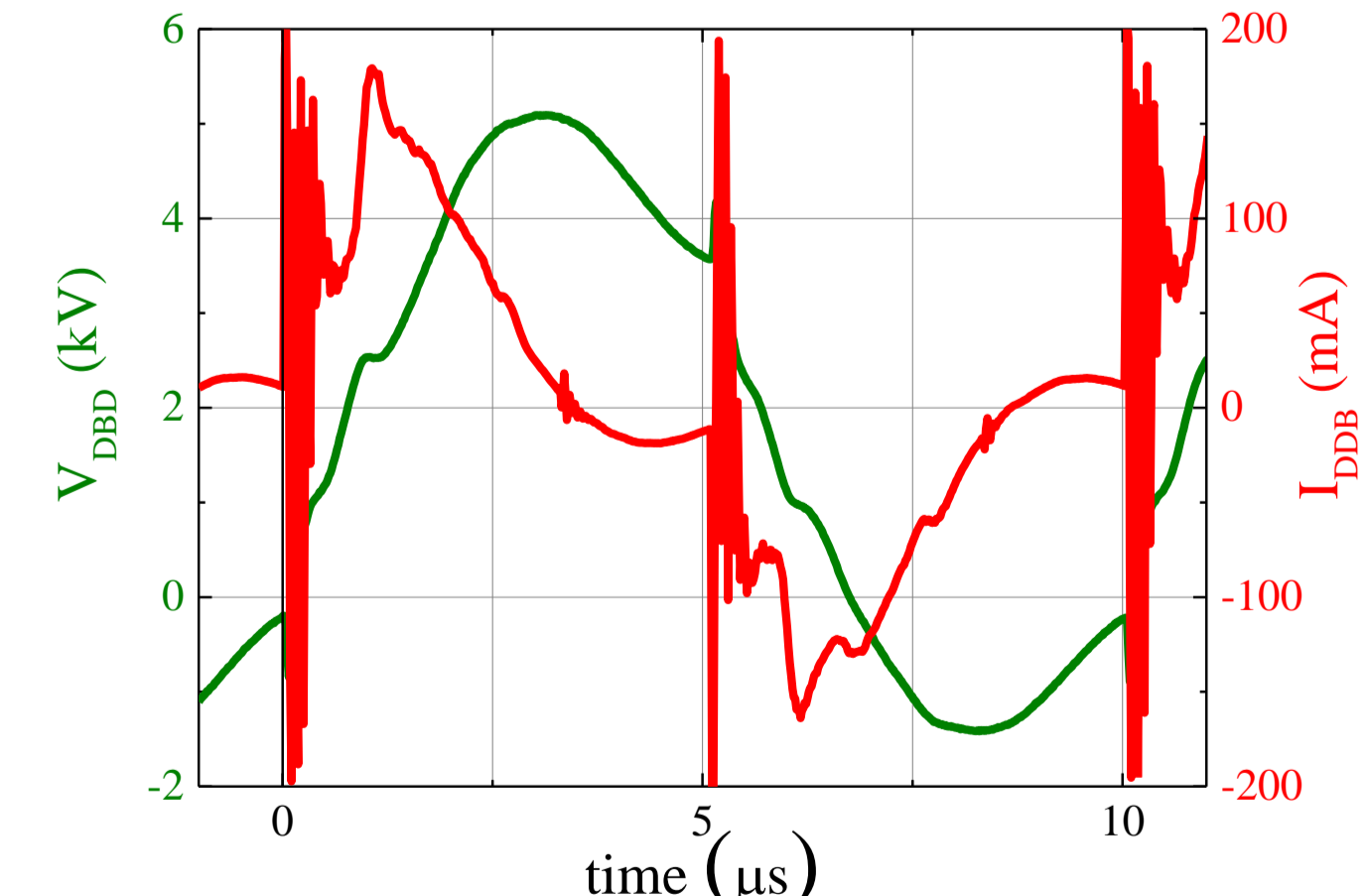
If all  $C_{oss}$  are equal, each MOSFET show different voltages  
→ SNUBBER (RC circuit) balances the MOSFETS voltages  
→ Losses in the SNUBBER

## Series MOSFET vs 10 kV SIC

### Efficiency at $f = 30$ kHz



### $P = 72$ W – $f = 100$ kHz



- At low power MOSFET in series are more efficient
- MOSFET in series allows to operate at frequencies up to 100 kHz
- Low  $t_{off} < 1$   $\mu$ s

## Conclusion

### Transformerless power supply

- Parasitic capacitances issues
- Over voltage on the transistor
- $C_{oss}$  implies losses at turn-ON

### SIC MOSFET 10 KV

- High  $C_{oss}$  value
- Losses depend on  $V_{DBD}$  and not on the power
- Adapted to high power applications

### MOSFET in series

- Voltage balance
- Add SNUBBER
- Well suited to low power applications