Parasitic Capacitances in transformerless power supply for DBD

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Context and experimental setup

Traditional High voltage power supply for DBD:
- Voltage applied to obtain breakdown > 4 kV
- Traditional semiconductors sustain 1.7 kV max

Transformer:
- Amplifies the voltage -> low voltage switch
- Parasitic elements (Lpara and Cpara)
- Overlap of converter’s switches (Loverlap)
- Current leak in parallel Coss capacitance
- Discharge duration and transferred power

Power supply : Operating Principle

DBD lamp:
- Length: 115 mm
- Gap: 20 mm - Ne-Cl - Pressure: 120 mBar
- Pm=100 W
- Breakdown voltage > 4 kV
- Coss=28 pF - Cpara=65 pF

High Voltage Switch

“Low” voltage DIODE
-> MOSFET:
- High voltage SIC MOSFET

10 kV SIC experimental Validation

- DBD ignition with control of pulses energy
- Oscillations -> Parasitic capacitances

Parasitic capacitance and MOSFETS in series

- Isolated boards for the control of each MOSFET
- Parasitic capacitance Coss between these boards and the ground: 0 to 10 pF

Series MOSFET vs 10 kV SIC

- At low power MOSFET in series are more efficient
- MOSFET in series allows to operate at frequencies up to 100 kHz
- Low $t_{on}<1 \mu s$

Efficiency at f = 30 kHz

P= 72 W – f=100 kHz

Parasitic capacitance of the MOSFETS

- Intrinsic parasitic capacitance Coss of the MOSFET sustain $V_{DBD,post}$
- MOSFET turn-ON $E_f = \frac{1}{2} \frac{L_{MOSFET}}{C_{oss,post}}$ dissipated in the MOSFET
- USE LOW Coss MOSFET in series.

Conclusion

Transformerless power supply
- Parasitic capacitance issues
- Over voltage on the transistor
- Coss implies losses at turn-ON
- Adapted to high power applications

SIC MOSFET 10 kV
- High Coss value
- Losses depend on $V_{DBD}$ and not on the power

MOSFET in series
- Voltage balance
- Add SNUBBER
- Well suited to low power applications