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Elimination of Circulating Current in Wide Range LLC Resonant Converter with a Hybrid Bridge and Simultaneous PWM and PFM Control

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Abstract—A hybrid bridge LLC-type converter is proposed for wide range dc-dc resonant conversion, to eliminate circulating current with the simultaneous use of pulsewidth modulation and pulse frequency modulation. The exact model of the converter is derived based on time domain analysis to aid design and control. Secondary side and output capacitor rms currents are significantly reduced, benefitting low output voltage/high power designs in terms of lower cooling and output filtering requirements. Absence of the L_m - L_r - C_r resonance interval, also suppresses secondary side parasitic ringing and can help to mitigate EMI issues. A GaN-based prototype of the converter is built and tested at 400V/18-36V, 500W. Analytical and experimental comparisons made with a standard LLC converter as well as with an alternative fixed frequency modulation scheme, validate the reduction of rms currents enabled by the proposed method and its potential for increased efficiency at higher power levels.

I. INTRODUCTION

The LLC resonant converter [1] (Fig. 1) is today one of the most established topologies for isolated dc-dc resonant conversion due to its simple circuit structure, soft switching characteristics, ability to regulate to zero load and scope for magnetic integration.

While the performance of the LLC resonant converter in terms of power density and efficiency can hardly be matched for medium to high frequency operation, its superiority is more contestable in wide input/output range applications. The LLC converter is preferably employed in the DCMB2/PO mode [2] [3] where its inverting bridge ZVS + rectifying bridge ZCS [4] characteristic can be exploited. With the isolation transformer turns ratio, n designed to place the minimum gain requirement at the series resonant point, when the switching frequency, f_s is pulled down towards the parallel resonant frequency to attain higher gains as shown in Fig. 2(a), the more prominent the parallel resonant facet of the LLC converter becomes as an increasing amount of circulating current is introduced in the primary side of the circuit.

This behaviour is illustrated in Fig. 2(b) where the resonant current i_{Lr} , the magnetizing current i_{Lm} and output side diode currents $i_{D1/4}$ are shown for the minimum and maximum gain points in a wide range design where $M_{\min} = 1$ and $M_{\max} = 2$. Ignoring the short deadtime interval that is

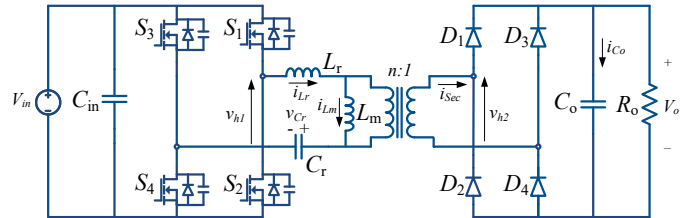


Fig. 1. The LLC resonant converter

normally allowed, for M_{\min} , i_{Lr} and i_{Lm} become equal at half of the switching period, $T_s/2$ just before the primary bridge is switched to invert the polarity of the square wave being applied to the resonant tank. The magnetizing inductance L_m does not participate in resonance but only ensures a minimum tank current level to assist the ZVS turn-on of incoming switches. The primary and secondary sides of the converter are always connected and power transfer from the input to the output is distributed over the entire switching period T_s through the diodes that operate in boundary conduction mode.

At M_{\max} , the direct power transfer interval is drastically reduced – the instant when i_{Lr} equals i_{Lm} occurs very early in every half switching period. The input and output sides of the converter are disconnected at t_1 , and all of the input source energy flows into L_m for $t_1 \leq t < T_s/2$ building up its current for voltage boost operation. On the output side, diodes do not conduct and the load, R_o is fed from the output capacitor, C_o . The prolonged zero power interval not only increases the circulating current on the primary side, but also increases the peak and rms currents of the output bridge rectifier that operates in highly discontinuous conduction mode. This results in increased conduction losses for the converter, when compared to the case where the input or the output voltage corresponding to that maximum gain point had been placed at the series resonant point.

As a solution to this inherent problem of wide range LLC resonant converters, a new modulation scheme based on a modified primary bridge [5]–[8], with the addition of two switches giving access to the input dc bus midpoint,

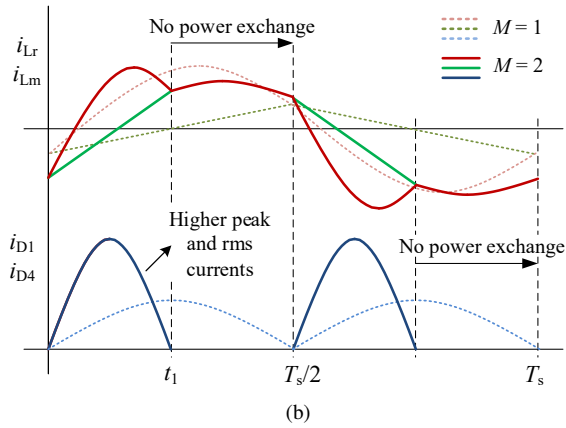
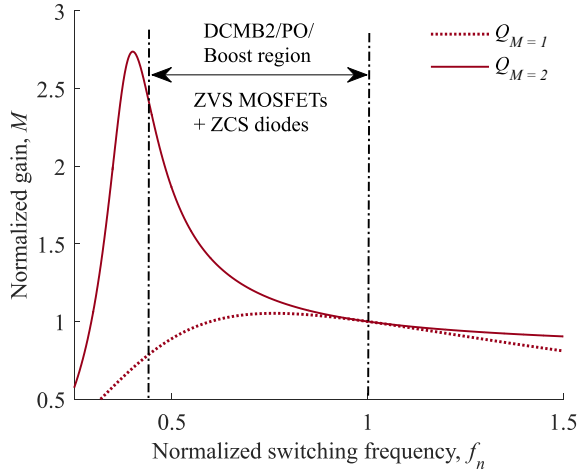


Fig. 2. (a) Gain v/s frequency characteristics of LLC converter for quality factors corresponding to $M = 1$ and $M = 2$ at constant power and (b) comparison of LLC resonant current i_{Lr} , magnetizing current i_{Lm} and diode currents $i_{D1/4}$ for conversion gains $M = 1$ and $M = 2$

is proposed. This introduces a new voltage level $V_{in}/2$ into the system, which in essence gives the primary bridge the ability of alternating between a half bridge and a full bridge configuration within the same switching cycle. The modulation strategy combines the duty ratio control of two possible voltage levels V_{in} and $V_{in}/2$ that can be imposed onto the resonant tank along with the frequency of their application to achieve two control objectives – traditional voltage regulation and elimination of the zero power exchange intervals/circulating currents in the converter within a gain range $M \in [0.5 \ 1]$, that corresponds to a gain range $M \in [1 \ 2]$ for a regular LLC converter with same input and output voltage specifications.

Usage of combined pulsewidth modulation (PWM) and pulse frequency modulation (PFM) can be found in [9], [10] but they are employed in distinct operating intervals and/or to address different problems: in [9] PFM is applied during regular operation and PWM control is applied only in abnormal condition for hold up time compensation, while the hybrid control method is used to address microcontroller limitations at high frequencies in [10]. A similar hybrid bridge

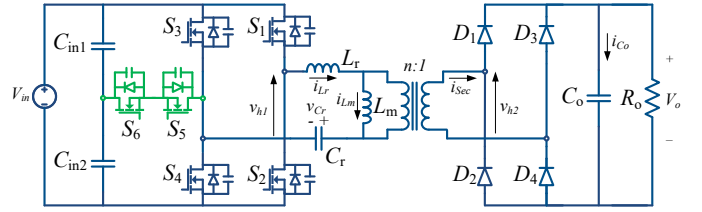


Fig. 3. Proposed two-parameter controlled hybrid bridge LLC resonant converter

LLC resonant converter, is reported in [7] but the resulting topology is controlled by PWM only at fixed frequency to facilitate magnetics and filter designs; circulating currents still exist and compromise efficiency.

The paper is organized as follows: Section II describes the operation of the converter with the proposed modulation scheme. Time domain analysis is applied to derive the converter model in Section III from which its characteristics are determined and explained. The performance of the converter, evaluated through comparisons with a benchmark LLC design and a fixed frequency modulation technique for the hybrid bridge LLC topology is presented in Section IV. Experimental validation and further comparative analysis is performed on a 400V/18-36V, 500W prototype in Section V.

II. MODULATION SCHEME AND CONVERTER OPERATION

The modulation drives all six switches at a certain switching frequency, f_s while simultaneously adjusting the duty ratio, D of the T-type leg to achieve two targets – gain setpoint and elimination of the zero power exchange intervals/circulating currents in the converter. More specifically, three complementary switch pairs can be identified: $S_1(\overline{S_2})$, $S_3(\overline{S_5})$ and $S_4(\overline{S_6})$. S_1 and S_2 have a fixed duty ratio of 0.5. S_4 is controlled at a particular duty ratio and its rising edge is synchronized with that of S_1 . S_4 conduction interval represents full-bridge mode of operation while its complementary switch S_6 conduction interval represents half-bridge mode of operation during a positive half cycle. Opposite phase complementary switches S_3 and S_5 are controlled in a similar fashion, synchronized with S_2 for conduction during the negative half period.

The operation of the converter can be fully described by the time-domain evolution of the resonant current i_{Lr} , the resonant capacitor voltage v_{Cr} and the magnetizing inductor current i_{Lm} during five equivalent circuit state intervals (Fig. 4 and Fig. 5) that make up half a switching period. Voltages, time, currents and frequency are normalized using the following bases: $V_{base} = V_{in}$, $t_{base} = \theta/\omega_r$, $I_{base} = V_{in}/Z_o$ and $f_{base} = f_r$, where V_{in} is the converter input dc bus voltage, $\omega_r = 1/\sqrt{L_r C_r}$ is the resonant tank angular frequency, $Z_o = \sqrt{L_r/C_r}$ is the resonant tank characteristic impedance and $f_r = \omega_r/2\pi$ is the resonant tank frequency. A normalized half period is given by

$$\gamma = \omega_r \frac{T_s}{2} = \frac{\pi}{f_n} \quad (1)$$

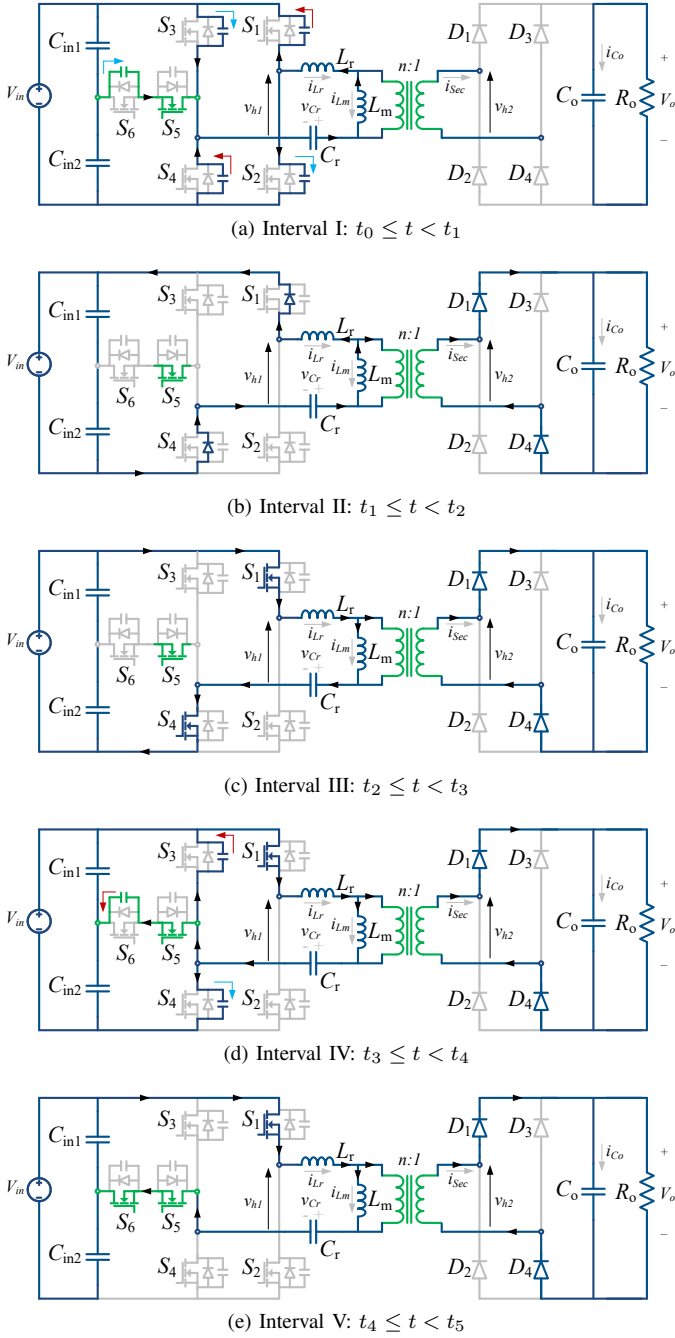


Fig. 4. Converter equivalent switching states during a positive half cycle

where T_s is the switching period and f_n is the normalized switching frequency, given by

$$f_n = \frac{f_s}{f_r} \quad (2)$$

1) *Interval 1* ($t_0 \leq t < t_1$): Before t_0 , during the negative half switching period, the converter was operating in half bridge mode, with switches S_2 , S_5 and S_6 carrying the negative magnetizing current. At $t = t_0$, switches S_2 and S_6 are turned off. Charges on the switch output capacitances $C_{oss1} - C_{oss6}$ of the switch network $S_1 - S_6$ start to redistribute themselves with the aid of the magnetizing current: 1) C_{oss1}

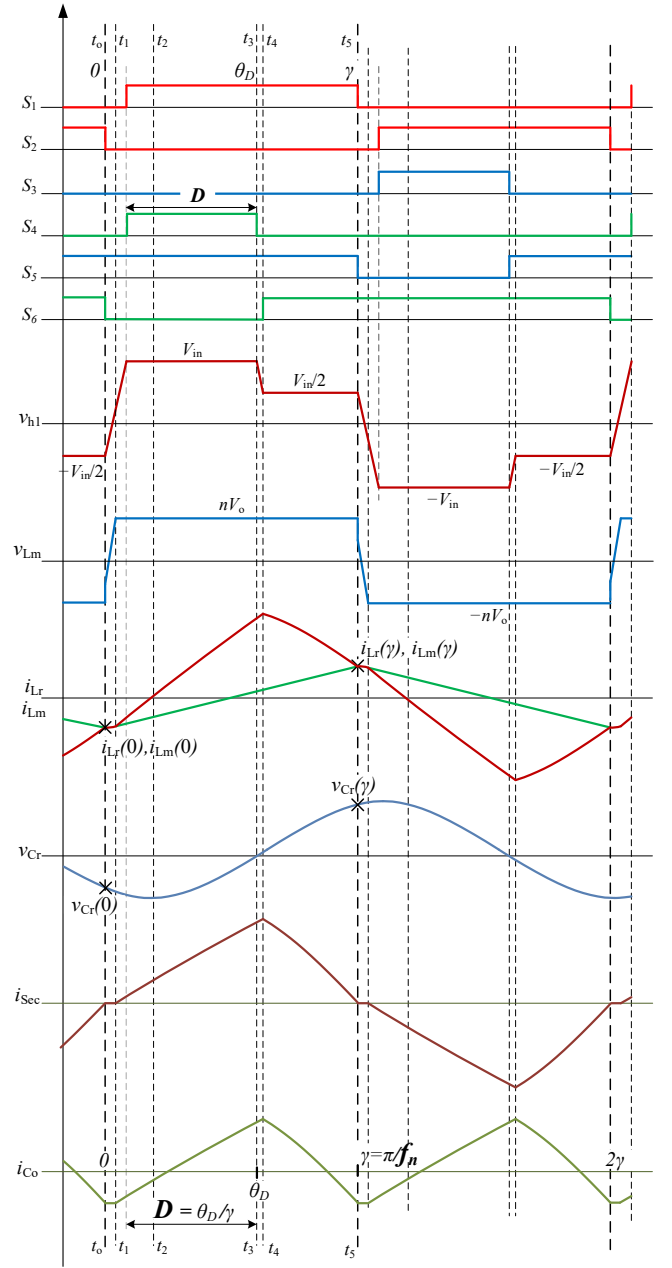


Fig. 5. Converter gating signals S_1 - S_6 , primary bridge voltage v_{h1} , magnetizing inductor voltage v_{Lm} , resonant inductor current i_{Lr} , magnetizing inductor current i_{Lm} , resonant capacitor voltage v_{Cr} , secondary bridge current i_{Sec} and output capacitor current i_{Co}

starts discharging from V_{in} to 0; 2) C_{oss2} starts charging from 0 to V_{in} ; 3) C_{oss3} starts charging from $V_{in}/2$ to V_{in} ; 4) C_{oss4} starts discharging from $V_{in}/2$ to 0; 5) C_{oss5} is unaffected and remains discharged as S_5 is kept on; 6) C_{oss6} starts charging from 0 to $V_{in}/2$.

The primary bridge voltage v_{h1} starts inverting its polarity from $-V_{in}/2$ to V_{in} and the magnetizing inductor L_m , part of a resonant tank being subjected to a linearly increasing excitation voltage v_{h1} , sees its voltage v_{Lm} rising as well. The input side and output sides of the converter are disconnected

during this short deadtime interval, allowed to ensure 1) ZCS turn-off of diodes D_2 and D_3 that were conducting in the previous interval and 2) ZVS turn-on of S_1 and S_4 in interval 3.

2) *Interval 2* ($t_1 \leq t < t_2$): At $t = t_1$, v_{Lm} reaches the reflected output voltage nV_o and secondary side diodes D_1 and D_4 get forward biased and start to conduct to re-establish power transfer. On the primary side, body diodes of switches S_1 and S_4 start to conduct just after their respective C_{oss} are completely discharged. The full dc bus voltage V_{in} is applied to the resonant tank. Series resonance between elements L_r and C_r causes the primary current i_{Lr} to increase whereas L_m is clamped to the reflected output voltage nV_o and its current increases linearly. The difference between i_{Lr} and i_{Lm} reflected to the secondary side is fed to the output capacitor C_o and load resistor R_o through diodes D_1 and D_4 . The normalized resonant inductor current i_{Lr} , magnetizing current i_{Lm} and resonant capacitor voltage v_{Cr} are given by

$$i_{Lr}(\theta) = i_{Lr}(0) \cos \theta + [1 - M - v_{Cr}(0)] \sin \theta \quad (3a)$$

$$i_{Lm}(\theta) = i_{Lm}(0) + M\theta/k \quad (3b)$$

$$v_{Cr}(\theta) = 1 - M - [1 - M - v_{Cr}(0)] \cos \theta + i_{Lr}(0) \sin \theta \quad (3c)$$

where $M = nV_o/V_{in}$ is the normalized output voltage or gain and k is the resonant tank inductance ratio L_m/L_r . Gating signals of S_1 and S_4 can be applied from this point onward before the zero crossing of i_{Lr} for their ZVS turn-on.

3) *Interval 3* ($t_2 \leq t < t_3$): At $t = t_2$, i_{Lr} polarity reverses and switches S_1 and S_4 turn on with ZVS. Currents and voltages of the resonant tank are still given by (3).

4) *Interval 4* ($t_3 \leq t < t_4$): At $t = t_3$, gating signal of S_4 is removed. Charges of switch output capacitances $C_{oss3} - C_{oss6}$ of the T-type leg start to redistribute themselves with the aid of the positive resonant tank current: 1) C_{oss3} starts discharging from V_{in} to $V_{in}/2$; 2) C_{oss4} starts charging from 0 to $V_{in}/2$; 3) C_{oss5} is unaffected and remains uncharged as S_5 is kept on; 4) C_{oss6} starts discharging from $V_{in}/2$ to 0. Its body diode starts conducting hereafter, preparing for its ZVS turn-on. This interval marks the end of operation in full-bridge mode at $\theta = \theta_D$, based on which the duty ratio of the converter is defined as $D = \theta_D/\gamma$.

5) *Interval 5* ($t_4 \leq t < t_5$): At $t = t_4$, gating signal of S_6 is applied and turns on under ZVS; current flowing in its body diode is transferred to the MOSFET channel that starts conducting in synchronous rectification mode. The converter operates in half-bridge mode, with the resonant tank being excited by half of the dc bus voltage. The resonant tank normalized currents and voltages are now given by

$$i_{Lr}(\theta) = i_{Lr}(\theta_4) \cos(\theta - \theta_4) + [0.5 - M - v_{Cr}(\theta_4)] \sin(\theta - \theta_4) \quad (4a)$$

$$i_{Lm}(\theta) = i_{Lm}(\theta_4) + M(\theta - \theta_4)/k \quad (4b)$$

$$v_{Cr}(\theta) = 0.5 - M - [0.5 - M - v_{Cr}(\theta_4)] \cos(\theta - \theta_4) + i_{Lr}(\theta_4) \sin(\theta - \theta_4) \quad (4c)$$

III. CONVERTER MODEL AND CHARACTERISTICS

Based on the development of the resonant tank state variables from (3) and (4), with the short deadtime intervals $t_0 \leq t < t_1$ and $t_3 \leq t < t_4$ ignored, and applying half-wave symmetry condition

$$i_{Lr}(\gamma) = -i_{Lr}(0) \quad (5a)$$

$$v_{Cr}(\gamma) = -v_{Cr}(0) \quad (5b)$$

tank currents equivalence at half period

$$i_{Lr}(\gamma) = i_{Lm}(\gamma) \quad (5c)$$

power transfer equivalence over half period

$$\frac{1}{\pi} \int_0^\pi (i_{Lr}(\theta) - i_{Lm}(\theta)) d\theta = I_o = \frac{8MQ}{\pi^2} \quad (5d)$$

where the quality factor Q is given by

$$Q = \frac{\pi^2 Z_o}{8n^2 R_o} = \frac{\pi^2 I_o}{8 V_o} \frac{1}{n^2} Z_o = \frac{\pi^2 P_o}{8 (nV_o)^2} Z_o \quad (6)$$

the time domain steady-state model of the converter with the proposed two parameter modulation strategy can be derived as

$$i_{Lr}(0) + i_{Lr}(0) \cos \gamma + [1 - M - v_{Cr}(0)] \sin \gamma - 0.5 \sin(\gamma - \theta_D) = 0 \quad (7a)$$

$$0.5 + v_{Cr}(0) - [M - 0.5 \cos(\gamma - \theta_D) + [1 - M - v_{Cr}(0)] \cos \gamma - i_{Lr}(0) \cos \gamma] = 0 \quad (7b)$$

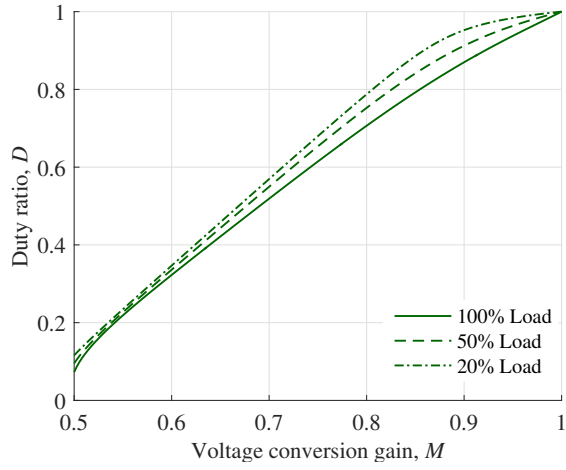
$$i_{Lr}(0)(\cos \gamma - 1) + [1 - M - v_{Cr}(0)] \sin \gamma - 0.5 \sin(\gamma - \theta_D) - M\gamma/k = 0 \quad (7c)$$

$$[1 - M - v_{Cr}(0)](1 - \cos \gamma) + 0.5[\cos(\gamma - \theta_D) - 1] + i_{Lr}(0)[\sin \gamma - \gamma] - M\gamma^2/2k - 8MQ\gamma/\pi^2 = 0 \quad (7d)$$

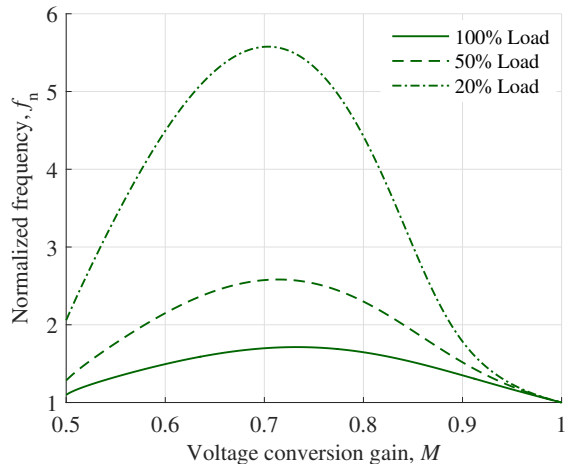
The model – a non-linear system of equations – is solvable with numerical solver packages for e.g. MATLAB with its function *fsolve*, for θ_D and γ that correspond to the duty ratio and normalized frequency to be applied for a desired M at designed values of k and Q . Fig. 6 shows the duty ratio and normalized frequency variations over $M \in [0.5, 1]$ for $k = 8$ and $Z_o = 20\Omega$, for different load conditions. While the duty ratio is monotonically increasing, the normalized frequency characteristic curves have parabolic natures, that in an actual implementation would require a non-linear controller. It can also be observed that the frequency compensation required to maintain the converter in zero circulating current mode, has a rapidly peaking behaviour at light loads. A maximum frequency limit can be set above which the converter is frozen and operated with duty ratio only as in [7], based on an optimum between switching and conduction losses in the converter.

IV. CONVERTER PERFORMANCE EVALUATION AND BENCHMARKING

The performance of the proposed converter is evaluated against a conventional wide range LLC converter as well as against the converter in [7] for the 400V/18-36V dc-dc stage of a 24V/3kW battery charger. For the comparison to



(a)

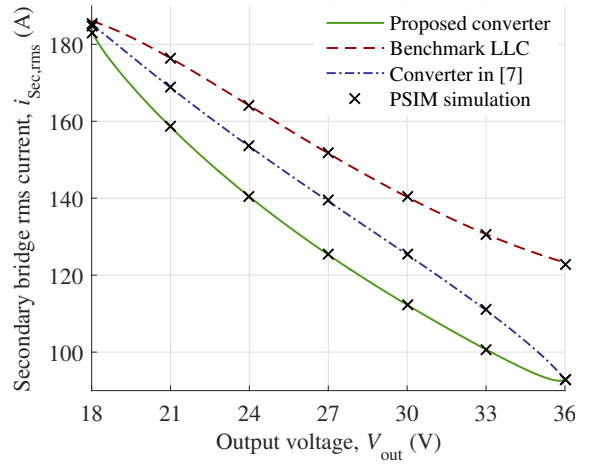


(b)

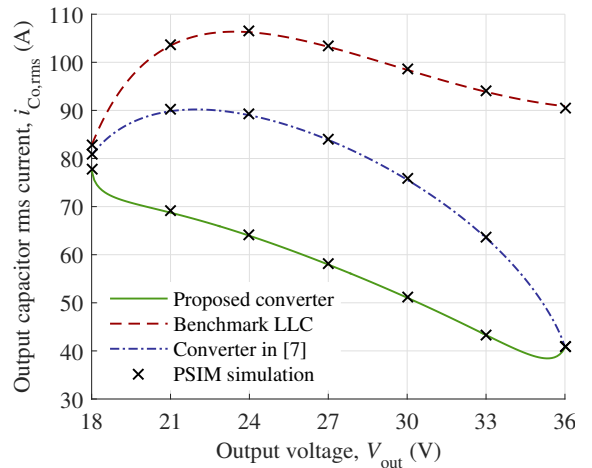
Fig. 6. Control to output characteristics of converter

be fair, the benchmark LLC converter is designed according to the methodology proposed in [11] to 1) maximize its tank characteristic impedance while keeping the converter in the DCMB2/PO mode throughout $M \in [1 \ 2]$ and 2) ensure ZVS at zero-load operation at minimum conversion gain with a maximum dc input voltage of 420V and a maximum switching frequency of $1.35f_n$, specified. The proposed converter is designed based on 1) the minimum value of tank characteristic impedance above which the resonant tank currents cannot be sensibly reduced and 2) the maximum k to ensure ZVS throughout the entire voltage and load range. The converter in [7] is designed in a similar way and results in the same parameters as listed in Table I. All converters full load switching frequencies fall within 100kHz–200kHz.

In contrast to the conventional LLC converter, the proposed converter's normalized frequency $f_n > 1$ for boosting action (Fig. 6(b)), keeping the magnetics volume low while the step down characteristic of the converter halves the required transformer turns ratio. The gain for $M \in [0.5 \ 1]$ is not constrained by the quality factor and inductance ratio as in the case of the LLC converter, which simplifies the optimal



(a)



(b)

Fig. 7. Analytical comparison of the proposed converter's currents against two other converters for 400V/18-36V, 3kW constant power (a) secondary bridge rms currents and (b) output capacitor rms currents

design of the resonant tank.

Converter rms currents are analytically determined for $V_o \in [18V \ 36V]$, based on (3), (4) and (7). Corresponding time-domain models of the LLC converter operating in DCMB2/PO mode [3] as well as that of [7] are also solved for their respective rms currents. The accuracy of the calculated currents for

TABLE I
DESIGNED PARAMETERS FOR ANALYTICAL COMPARISONS

Parameters	Proposed converter	Benchmark LLC	Converter in [7]
n	11	22	11
$L_r(\mu\text{H})$	23.9	22.3	23.9
$L_m(\mu\text{H})$	287	89.1	287
$C_r(\text{nF})$	106	28.4	106
k	12	4	12
Z_o	15	28	15
$f_{r1}(\text{kHz})$	100	200	100
$C_{oss}(\text{pF})$	200	200	200
Deadtime(ns)	100	100	100

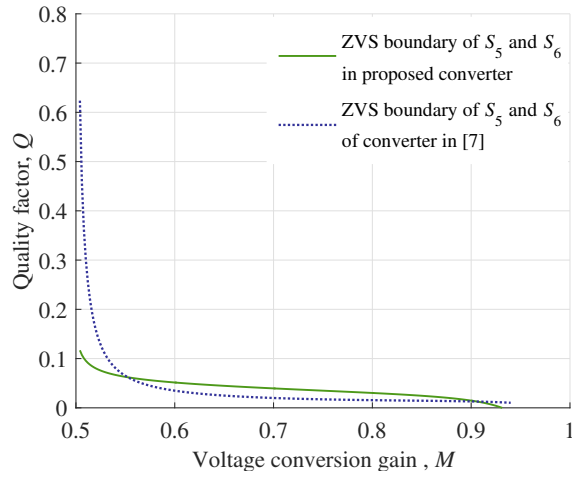


Fig. 8. ZVS boundaries of auxiliary switches S_5 and S_6 of proposed converter and the converter in [7]

all three converters are validated by PSIM circuit simulation. For this high step-down battery charger application, secondary side currents are particularly important to keep in check for conduction losses, cooling and filtering requirements to be minimized. Fig. 7 shows the full load secondary bridge rms current, $i_{Sec,rms}$ and the output capacitor rms currents, $i_{Co,rms}$ for the three designs. The proposed converter allows a solid reduction of current stresses in the secondary bridge and a significant reduction in output capacitor rms currents.

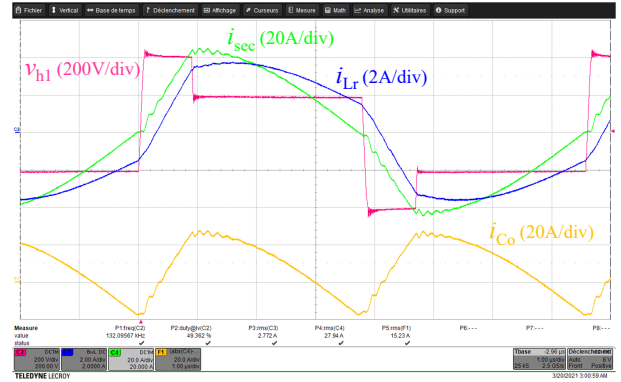
The proposed converter's main switches $S_1 - S_4$ achieve ZVS down to zero load and auxiliary switches S_5 and S_6 lose ZVS only at extremely light loads. Their ZVS range is derived based on the parameters in Table I and shown in Fig. 8. The ZVS boundary when the converter is controlled at fixed frequency as in [7], [8] is also plotted on the same diagram. Regions under each curve are their respective non-ZVS range. It can be observed that the proposed converter although having slightly lower ZVS range because of lower resonant current across the gain range, has an improved ZVS characteristic at very low M , where in comparison [7] loses ZVS of S_5 and S_6 for fairly high power levels.

TABLE II
DESIGNED PARAMETERS FOR EXPERIMENTAL COMPARISONS

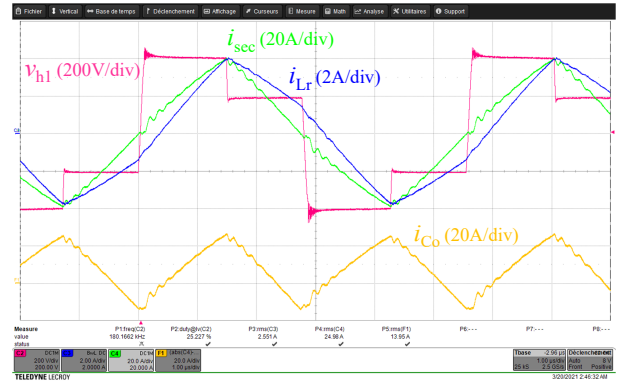
Parameters	Proposed converter	Benchmark LLC (Half-bridge)	Converter in [7]
n	11	11	11
$L_r(\mu\text{H})$	36.2	19.2	36.2
$L_m(\mu\text{H})$	286	76.7	286
$C_r(\text{nF})$	68	33	68
k	7.9	4	7.9
$Z_o(\Omega)$	23	24	23
$f_{r1}(\text{kHz})$	100	200	100
$C_{oss}(\text{pF})$	100	100	100
Deadtime(ns)	100	70	100
f_s range (kHz)	100-180	140-200	100

V. EXPERIMENTAL VALIDATION

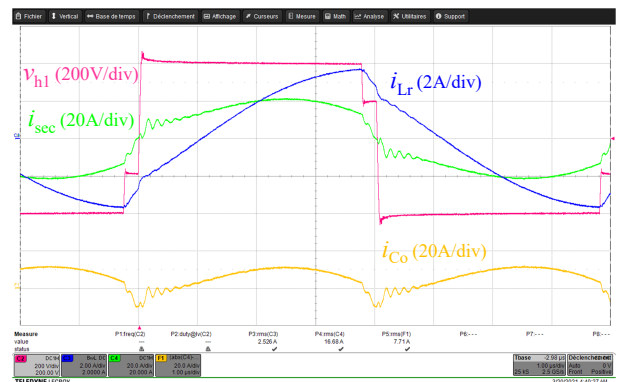
A 500W, 400V/18-36V GaN prototype is built to validate the operating principles of the converter. The primary bridge is made of GS66506T GaN HEMTs, ADuM4121-1 gate drivers and NKE0509DC isolated power supplies. The secondary bridge consists of STPS61H100C schottky rectifiers. The bridges are built on two different PCBs, to facilitate their reconfiguration into similar converter topologies with adjustment of the liaising resonant tank and transformer, for



(a)

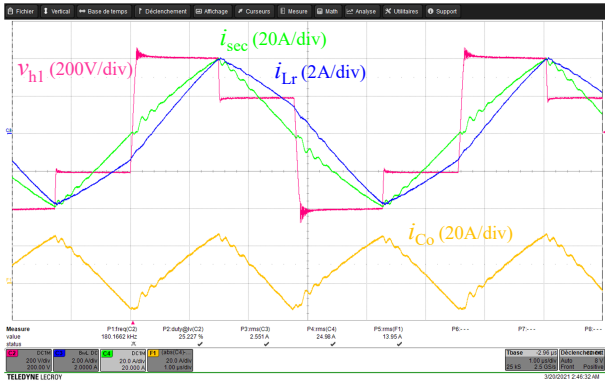


(b)

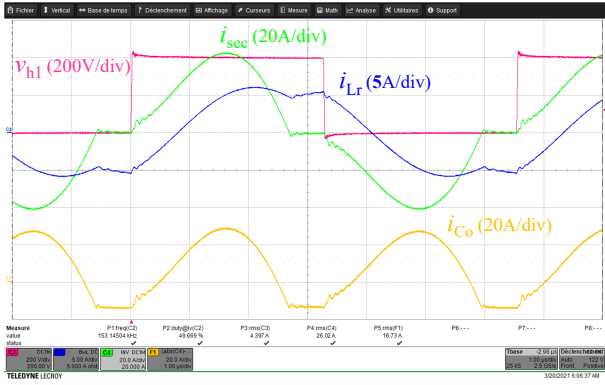


(c)

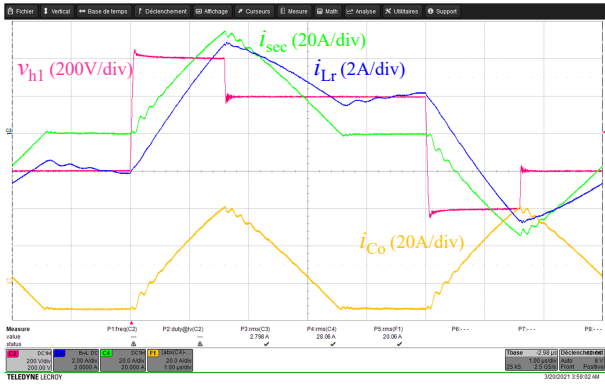
Fig. 9. Experimental waveforms of proposed converter at $V_{in} = 400\text{V}$ and $P_o = 500\text{W}$ across the output voltage range – (a) $V_o = 21\text{V}$: $D = 0.340$, $f_s = 158\text{kHz}$ (b) $V_o = 27\text{V}$: $D = 0.652$, $f_s = 180\text{kHz}$ and (c) $V_o = 33\text{V}$: $D = 0.920$, $f_s = 124\text{kHz}$



(a)



(b)

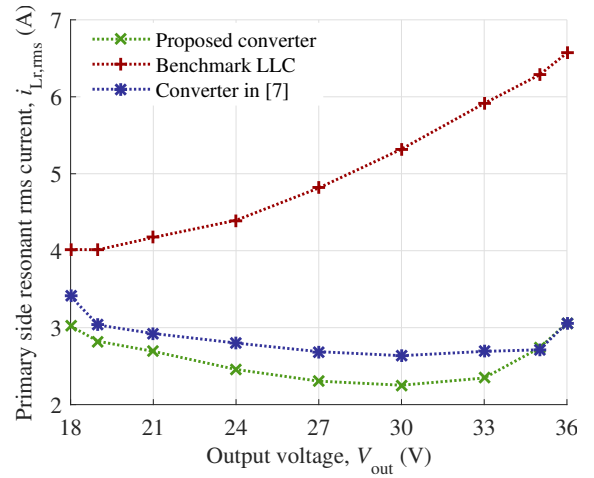


(c)

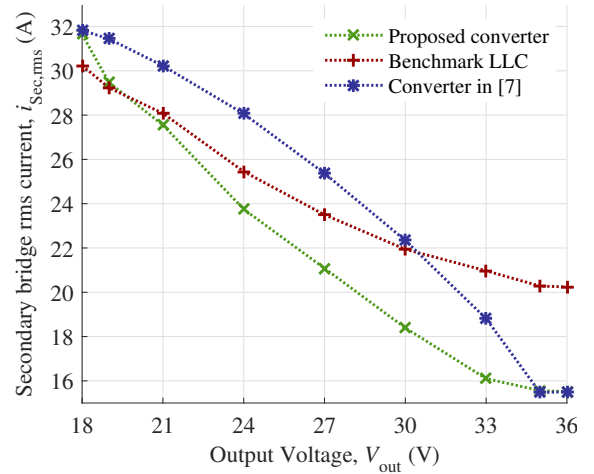
Fig. 10. Experimental comparison of proposed converter waveforms against two other converters at $V_{in} = 400V$, $P_o = 500W$ and $V_o = 24V$ – (a) proposed converter: $D = 0.524$, $f_s = 180kHz$ (b) benchmark LLC converter: $D = 1$, $f_s = 153kHz$ and (c) converter in [7]: $D = 0.320$, $f_s = 100kHz$

platform-like performance comparisons and benchmarking.

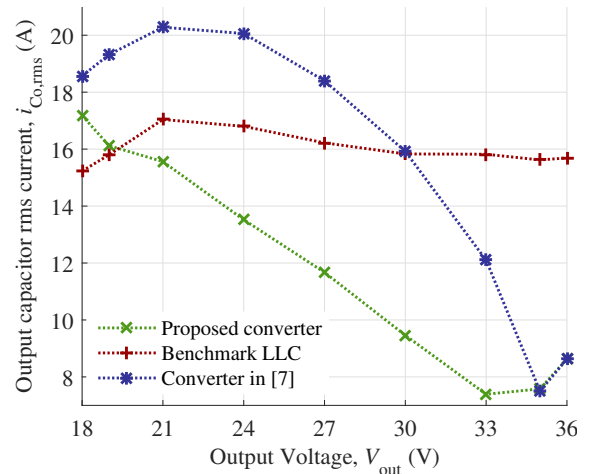
The proposed converter's waveforms: primary bridge voltage v_{h1} , resonant current i_{Lr} , secondary bridge current, i_{Sec} and output capacitor current, i_{Co} for three operating points across the output voltage range are shown in Fig. 9. Design parameters are listed in Table II. The two level step voltage v_{h1} applied to the resonant tank at a specified frequency and duty ratio is shown to effectively spread the secondary current over the switching period, thus eliminating the zero power exchange interval, as indicated by the zero crossing



(a)



(b)



(c)

Fig. 11. Experimental comparison of proposed converter currents against two other converters at $V_{in} = 400V$ and $P_o = 500W$ across the output voltage range – (a) primary side resonant currents (b) secondary bridge currents and (c) output capacitor currents

of i_{Sec} just before the end of the half period. This translates

into an efficiently utilized switching cycle by the secondary side current, of utmost importance in low output voltage/high current applications for conduction losses minimization.

The non-appearance of the zero power transfer interval, also signifies the suppression of parasitic ringing between the transformer secondary winding leakage inductance and diodes output capacitance frequently observed in LLC converters during the L_m - L_r - C_r resonance interval when the secondary is decoupled from the primary bridge. This may have a positive impact on the EMI performance of the proposed converter.

The analytical comparisons started in Section IV are pursued experimentally based on the same design methodologies to evaluate the performance of the converter. The benchmark LLC here is designed in its half bridge form rather than its full bridge configuration 1) as a more realistic design reference at this power level i.e. $< 1\text{ kW}$ and 2) allowing the same transformer with identical turns ratio to be used for all three converters. Design parameters are given in Table II.

Waveforms for v_{h1} , i_{Lr} , i_{Sec} and i_{Co} at nominal battery voltage $V_o = 24\text{V}$, are shown in Fig. 10. At this operating point, the L_m - L_r - C_r resonance interval starts appearing for the LLC converter, Fig. 10(b), and the secondary bridge discontinuous conduction mode only worsens for higher voltages. For the converter in [7], Fig. 10(c), the operating point $V_o = 24\text{V}$, falls within its worse case i_{Sec} discontinuous conduction mode region, but improves for higher operating voltages when approaching the second pure resonance point at $V_o = 36\text{V}$. Fig. 11 illustrates the variation of the rms values of primary side resonant current, secondary bridge and output capacitor currents recorded on the three prototypes for $V_o \in [18\text{V } 36\text{V}]$ at 500W constant power. Except at very low output voltage $V_o < 20\text{V}$ where it is slightly outperformed by the LLC converter – operating in the vicinity of its most efficient series resonance point – the superiority of the proposed converter is overt.

VI. CONCLUSION

A two-degrees-of-freedom modulation technique, based on minimal structural change to the input bridge, is proposed to address the highly discontinuous mode of power transfer in wide range LLC converters. A precise time-domain model of the converter is developed and used for designing, validating and evaluating its performance against state-of-the-art converters. Analytical, simulation and experiments run on a

500W , $400\text{V}/18\text{-}36\text{V}$ GaN prototype confirm the effectiveness of the proposed method in driving the system into boundary conduction mode at all operating points, thereby eliminating primary side circulating currents, lowering secondary side peak and rms currents, and significantly reducing output filter capacitor currents, for attaining higher power efficiency and density targets.

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