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An Efficient Model to Evaluate the Impact of Design parameters on Charge Pump Circuits' Performances: Application on RFID circuits

 1 H Aziza

 $1&\&2E.Bergeret$

1 L2MP-UMR CNRS 6137 ² IMT - Technopôle de Château Gombert ZI de Rousset BP 2 13451 Marseille Cedex 20, France F-13106 Rousset Cedex, France Hassen.Aziza@polytech.univ-mrs.fr Emmanuel.Bergeret@ieee.org Tel:(33)-491-054-784 Tel:(33)-442-688-815

Abstract

In this paper a charge pump model based on a DOE (Design Of Experiment) model generation technique is presented. The DOE technique takes as input electrical simulation results of a charge pump circuit for different component geometries and different oscillator pulse periods. It produces, as outputs, polynomial equations of the charge pump output voltage HV and the consumption current ISUNK. Using those equations, impact of specific charge pump design parameters on charge pump outputs is clearly shown. Thus, design guidelines can be followed to optimize charge pump circuits efficiency. To validate this approach, this optimization methodology is used to evaluate the charge pump optimal configuration of a low voltage and low current IC circuit (RFID tag).

Keywords - charge pump, optimization, modeling, MVM.

1. Introduction

 Embedded Electrically Erasable Programmable Read Only Memory (EEPROM) is now extensively used in various applications such as radio frequency identification (RFID) tag. An RFID system is made up of a reader and a tag which must communicate together. This communication is based on a wireless write and read access to the tag EEPROM.

In passive system, the tag, shown in Figure 1, must recover power supply from the incident wave. Actually, a new demand appears on UHF RFID system which works around 915 MHz. In the USA, the norm allows an emission power of 4 Watts; this value leads to a read range around 10 meters. But the writing range is often limited to a few meters. Indeed, UHF tag is often powered with voltage around 1V, but writing in EEPROM memories require high voltage (15V-16V). That's why charge pump circuits (which convert low DC

 $¹$ A. Perez</sup>

 $¹$ J-M. Portal</sup>

 ST-Microelectronics

voltage to high voltage) are included in RFID tag designs. Charge pump circuits consumes a great part of tag available power and are very critical in terms of RFID system reliability.

During the tag EEPROM programming operations and especially during a write operation, more than 90% of the current is consumed by the charge pump [1]. During this stage, we have to provide enough current in order to maintain the required HV level. The memory part of the tag consists of a charge pump and some auxiliary circuits, including non overlapping clock generator, comparator circuits, discharge circuits and voltage dividers circuits. EEPROM programming levels are obtained from the charge pump output voltage HV. This high voltage level has to be monitored as well as possible because it is one of the main causes of EEPROM memory issues. To achieve this goal, we build a polynomial model in order to link intrinsic (transistor widths, charge capacitance…) and extrinsic charge pump parameters (clock frequency) to specific charge pump outputs like the voltage level HV or the consumption current I_{SUNK} . Thanks to this model, we will see how it is possible to improve charge pumps circuits reliability performances and guarantee robust circuit functionality.

This paper is organized as follows. Section 2 gives a short overview of high voltage generator structures and presents in details the architecture considered for simulations. In section 3, the DOE technique is detailed in order to explain the charge pump polynomial models generation. In this section, the evaluation of the charge pump outputs (HIV and I_{SINK}) as function of the charge pump critical parameters is developed. The section 4 is dedicated to the polynomial models processing. Finally, Section 5 gives some concluding remarks.

2. Charge pump simulation context

 Charge pumps are circuits that generate a voltage larger than the supply. Most high voltage generators are based on the Dickson charge pump [2]. However, as supply voltage being scaled down below 3V, the pumping efficiency of the Dickson charge pump is severely degraded. An optimized strategy for designing these circuits is proposed in [3], with an analytical model. In this model, efficient design parameters, such as number of capacitor stage, can be computed for a chosen technology. Charge pump circuit performance is affected by threshold voltage, reverse current and body effect. That's why others architectures have been developed to overcome these limitations like the NCP-2 [4] shown Figure 2.a. In this architecture, the same equations are used, but the design becomes harder because of the increase of devices.

In [5], the NCP-2 structure was then compared to another charge pump which is presented Figure 2.b. Although this architecture is far from Dickson one, this circuit generates higher output voltage than Dickson and NCP-2 charge pump.

Figure 2: (a) NCP-2 Charge pump (b) CTS charge pump stage

The complete design scheme of a charge pump circuit needs an optimization step, with global simulations which take into account of effects. Charge pump simulation is slow: a small time step is needed because the input clock's frequency. The optimization of charge pump designs with several parameters to find could take a long time, even if an approximation value is obtained for the main parameters. In this work, the impact of specific charge pump parameter variation around chosen value is evaluated. This method is presented for the CTS structure shown in Figure 2.b which currently presents the best choice for low voltage and low current IC [5] [6] such as RFID tag.

In a first approximation, we assume that the charge pump outputs (HIV and I_{SUNK}) depend mainly on the two enhanced NMOS transistors widths W_n , the two PMOS transistors widths W_p , the value of the pump capacitors C_{pump} and also the input clock period T_{osc} . These four parameters W_n , W_p , C_{pump} and the clock period T_{osc} (see Figure 2.b) are chosen as well as the charge pump critical parameters. This parameters needs to be optimized in order to get the correct output voltage HV and the smallest consumption current.

The simulation context is defined by the different elements surrounding our 10 stages CTS charge pump. In order to be as close as possible of the product working conditions, simulations are performed by including in the design the following elements (Figure 3).

- the charge pump,
- the clock driver.

Figure 3: High voltage generator circuit

Charge pump output curves, obtained for a given configuration of input parameters are shown Figure 4, after transient simulations. The first response is the HIV voltage. The second response is the consumption current which is obtained by adding the average current sunk by the clock and the average current sunk on V_{DD} . The total consumption current for a given load and a given supply voltage V_{DD} is called I_{SUNK} .

3. Charge pump outputs polynomial model

As mentioned in the introduction, a good understanding of charge pump circuits needs to be able to link intrinsic charge pump parameters (transistor widths, charge capacitance…) and extrinsic parameters (clock frequency) to specific output responses like the high voltage HV or the consumption current I_{SUNK} . To do so, any possible variation of all the 4 selected parameters with any possible value of the output voltage must be considered. It clearly appears that a classical approach based on changing one parameter at a time for all other possible parameter values is intractable in number of experiments to perform. For example, considering 100 possible values for each parameter, such a method would lead to perform $100⁴$ simulations to build a database for one output response.

To pass over this limitation, a technique based on "Design Of Experiment" (DOE) is used. Our experiments are in fact a set of simulations, thus this technique is here called "*Design Of Simulation*" (*DOS)*. DOS allows having a complete knowledge of the selected outputs (HV and I_{SUNK}) in the domain of variation of the 4 input parameters, from a limited number of simulations. This domain of variation is called sphere of knowledge. In practical terms, a Doehlert matrix [7] is selected to define all the configurations to simulate. The selected outputs are generated from a Surface Response analysis. In this approach each 4 input parameters are associated to a factor, thus 4 factors are necessary. The levels chosen for these factors, according to the Doehlert matrix, are given as follows:

- C_{pump} is affected to factor X1 with 5 levels,
- \overline{W}_n is affected to factor X2 with 7 levels,
- W_p is affected to factor X3 with 7 levels,
- $T_{\rm osc}$ is affected to factor X4 with 3 levels,

Table 1: Map of Simulations

With this information, the map of simulations is build around 21 different configurations of the input parameters as shown Table 1. Therefore, 21 ELDO simulations of the circuit are automatically performed. From the result of these simulations, a multi-regression algorithm extracts the polynomial model of each considered output response. The general form of the polynomial model is given by the following equation:

$$
P=\!\!-\!\!b\!\!+\!\!\sum_i\!\!b_i\!\cdot\! X_i\!\!+\!\!\sum_i\!\!b_{ii}\!\cdot\!\big(X_i\!\cdot\! X_i\big)\!\!+\!\!\sum_{ij}\!\!b_{ij}\!\cdot\!\big(X_i\!\cdot\! X_j\big)
$$

The confidence on the 2 equations (output voltage and consumption current) is given by the study of residuals, i.e. the difference between values obtained from the equations and those obtained from simulations. The maximal difference for HV is 0.27V and only 0.45µA for the consumption current I_{SUNK} . It is important to notice that these values are obtained from corner cases at the limit of the sphere of knowledge. They represent respectively less than 1.5% and 0.3% of error compared to the simulated values. The rectilinear normal plot, shown in Figure 5 confirms these results for the HV output.

Figure 5: Normal plot of the HV response

Figure 6 summarizes the different steps of the polynomial model generation technique. Advantages offered by the polynomial model are listed below:

- A simple polynomial expression which allows fast computation time,
- Only 21 simulations are necessary, allowing a short generation time. This property can be used to automatically fast calibrate the model to switch from one technology to another. Besides, this technique can be easily adapted to other charge pump architectures,
- The validation of the model is achieved by monitoring the accuracy of each output (study of residuals).

Figure 6: Model generation bloc diagram

Of course, we can consider the impact of other input parameters like parasitic capacitances or clock phases overlap, on the selected outputs to refine the model. It will result in an increase of the simulation number in order to cover the domain of variation of the whole input parameters. It is also possible to link other charge pump outputs to the input parameters like the charge pump power efficiency η (see Section 4). Charge pump power efficiency is defined as the ratio between the output power P_{OUT} delivered to the load and the input power P_{IN} obtained from the supply.

4. Graphical Results & discussion

When dealing with charge pump circuits, constraints as design robustness, maximum output voltage, minimal consumption current, and maximal power efficiency have to be taken into account.

Figure 7, 8 and 9 are a graphical illustration of our polynomial model outputs versus given input parameters. The domain of variation of each input parameter related to its nominal value is given in Table 2. With such a representation, the impact of each charge pump parameter can be easily evaluated by considering one output at a time as a function of two input parameters (the other parameters being set at their nominal values).

Figure 7 shows the evolution of outputs HV and I_{SINK} versus C_{pump} and T_{osc} parameters. The first information is the existence of an optimal HV value which is obtained for high time period T_{osc} (low oscillator clock

frequencies) and important C_{pump} values. From a robustness point of view, sensitivity to the given input parameters variation seems to be acceptable inside the maximal HV area. Concerning the consumption current, its minimal value is obtained for low C_{pump} values. For both HV and I_{SUNK}, we can notice that the impact of the clock frequency is relatively weak compared to the impact of the pump capacitance.

	-pump	W,		$T_{\rm osc}/2$
Nominal Values	270 fF	$3 \mu M$	$1 \mu M$	2.75 ns
	± 160 fF	\pm 1.5 µM	$\pm 0.8 \mu M$	\pm 0.28 ns
Min	190 fF	$1.5 \mu M$	$0.2 \mu M$	2.75 ns
Max	430 fF	$4.5 \mu M$	$1.8 \mu M$	2.75 ns

 $T_{\rm eff}$ $\sim 2.$ $N_{\rm eff}$ the each parameter of each parameter \sim

In Figure 8, impacts of W_p and W_n parameters are evaluated. We can see clearly that a maximal HV corresponds to minimal W_p and W_n values. Moreover, a minimal consumption current is correlated with low W_n and W_p values. For these two parameters, maximal HV and minimal I_{SUNK} values are obtained from the same parameters variation trend.

One can notice that each input parameter impacts differently HV and I_{SUNK} evolutions according to design constraints. Indeed, high values of C_{pump} lead to high HIV but also to an increase of I_{SUNK}. Thus, the power efficiency criterion is chosen to characterize charge pump circuits effectiveness. The power efficiency model is obtained by the ratio between the output power P_{OUT} delivered to the load and the input power P_{IN} obtained from the supply. P_{OUT} and P_{IN} are respectively obtained by measuring the HV output voltage and by extracting I_{SUNK} (on the supply).

The evolution of η versus C_{pump} and T_{osc} (Figure 9) gives interesting information. First, there is a maximal power efficiency peak value, corresponding to a minimal C_{pump} value and to a minimal clock frequency. Second, one can notice that this maximal point is not stable, especially regarding C_{pump} parameter. However, the 3D curve shows a robust area close to input parameters nominal values. When analyzing the impact of W_n and Wp on η, it appears clearly that these parameters have a huge impact on this output (i.e. all the power efficiency variation range is covered). Besides these two curves exhibit also an instable maxima for lower W_n and W_p values.

Figure 7: HV and I_{SUMK} outputs versus C_{pump} and T_{osc} (for W_n and W_p nominal values)

Figure 8: HV and I_{SUMK} outputs versus W_n and W_p (for T_{osc} and C_{pump} nominal values)

Figure 9: Charge pump power efficiency η (%) versus charge pump critical parameters

5. Conclusion

In this paper a charge pump model based on a DOE technique is presented. Knowing that high voltage generators circuits performances are strongly dependant on the charge pump design parameters, and input clock frequency, the original model presented here is very useful to understand the charge pump functioning. Indeed, impacts of specific design parameters on given responses as the high voltage and the consumption current are quickly evaluated. Thus, design guidelines can be followed to meet the targeted outputs. The high voltage generator model can be quickly generated for any charge pump architecture (depending on the number of input parameters) and allows fast calculation time with respect of accuracy.

In this modeling methodology only four charge pump parameters have been taken into account. The next step will evaluate charge pump outputs for an exhaustive list of input parameters, including power supply variations or output charge variation. The goal is to try to obtain a global charge pump model.

6. Reference

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