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Pulse Design Method for Complexity Reduction of IEEE IR-UWB Pulse Synthesizers

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***Abstract*— This paper presents a sample & hold pulse envelope synthesis method and shows that only 5 (resp. 7) samples are necessary to respect the sidelobes rejection in adjacent channels of 18dB (resp. 20dB) required by the IEEE 802.15.4 (resp. 802.15.6) standard if a sample & hold Gaussian envelope is used. These required numbers of samples, which enable complexity reduction of IR-UWB emitters for IEEE standards, are validated using measurement results of a pulse synthesizer presented in this paper since a sidelobes rejection in adjacent channels of 21.8dB (resp. 21.4dB) is obtained when transmitting in the mandatory low band of the IEEE 802.15.4 (resp. 802.15.6) standard.**

Keywords— IEEE 802.15.4 standard, IEEE 802.15.6 standard, Impulse-Radio Ultra-WideBand, pulse shaping, pulse synthesizer

I. Introduction

Since the frequency band between 3.1GHz and 10.6GHz has been allocated to Ultra-WideBand (UWB) applications by the Federal Communication Commission (FCC) in 2002, several standards using this frequency band have been defined. Among them, two IEEE standards, the IEEE 802.15.4 standard introduced in 2011 and the IEEE 802.15.6 introduced in 2012, have chosen Impulse Radio (IR) to exploit this UWB frequency band instead of usual carrier modulations.

As for usual carrier modulations, a modulated IR-UWB signal must be compliant with a frequency mask. Considering the case of impulse modulations, it has been demonstrated that the emitted Power Spectrum Density (PSD) is directly proportional to the square modulus of the emitted pulse's spectrum [1]. Thus, one way to ensure this compliance is to use pulses with a spectrum which fits into the targeted frequency mask. For this reason, several particular pulses with no sidelobe have been defined for IR-UWB applications such as the ideal up-converted Gaussian pulse [2].

However, when pulses use the entire FCC frequency band, the antenna can mitigate constraints on sidelobes rejection since its frequency response generally fits with the FCC mask. Nevertheless, when considering IEEE standards, sidelobes rejection in adjacent channels is one of the more difficult issues to solve since the expected rejection is 18dB (resp. 20dB) for the IEEE 802.15.4 (resp. 802.15.6) and the adjacent channels are in the unfiltered part of the antenna frequency band.

Several pulse shaping methods have been introduced to limit sidelobe rejection issues. In the analog domain, pulse can be shaped by using modulated inverters or class C drivers as antenna driver [3]. In digital domain, this can be done by enabling parallel antenna drivers [4]. However, impairments such as Process, Voltage, and Temperature (PVT) variations can modify the shape of the emitted pulse, leading to the raise of the sidelobes in adjacent channels. To counterbalance for impairments, the pulse shape might be finely tuned as it can be easily done with digital shaping methods [5][6]. However, the more the degrees of freedom an IR-UWB emitter has, the more complex it is, which unfortunately increases its area and power consumption.

In order to relax architecture complexity and design constraints, it is firstly shown in this paper that how the sidelobes rejection in adjacent channels required by the IEEE 802.15.4 (resp. 802.15.6) standard can be fulfilled with pulses shaped by a sample & hold Gaussian envelope with 5 (resp. 7) samples only. In a second time, a pulse synthesizer allowing the generation of pulses shaped by a sample & hold Gaussian envelope having 5 or 7 samples and their tuning is presented. Finally, measurement results of the pulse synthesizer are used to validate in practice the approach developed in this paper.

The paper is organized as follows. Section II details the synthesis of sample & hold Gaussian envelope. Next, the design of an UWB pulse synthesizer able to deal with this type of envelope is described in Section III. Finally, measurement results are shown and discussed in section IV.

II. Sample & Hold Gaussian Envelope Synthesis

A way to ensure that a modulated IR-UWB signal is compliant with a frequency mask is to use pulses having a spectrum which can easily fit into this mask such as the up-converted Gaussian pulse. The up-converted Gaussian pulse $p_G(t)$ can be defined as follows:

$$p_G(t) = e_G(t) \cdot \sin(2\pi f_M t) \tag{1}$$

where the envelope $e_G(t)$ is the well-known Gaussian function which is here up-converted to the frequency f_M (central frequency of the targeted frequency band). In this case, $e_G(t)$ is a function of the form:

$$e_G(t) = A\exp(-\beta t^2) \tag{2}$$

where A is the maximum of the Gaussian function and β a parameter which can be linked to the $p_G(t)$ bandwidth BW_{-XdB} defined at X dB as follows [2]:

$$\beta = \left(\pi^2 BW_{-XdB}^2\right) \Big/ \left(2\ln\left[10^{XdB/10}\right]\right). \tag{3}$$

Since the Fourier transform of a Gaussian is a Gaussian, the main advantage of this ideal pulse $p_G(t)$ is that its spectrum is a Gaussian centred on f_M and also do not have sidelobes as shown in Fig. 1.

However, an up-converted Gaussian pulse has an infinite duration and also has to be truncated in practice according to a certain percentage of A. This truncated up-converted Gaussian pulse noted $p_{TG}(t)$ can be defined as follows:

$$p_{TG}(t) = e_{TG}(t) \cdot \sin(2\pi f_M t) \quad (4)$$

where the envelope $e_{TG}(t)$ is the truncated Gaussian which is a function of the form:

$$e_{TG}(t) = e_G(t) \cdot \Pi_T(t) \quad (5)$$

with $\Pi_T(t)$, the gate function equals to 1 for t between $-T/2$ and $T/2$ and 0 outside. Unfortunately, sidelobes occur due to this truncation as shown in Fig. 1 and the more truncated the Gaussian is, the higher the sidelobes are. The truncation percentage must also be moderated.

To allow pulses with finite time envelope, such as the truncated up-converted Gaussian pulse, to be generated using a digital approach, it is proposed to discretise this envelope using K samples having a duration τ. Thus, the sample duration must be equal to:

$$\tau = D / f_M \quad (6)$$

where D is an integer chosen to make τ a multiple of the sine period and also to be able to clock the pulse envelope generator with an oscillator working at f_M. In this case, the number of samples K is given by:

$$K = T / \tau \quad (7)$$

where K can be an integer if:

$$T = N / f_M \quad (8)$$

and if N is an integer equal to the product of K by D (T being the $e_{TG}(t)$ duration and also the $p_{TG}(t)$ duration). In the case of a truncated Gaussian envelope, this condition is fulfilled when particular percentages of A are used for truncation.

Considering these assumptions, the discretised truncated up-converted Gaussian pulses $p_{DTG}(t)$ can be defined as follows:

$$p_{DTG}(t) = e_{DTG}(t) \cdot \sin(2\pi f_M t) \quad (9)$$

where the discretised truncated Gaussian $e_{DTG}(t)$ is equal to:

$$e_{DTG}(t) = \sum_{k=0}^{K-1} e_{TG}\left(k\tau - \frac{K-1}{2}\tau\right) \cdot \Pi_\tau\left(t - k\tau + \frac{K-1}{2}\tau\right). \quad (10)$$

This approach can be extended to any envelope $e(t)$ with a finite duration by replacing $e_{TG}(t)$ with $e(t)$. However, this discretisation leads to sidelobes increase as shown in Fig. 2 and Fig. 3 and the lower K is, the higher sidelobes are.

Nevertheless, it can be demonstrated that it is possible to use a sample & hold envelope while limiting sidelobes magnitude if K and D are chosen according to the following inequality:

$$\tau \leq 1/q \cdot BW_{-XdB} \quad (11)$$

where q is a parameter which can be numerically computed and depends on the targeted rejection of sidelobes X in dB and the $e(t)$ Fourier transform.

Finally, as shown in Fig. 2 (resp. Fig. 3), a pulse having a sample & hold Gaussian envelope with only 5 (resp. 7) samples can be compliant with the frequency mask of the mandatory low band channel C3 (resp. C1) defined in the IEEE 802.15.4 HRP UWB PHY (resp. 802.15.6 UWB PHY) regarding sidelobes rejection in adjacent channels between 3.1GHz and 10.6GHz. However, as shown in Fig. 2, other sidelobes, which must not be confused with sidelobes in adjacent channels circled in green, can be observed between 0.91GHz and 1.61GHz which is not compliant with FCC regulation. Nevertheless, AC coupling and filtering due to antenna will reduce enough these sidelobes since it is reasonable to consider that the antenna frequency response fits into the FCC mask.

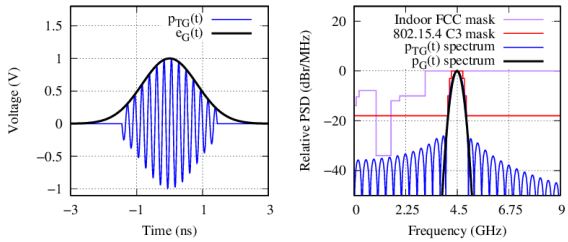


Fig. 1. Up-converted Gaussian pulse truncated at 22% and compliant with the channel 3 frequency mask of the IEEE 802.15.4 standard.

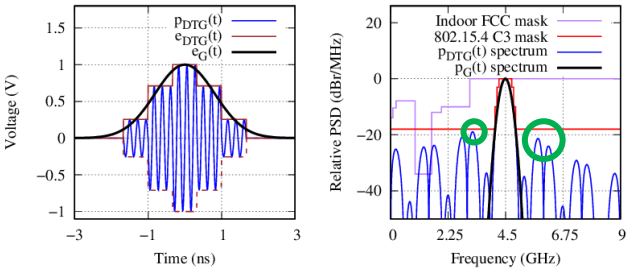


Fig. 2. Example of a pulse with sample & hold Gaussian envelope compliant with the channel 3 of the IEEE 802.15.4 standard (K = 5, D = 3 ; the highest sidelobes in adjacent channels are circled in green).

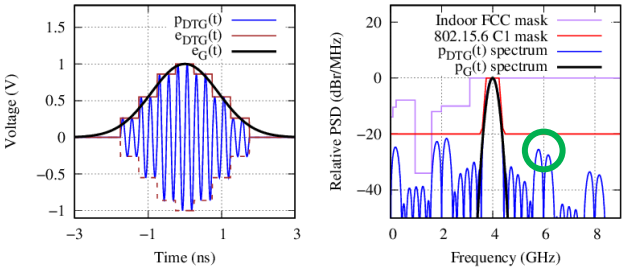


Fig. 3. Example of a pulse with sample & hold Gaussian envelope compliant with the channel 1 of the IEEE 802.15.6 standard (K = 7, D = 2 ; the highest sidelobes in adjacent channels are circled in green).

III. Design of the Associated Pulse Synthesizer

A. Pulse synthesizer architecture

The topology of the pulse synthesizer associated to the pulse design method is based on a H-bridge. Although a H-bridge has been already proposed for pulse shaping in UWB applications [2], the presented structure has been modified to allow a digitally control of the pulse envelope. In addition, the H-bridge is here driven by a differential Voltage Controlled ring Oscillator (VCO; detailed in [7]) as shown in Fig. 4.a (instead of a Voltage Controlled Delay Line such as in [2]) in order to allow the generation of high duration pulses as required by the IEEE standards. The VCO also controls alternatively the transmission gates couples (TGU1, TGD1) and (TGU2, TGD2) to alternate the current into the load which produces zero mean pulses. Thus, as represented in Fig. 4.a, the pulse envelope is controlled thanks to 4 transmission gates banks TGx (TG1 to TG4) which modify the current into the output load. Signals Sx (S1 to S4),

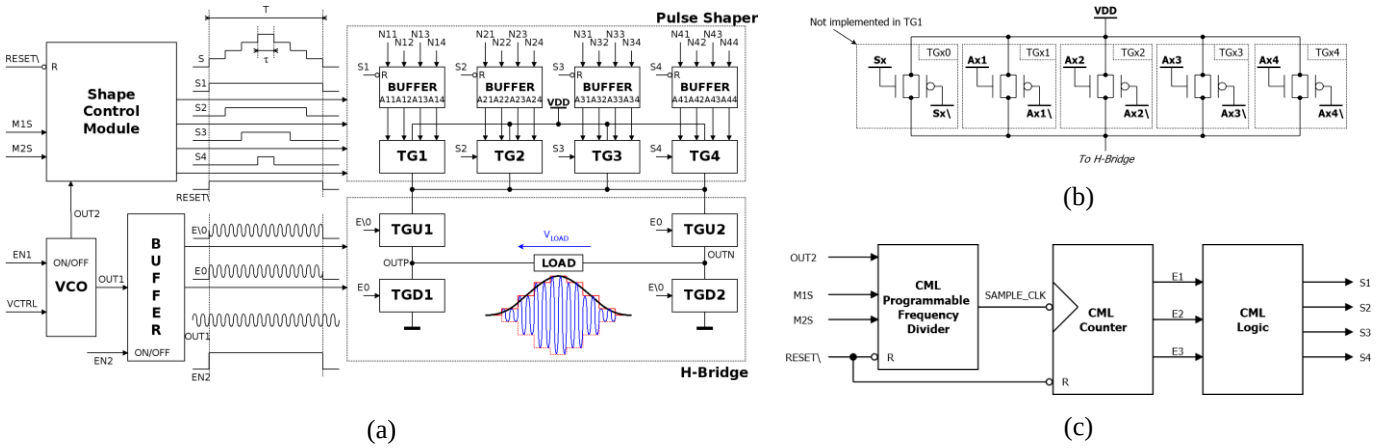


Fig. 4. Architecture of the pulse synthsizer (a), the transmission gates bank (b), the shape control module (c).

provided by the shape control module, control the transmission gates banks TGx and their associated buffers. As shown in Fig. 4.a, this allows a pulse having a sample & hold envelope with a maximum of 7 samples to be generated. Finally, the magnitude of samples is controlled at the transmission gates bank (TGx) level by 4 control bits (Nxy). Indeed, when Sx activates a buffer, the control bits Nxy (Nx1 to Nx4) are applied to the TGxy (TGx1 to TGx4) gates that composed the TGx as presented in Fig. 4.a.

B. Design of the pulse shaper

The pulse shaper is mainly composed of 4 banks of transmission gates (TGx) and each transmission gates bank is based on 5 parallel transmission gates (TGxy) as shown in Fig. 4.b. The voltage level of envelope samples is also controlled by changing the number of active TGxy which modifies the amount of current flowing through the output load. Since the current driven by one transmission gate depends on the width of the transmission gate transistors, the transmission gates have been sized to achieve levels which are distributed around the ones required by the sample & hold Gaussian envelope compliant with IEEE standards, considering that when the x^{th} TGx is activated, all other previous ones (i.e. all TGx from 0 to x-1) are also activated. It is worth to mention that the smallest transmission gate TGx0 of each TGx is directly controlled by Sx to tune the samples level around its nominal value. However, TG10 is not implemented in order to completely disable TG1 which allows the generation of pulses having an envelope with K=5 or 7 samples.

C. Design of the shape control module

To synchronize the pulse shaper with the H-Bridge, the same VCO is used to clock the H-bridge and the shape control module. However, to maintain a constant bandwidth over the different channels, the time duration of the envelope must be constant whatever the VCO oscillation frequency (f_M) is. To this end, the shape control module shown in Fig. 4.c is in charge of tuning the samples duration which is determined by two consecutive edges of the control signals Sx and Sx+1 as represented in Fig. 5. Thus, a programmable frequency divider driven by the VCO has been designed to generate a clock (SAMPLE_CLK in Fig. 4.c) having a period equal to D/f_M with $D \in [2,3,4,5]$. The value of D is then set by the couple of bits MzS. Considering a given channel mask, D can be set to 2 for the lowest channels which leads to a sample duration of $2/f_M$ whereas for the highest channels, D is set to 5 which leads to a sample duration of $5/f_M$. To address larger bandwidth, it is also possible to set D to a low value while using a high f_M. Finally, the outputs (Ei in Fig. 4.c of the counter (CML Counter in Fig. 4.c) clocked by the SAMPLE_CLK signal are used to generate the control signals Sx with conventional logic gates. However, only Current Mode Logic (CML) gates are used in the shape control module since the CML gates can operate at higher frequencies than the CMOS ones.

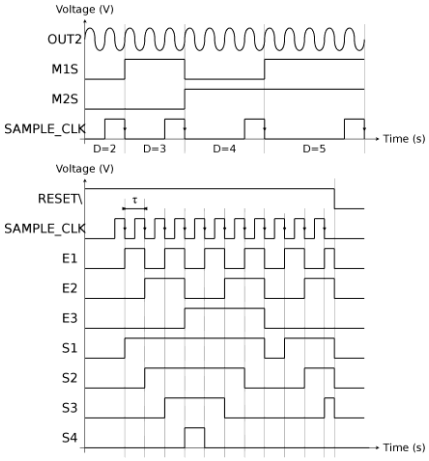


Fig. 5. Chronograms of the shape control module.

IV. Measurements Results

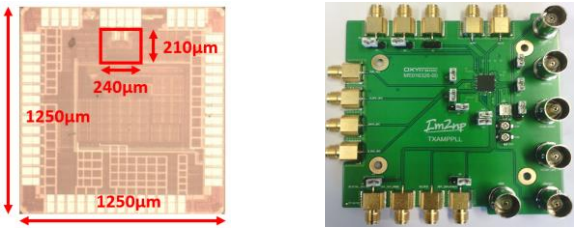
The proposed programmable digital pulse synthesizer has been implemented using a 65nm technology from ST Microelectronics and a supply voltage of 1.2V. As shown in Fig. 6.a, the manufactured chip, which is pad limited, has a die area of 1.56mm² but a core area of 0.05mm² since it uses only MOS transistors and since others functions not discussed in this paper have been implemented such as a Phase-Locked Loop (PLL) to control the built-in VCO. Moreover, a Serial Peripheral Interface (SPI) slave has been added to make easier the set of Nxy (resp. MzS) bits which control the envelope samples magnitude (resp. duration). Finally, as shown in Fig. 6.b, the test chip has been soldered on a dedicated Printed Circuit Board (PCB) for measurement purposes.

To validate the use of a sample & hold Gaussian envelope with only 5 or 7 samples for pulse generation having sidelobes rejection compliant with IEEE standards (18dB for IEEE 802.15.4 and 20dB for IEEE 802.15.6), pulses for the mandatory channel in low band of each standard (C3 for IEEE 802.15.4 and C1 for IEEE 802.15.6) has been measured and are shown in Fig. 7 and Fig. 8. They

have been obtained by varying Nxy and MzS around the initial values obtained using the ideal pulse introduced in section II. This has led to 802.15.4 (resp. 802.15.6) compliant pulses regarding the sidelobes rejection in adjacent channels with a peak-to-peak voltage of 0.71V (resp. 0.76V) and a sidelobes rejection of 21.8dB (resp. 21.4dB), which leads to an emitted energy of 1.22pJ (resp. 1.72pJ) on a 2x50Ω load whereas the measured power consumption is 1.9nJ/pulse. Performances of the proposed pulse synthesizer are summarized in Tab. I and compared with state-of-the-art works. From the authors knowledge, it appears that it is the first time than pulses shaped by a sample & hold envelope with only 5 samples have been used to respect sidelobes rejection in adjacent channels required by the 802.15.4 standard, which will pave the way to less complex UWB emitters. Finally, to highlight the ability of the presented pulse synthesizer to shape the pulse envelope and also its spectrum, the shorter (resp. longer) envelope measured for *K*=5 and *D*=2 (resp. *K*=7 and *D*=5) is shown in Fig. 9.a (resp. Fig. 9.b) and shows a sidelobes rejection in adjacent channels higher or equal to 20dB.

V. Conclusion

In this paper, a sample & hold pulse envelope synthesis method has been introduced and shows that only 5 (resp. 7) samples are necessary to respect sidelobes rejection in adjacent channels required by the IEEE 802.15.4 (resp. 802.15.6) standard. Next, this has been validated using measurement results of a pulse synthesizer implemented with a 65nm CMOS technology from ST-Microelectronics. Authors hope that this work will pave the way to less complex UWB emitters and also reduce their area and power consumption.



(a) (b)

Fig. 6. Test chip photo (a) and test PCB photo (b).

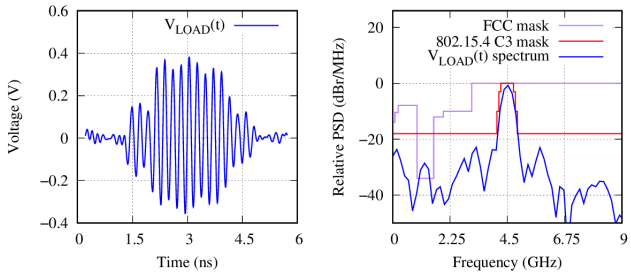


Fig. 7. Pulse for the channel 3 of the IEEE 802.15.4 standard (mandatory).

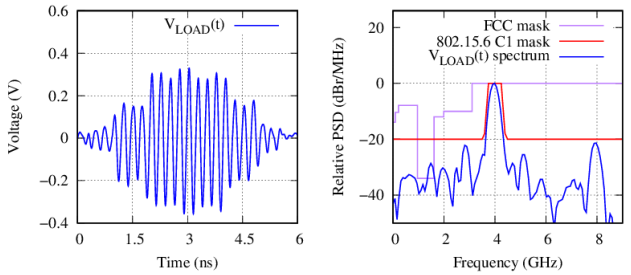
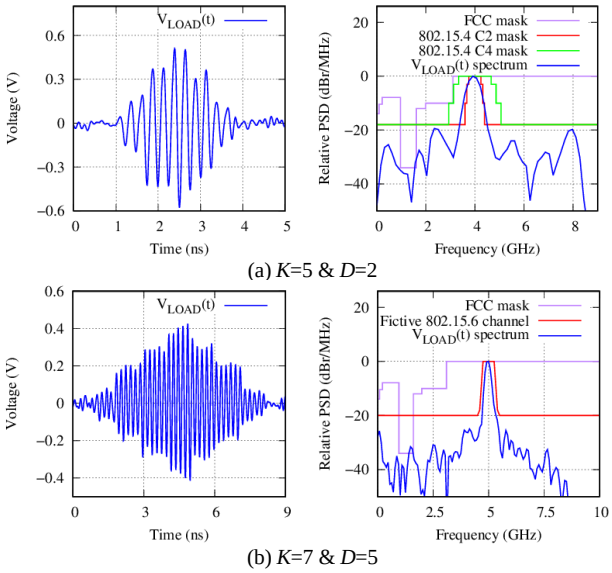


Fig. 8. Pulse for the channel 1 of the IEEE 802.15.6 standard (mandatory).

TABLE I. State of the art comparison

	This Work	[3]	[4]	[5]	[6]
Techno.	65nm	130nm	90nm	130nm	28nm FDSOI
IEEE Standards	15.4 / 15.6	No	15.4	No	15.4
Vpp (V)	0.71 / 0.76	0.5	0.71	0.94	0.35
Sidelobe reject. (dB)	21.8 / 21.4	20	20.7	24	25
PRF (pulse/s)	15.6M	5M	15,6M	10M	27.24M
Ep (pJ)	1.22 / 1.72	1.3	2.5	3.6	0.64
Fine tuning	yes	no	yes	yes	yes
Number of envelope samples	5 / 7	NA	7	7	9 or 18
Pcons@<PRF>[a] (W@Hz)	600/700µ @1M	5.7µ@ 50k	4.36m@ 7,8M	379µ@ 10M	380µ@ 13,62M

[a] Mean Pulse Repetition Frequency (<PRF>)



(a) *K*=5 & *D*=2

(b) *K*=7 & *D*=5

Fig. 9. Example of pulses with the shorter (a) and the longer (b) envelope having a sidelobes rejection higher or equal to 20dB.

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