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# Repetitive short circuit capability of SiC MOSFET at specific low gate-source voltage bias for more robust extreme operation

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**Abstract** –This paper presents short-circuit (SC) performance of a commercial silicon-carbide (SiC) MOSFET device under repetitive SC stress at high drain source voltage. Two protocols are investigated to evaluate the impact of gate-source voltage ( $V_{GS}$ ) depolarization and SC duration ( $T_{SC}$ ) reduction. The  $V_{GS}$  depolarisation provides a power density reduction and allows to preserve a secure failure mode (FTO: Fail To Open) with an increase of the short circuit duration  $T_{SCmax}$ . The results demonstrate that SiC MOSFET  $V_{GS}$  depolarization does not reduce SC cycling capability at  $T_{SCmax}$ . However, using  $V_{GS}$  depolarization allows to get performance close to IGBT robustness levels with almost 1000 cycles @ $T_{SC}=10\mu s$ . The simulation of the chip temperature evolution during SC tests suggests that the degradations stay attributed to the increase of junction temperature ( $T_j$ ) during the SC cycles, which leads to the fusion of the top Al inducing cracks into the thick oxide.

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## 1. Introduction

After years of research on device physics and manufacturing technology, silicon-carbide (SiC) power semiconductor devices have become key devices for future power electronics applications, e.g., railway traction, electric vehicles, and power grids [1]. The SiC thermal and physical properties make this material more attractive that can far exceed the performance of Si counterparts (i.e. high electric field strength, thermal conductivity and electron velocity) [2].

SiC MOSFETs have been commercialized since 2011 and show promising performance when considering static losses, fast switching, high voltage and high temperature operations in power conversion applications [3]. However, the long term reliability of these devices has not been fully established especially the reliability under abnormal operating conditions, such as short-circuit (SC) [4-5]. Various studies have reported that silicon-based devices have proven to be more reliable than SiC MOSFETs, under SC conditions due to higher current density and the thinner gate oxide of SiC MOSFETs [6-7]. According to the literature, two main failure mechanisms under single-event SC stress have been observed until now [4-8]: thermal runaway and gate oxide damage. The first mechanism is induced by extreme heat build-up in depletion regions within a short time period, leading to a drain-to-source holes generation and BJT triggering visible by a drain - source breakdown. The second mechanism is characterized by structural damage (e.g. crack) in the gate structure leading to a gate-to-source breakdown and the appearance of permanent gate leakage current [9].

Furthermore, it has been reported that the failure mechanism is highly related to the dissipated power density [10]. This power density could be impacted by many parameters such as the gate-source voltage, DC-link voltage, pulse time duration and junction temperature of the device [11]. SiC MOSFETs have to face different faults during it lifetime. Hence, the interest in performing repetitive SC test that enhances the different failure mechanisms and also provides more insight about the

degradation process. Hence, the interests in performing repetitive SC tests reflecting the influence of a single SC event and also providing more valuable insights about the degradation process [12].

In this context, the aim of this paper is to analyze the effect of gate-source voltage depolarization and pulse time duration on the electrical performance of a discrete SiC MOSFETs under repetitive SC stress. Various aging indicators are used to evaluate the robustness of SiC MOSFETs under repetitive SC stress: gate leakage current ( $I_{GSS}$ ) and drain source current ( $I_{DS}$ ). The thermal behavior during repetitive SC test is evaluated using 1D electro-thermal-metallurgical model simulation. The paper is organized as follows: section II presents the device under test and the SC test setup. In section III, the results of the repetitive SC tests are discussed. Electro-thermal-metallurgical model simulation is presented in section IV.

## 2. Experimental setup

The devices under test are commercially available 2<sup>nd</sup> generation planar SiC MOSFETs rated at 1200V/36A (ref. C2M0080120D), manufactured by CREE [13] and packaged in TO247 case. The experiments are carried out on the bench describe in Fig. 1 [14]. This bench provides an interface allowing users to set various SC test conditions such as various drain-source voltage ( $V_{DS}$ ), gate-source voltage ( $V_{GS}$ ), and short circuit duration ( $T_{SC}$ ) values. The SC test is conducted with series of SC cycles frames with a dead time of 3s avoiding the average overheating of the chip and allowing a threshold voltage ( $V_{GSTH}$ ) stabilization. For each last cycle of the SC test frame,  $V_{DS}$ ,  $V_{GS}$ , buffer voltage ( $V_{BUFFER}$ ),  $I_{GSS}$   $I_{DS}$  waveforms are recorded. The repetitive SC test is stopped when  $V_{GS}$  drops around 15% showing clear gate damage.

## 3. Device capability under repetitive SC stress

Repetitive SC tests have been performed at room temperature under two protocols. The first protocol aims at studying the effect of  $V_{GS}$  on the robustness of SiC MOSFETs

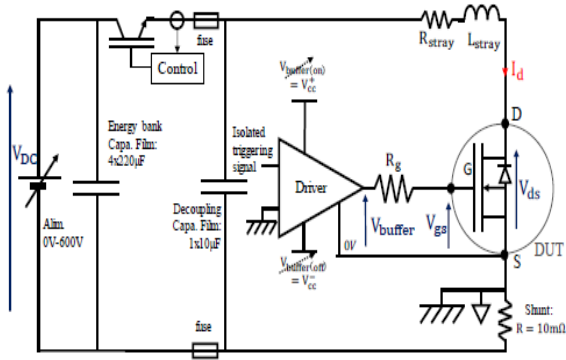


Fig. 1. Schematic of Type 1 short-circuit test [14]

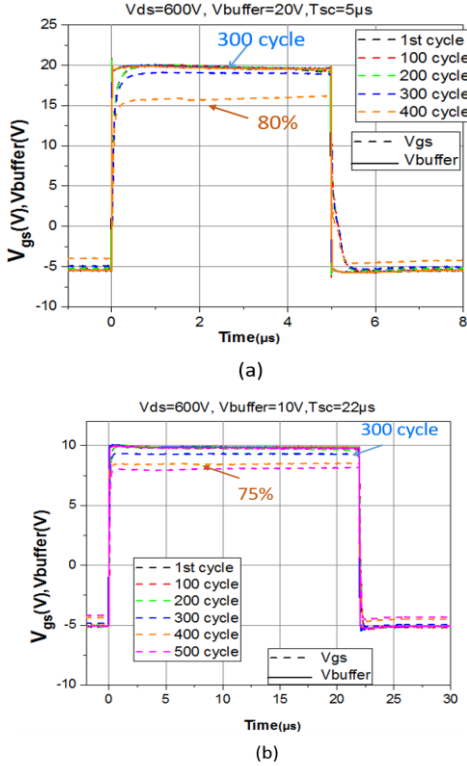


Fig. 2. Experimental waveforms of  $V_{BUFFER}$  and  $V_{GS}$  under  $V_{DS}=600V$  and  $T_{CASE}=25^{\circ}C$  for: (a) DUT#1 and (b) DUT#2.

under repetitive SC test. The second protocol is conducted to evaluate the impact of reducing  $T_{SC}$  on the robustness of SiC MOSFETs under repetitive short-circuit.

### 3.1. First protocol

For the first protocol, repetitive SC tests are conducted on two DUTs at  $V_{DC}=600V$  and  $T_{SCmax}=1\mu s$ .  $T_{SCmax}$  is the maximum pulse duration before the device failure under single-event SC test. For two fresh devices,  $T_{SCmax}$  was experimentally investigated for 2 values of  $V_{GS}$ :  $V_{GS}=20V$  and  $V_{GS}=10V$ , which leads to preserve a secure failure mode (FTO) approved by the authors [15]. It has been found that  $T_{SCmax}=6\mu s$  and  $T_{SCmax}=23\mu s$  for  $V_{GS}=20V$  and  $V_{GS}=10V$  respectively. These

results are used to select the suitable testing conditions for the

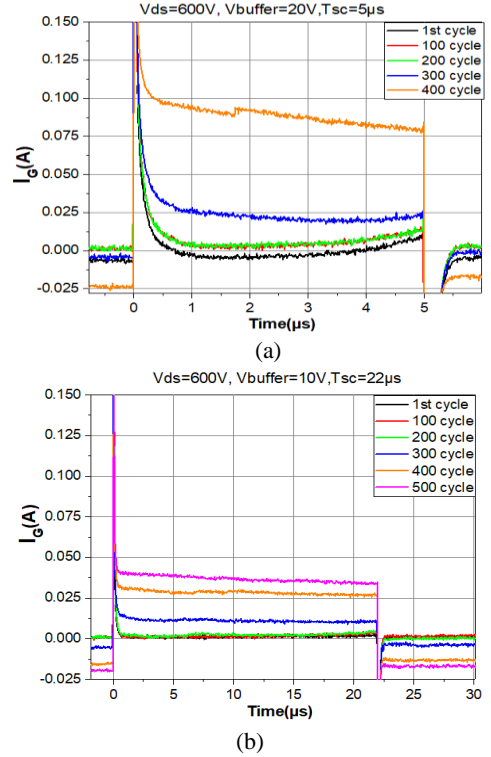


Fig. 3. Experimental waveforms of  $I_G$  under  $V_{DS}=600V$  and  $T_{CASE}=25^{\circ}C$  for: (a) DUT#1 and (b) DUT#2.

repetitive aging SC tests. Several tests have been led and for this study, gate-source polarization and SC duration are fixed at  $V_{GS}=20V$ ,  $T_{SC}=5\mu s$  for DUT#1 and  $V_{GS}=10V$ ,  $T_{SC}=22\mu s$  for DUT#2, where these operation conditions show an important gate leakage current before failure. Fig. 2 depicts the  $V_{BUFFER}$  and  $V_{GS}$  waveforms for repetitive SC tests on DUT#1 and DUT#2.

The SC tests show that devices DUT#1 and DUT#2 exhibit similar degradations at various  $V_{GS}$  biases. For both devices,  $V_{GS}$  drop can be observed starting from 300 SC cycles after delayed gate-crack at turn-off, excepted for DUT#1 at end cycling. This shift becomes more significant at 400 cycles (@ 80% of DUT#1 and @ 75% of DUT#2). The  $V_{GS}$  decrease is due to an increase of permanent  $I_{GSS}$  which becomes more important as the number of SC cycles increases, as illustrated in Fig. 3. The resulting leakage current is due to occurrence of cracks, and diffusion of metal (aluminium, Al) through interlayer dielectric (ILD) region leading to the partial shorting of the gate and source terminals. A thermal modelling and simulation of the chip temperature will be performed in section 3 in order to support this hypothesis. Fig. 4 shows a reduction of  $I_{DS}$  as the number of repeated SC increases, especially after 300 cycles, which is in agreement with the decreasing of  $V_{GS}$ . It can be noticed for each cycle that at the beginning of the gate pulse,  $I_{DS}$  rises rapidly to a peak value then it keeps decreasing during the stress time due to the increase of junction temperature. By comparing the

variations of  $V_{GS}$ ,  $I_G$  and  $I_{DS}$  of the DUT#1 and DUT#2, it can be noticed that the two devices present the same shifts from the same number of cycles whereas the power density is

cycle. For the two stressed devices (DUT#1 and DUT#2), a decrease in the dissipated power density and the critical energy ( $E_C$ ) can be noticed between the first cycle and last cycle. The DUT#1 has a higher dissipated power density compared to

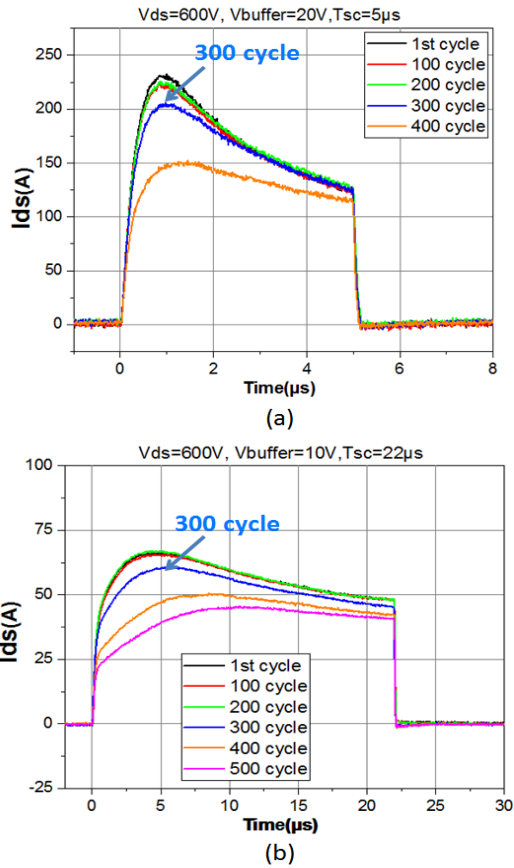


Fig. 4. Experimental waveforms of  $I_{DS}$  under  $V_{DS}=600V$  and  $T_{CASE}=25^{\circ}C$  for: (a) DUT#1 and (b) DUT#2.

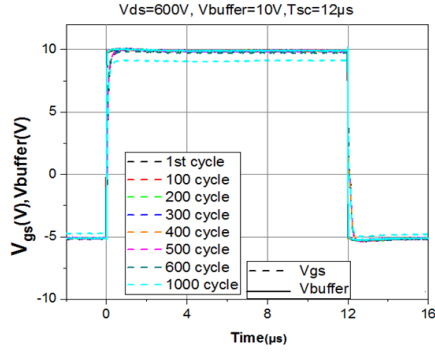
Table 1. Summary of dissipated power and critical energy of DUT#1 and DUT#2 at the first and last cycle.

	DUT#1	DUT#2
	( $V_{GS}=20V, T_{sc}=5\mu s$ )	( $V_{GS}=10V, T_{sc}=22\mu s$ )
<b>Dissipated power (W/mm<sup>2</sup>)</b>	9633 (First cycle)	3234 (First cycle)
	6769 (400 cycles)	2314 (500 cycles)
<b>Critical Energy <math>E_C</math> (J)</b>	0.501 (First cycle)	0.740 (First cycle)
	0.352 (400 cycles)	0.530 (500 cycles)

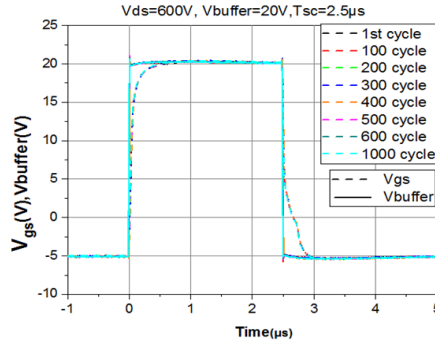
2.9 kW/mm<sup>2</sup> for DUT#1 and 0.9 kW/mm for DUT#2 (Table 1).

However, the degradations are emphasized for the DUT#1, at end of cycling more than 300 cycles with gate-crack during pulse, which is subjected to a higher gate polarization ( $V_{GS}=20V$ ) and a power density 3 times higher than DUT#2. It can be concluded that the  $V_{GS}$  depolarization and the low power density applied do not have a direct and great beneficial impact on the number of cycles at which degradation appears considering each  $T_{SCmax}$  value in the two cases.

Table 1 presents a summary of dissipated power and critical energy of DUT#1 and DUT#2 after the first cycle and the last

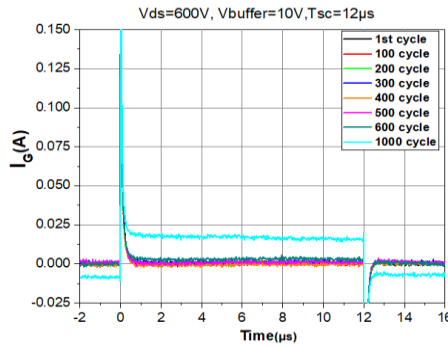


(a)

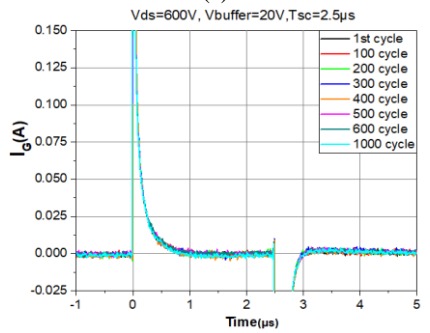


(b)

Fig. 5. Experimental waveforms of  $V_{BUFFER}$  and  $V_{GS}$  under  $V_{DS}=600V$  and  $T_{CASE}=25^{\circ}C$  for: (a) DUT#3 and (b) DUT#4.

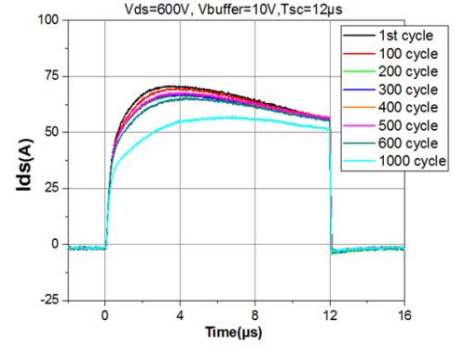


(a)

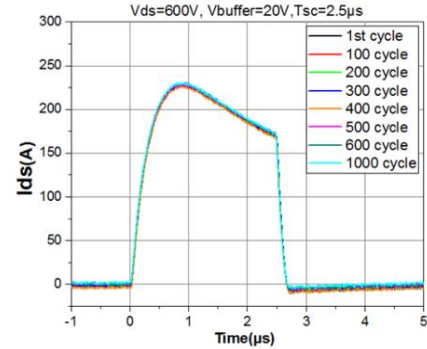


(b)

Fig. 6. Experimental waveforms of  $I_G$  under  $V_{DS}=600V$  and  $T_{CASE}=25^{\circ}C$  for: (a) DUT#3 and (b) DUT#4.



(a)



(b)

Fig. 7. Experimental waveforms of  $I_{DS}$  under  $V_{GS}=600V$  and  $T_{CASE}=25^{\circ}C$  for: (a) DUT#3 and (b) DUT#4.

Table 2. Summary of dissipated power and critical energy of DUT#3 and DUT#4 at the first and last cycle.

	DUT#3	DUT#4
	( $V_{GS}=10V, T_{sc}=12\mu s$ )	( $V_{GS}=20V, T_{sc}=2.5\mu s$ )
<b>Dissipated power (<math>W/mm^2</math>)</b>	3632 (#1 cycle)	11165 (#1 cycle)
	2966 (#1000 cycles)	11338 (#1000 cycles)
<b>Critical Energy <math>E_c</math> (J)</b>	0.453 (#1 cycle)	0.290 (#1 cycle)
	0.370 (#1000 cycles)	0.294 (#1000 cycles)

DUT#2, because the  $V_{GS}$  applied on DUT#1 is twice higher than the one applied on DUT#2. However, DUT#2 has a higher critical energy  $E_c$  since its SC duration  $T_{SC}$  is longer.

### 3.2. Second protocol

For the second protocol, repetitive SC aging stress is performed at  $T_{SC} = (T_{SCmax} - 1\mu s) / 2$  which presents typically the maximum duration, for designer, in order to ensure the gate-driver protection. The SC stress is conducted at room temperature on two devices, DUT#3 and DUT#4, with  $V_{DS}=600V$ .  $V_{GS}$  and the  $T_{SC}$  are fixed at (10V, 12 $\mu s$ ) and (20V, 2.5 $\mu s$ ) for DUT#3 and DUT#4 respectively.

Fig.5 presents the experimental waveforms of  $V_{BUFFER}$  and  $V_{GS}$  of DUT#3 and DUT#4. It can be noticed that  $V_{GS}$  is stable for DUT#4. However, the DUT3 shows a slight decrease of  $V_{GS}$  at 600 cycles due to the increase of permanent gate leakage current as shown in Fig. 6. The drop of  $V_{GS}$  and the increase of

$I_G$  is in correlation with the decrease of  $I_{DS}$  as shown in Fig. 7.

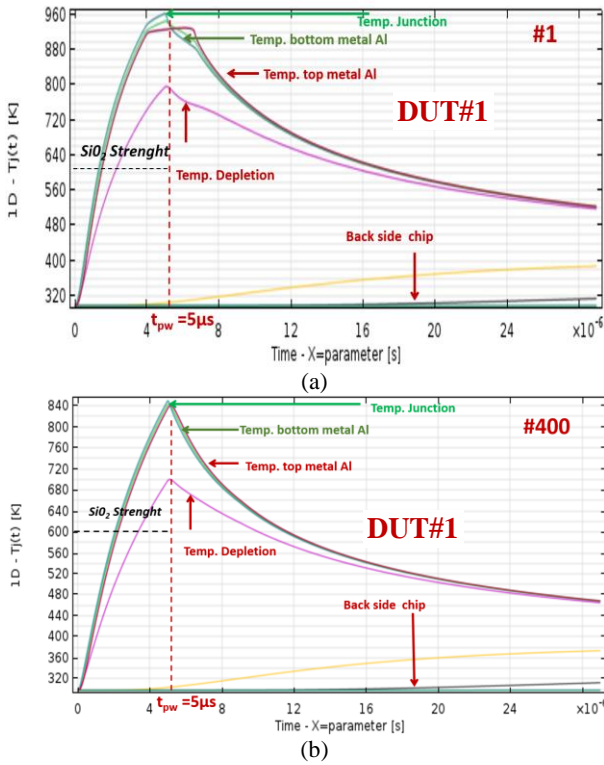


Fig. 8. Estimated temperatures of the main chip layers under Comsol for the DUT#1 at  $V_{DS}=600V$ ,  $V_{GS}=20V$  and  $T_{CASE}=25^{\circ}C$ : (a) first cycle and (b) last cycle (#400).

Table 2. summarizes the results of dissipated power density and critical energy of DUT#3 and DUT#4 after the first cycle and the last cycle (1000 cycles). Table 2 shows a decrease in the dissipated power and the critical energy ( $E_C$ ) for the DUT#3 at 1000 cycles. Therefore, for DUT#4, the critical energy is stable and a small variation of the dissipated power is noticed between the first cycle and the last cycle (1000 cycles). It can be noted that gate depolarization allows the SiC devices to approach IGBT robustness levels with 1000 cycles @  $10\mu s$  “Hard-Switch Fault” (HSF), which is not possible at its nominal gate polarization.

#### 4. Electro-thermal-metallurgical model simulation

##### 4.1. High $V_{GS}$ polarization Effect

The electro-thermal-metallurgical model developed in [16] is used to simulate the thermal behavior of studied devices under repetitive short-circuit test. This model considers the temperature dependency of thermal conductivity and mass heat of the SiC and Al metal, as well; the solid-liquid phase transition of the upper Al layer. Using Comsol<sup>TM</sup> software,  $I_{DS}(t)$  is used as input data with a constant  $V_{DS}$  value of 600 V. However, this model does not take into account the structural damage of the metal-oxide region in the thermal simulation between the first cycle and the last cycle. It is our belief that the decoupling is acceptable in this respect because the cracks in the oxide are very

small size compared to the geometries of a cellular region. Fig. 8 presents the temperature of the main chip layers during the short circuit time, for the first and last cycle using DUT#1

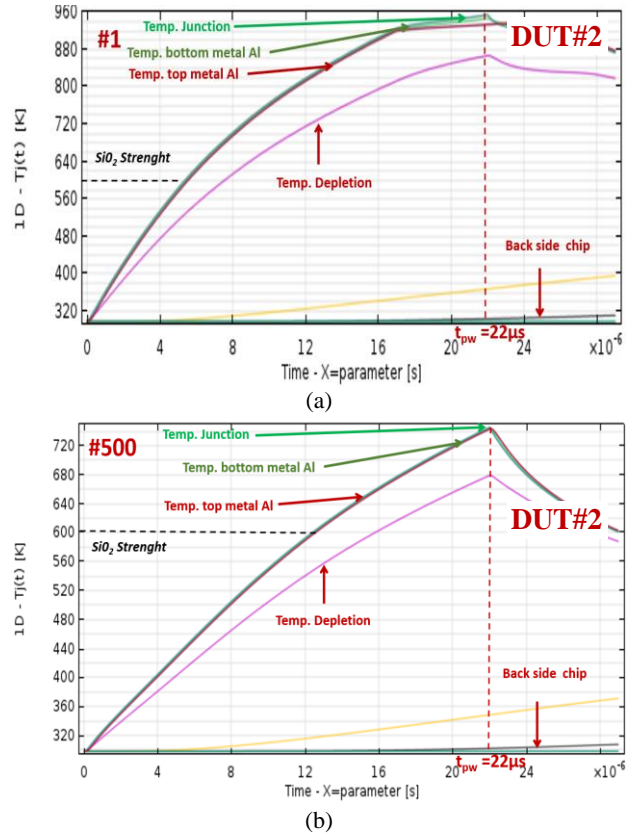


Fig. 9. Estimated temperature of the main chip layers under Comsol for the DUT#2 at  $V_{DS}=600V$ ,  $V_{GS}=10V$  and  $T_{CASE}=25^{\circ}C$ : (a) first cycle (b) last cycle (#500).

under  $V_{GS}=20V$  and  $T_{sc}=5\mu s$ . The simulation results of the first cycle (#1) illustrated in Fig. 8a shows from  $4\mu s$  that the temperature on the top layer of the Al reaches the start point of the metallurgical phase transition (solid-liquid). However, it should be noted that the pulse is very short. Moreover, the end of the short circuit appears just after  $1\mu s$  ( $t_{pw}=5\mu s$ ) which leads to a partial melting of the layer. In fact, it is clearly shown that during this  $1\mu s$  time slot, the metal layer temperature forms a plateau which shows a transient phase of latent heat accumulation of the metallurgical phase transition. Furthermore, at the end of the pulse ( $t_{pw}=5\mu s$ ), the Al layer still seems to be in a phase transition regime since the temperature on top layer of the Al did not change and did not follow the temperature increase on the bottom layer of the Al. Afterwards, the accumulated energy over  $1\mu s$  is released during the following microsecond, leading to the solidification of the whole Al layer. Through a thermo-mechanical stress point of view, it is obvious that the estimated temperature of the metal top is above 600K, which leads to the mechanical rupture of the ILD - SiO<sub>2</sub> to 1.4GPa, by compression to the Al layer on the top of SiO<sub>2</sub> [17]. At cycle #400, as illustrated in Fig. 8b, the simulation shows the lack of the Al layer melting even if the device continues its

ageing. This is related to  $I_{DS}$  decrease which is proportional to the power density reduction causing the metal temperature fails to reach the Al melting level. However, as indicated previously this level is still sufficient to exceed the critical limit of 600K

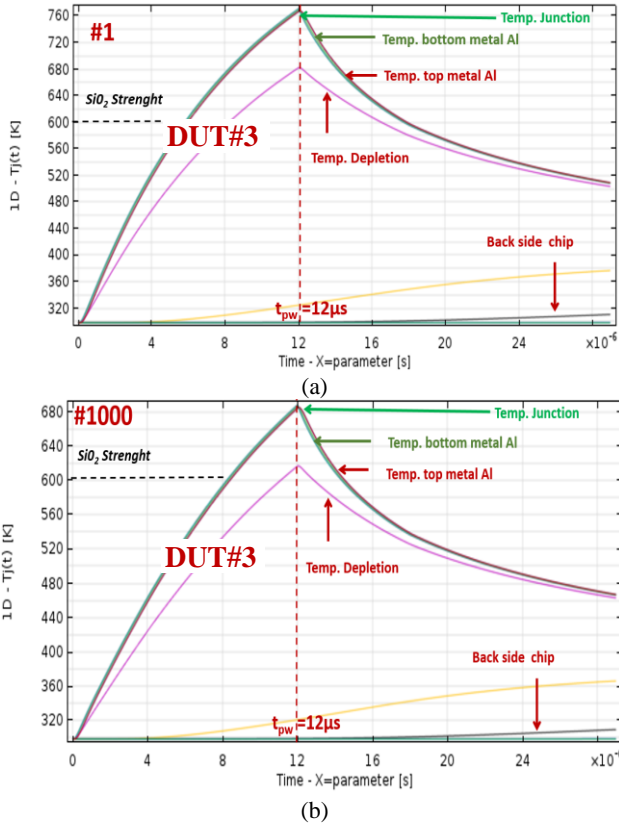


Fig. 10. Estimated temperature of the main chip layers under Comsol for the DUT#3 at  $V_{DS}=600V$ ,  $V_{GS}=10V$  and  $T_{CASE}=25^{\circ}C$ : (a) first cycle (b) last cycle (#1000).

and the mechanical failure of the ILD in which molten Al could have infiltrated at the beginning of cycling.

#### 4.2. High $V_{GS}$ depolarization effect ( $V_{GS}=10V$ )

Fig. 9 presents the estimated temperature of the main chip layers during the short circuit time for the first and the last cycle using DUT#2 under  $V_{GS}=10V$  and  $T_{SC}=22\mu s$ . The simulation shows the same behavior as for DUT1# under  $V_{GS}=20V$  and  $V_{DS}=600V$ . Consequently, the  $V_{GS}$  depolarization does not show any benefits on SiC MOSFET capabilities submitted to repetitive short-circuit.

#### 4.3. Short circuit duration effect

The device DUT#3 ( $V_{GS}=10V$  and  $T_{SC}=12\mu s$ ) shows different behavior of the estimated temperature as presented in Fig. 10. The simulation does not show the same behavior as for DUT1# under  $V_{GS}=20V$  and  $V_{DS}=600V$  because the maximum junction temperature does not reach the level of Al solid-liquid phase transition at 960K, yet the device shows ageing signs (such as  $V_{GS}$  drops). This result deserves to be consolidated by further works including thermo-mechanical simulation. It may

be suggested that the main gate-degradation condition is related to the oxide rupture at around 600K, without the necessity to reach the melting temperature of aluminum. In such conditions, it can probably deform the oxide and let aluminum penetrates cracks by compression of metal and epoxy resin. An additional

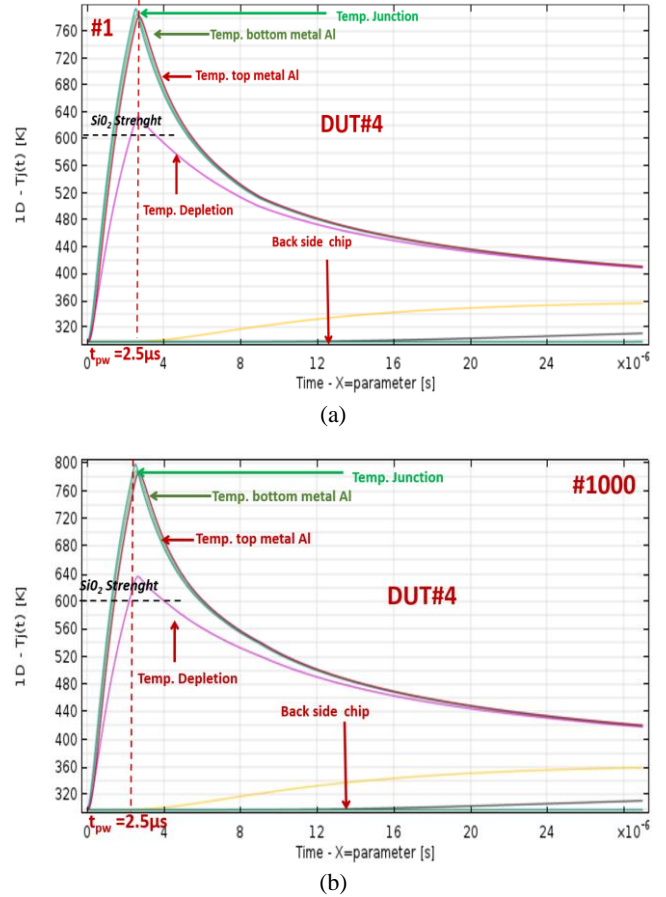


Fig. 11. Estimated temperature of the main chip layers under Comsol for the DUT#4 at  $V_{DS}=600V$ ,  $V_{GS}=20V$  and  $T_{CASE}=25^{\circ}C$ : (a) first cycle (b) last cycle (#1000).

condition is that mechanical deformation time constants have to be respected. Indeed, at low power density a slower temperature rate allows longer duration for cracks initiation to form completely deep down. The simulation shows that at cycle #1000 the temperature remains above 600K which is well confirmed by an ageing of the oxide. For both simulation cases, the temperature of top metal always exceeds the limit of the mechanical failure of the ILD-SiO<sub>2</sub>.

However, in Fig. 11, the estimated temperature during the short-circuit time for DUT#4 ( $V_{GS}=20V$  and  $T_{SC}=2.5\mu s$ ) does not present any variations between the first and the last cycle (#1000) while the temperature is still above 600K the considered SiO<sub>2</sub> strength. It should be noted that the pulse duration is 4.8 times shorter (2.5 $\mu s$  vs. 12 $\mu s$ ) and we can therefore hypothesize that the formation of gate damage is governed by a time constant and probably also a threshold effect which is not reached in the 2.5 $\mu s$  pulse case. Therefore, no-visible degradation has been

observed for this device which shows the benefit of reducing  $T_{SCmax}-1\mu s$  to  $(T_{SCmax}-1\mu s)/2$  at  $V_{GS}=20V$ .

#### 4.4. Imaging - Failure mode analysis

To confirm the assumptions on the failure mode type and also to provide a more detailed technological analysis, we

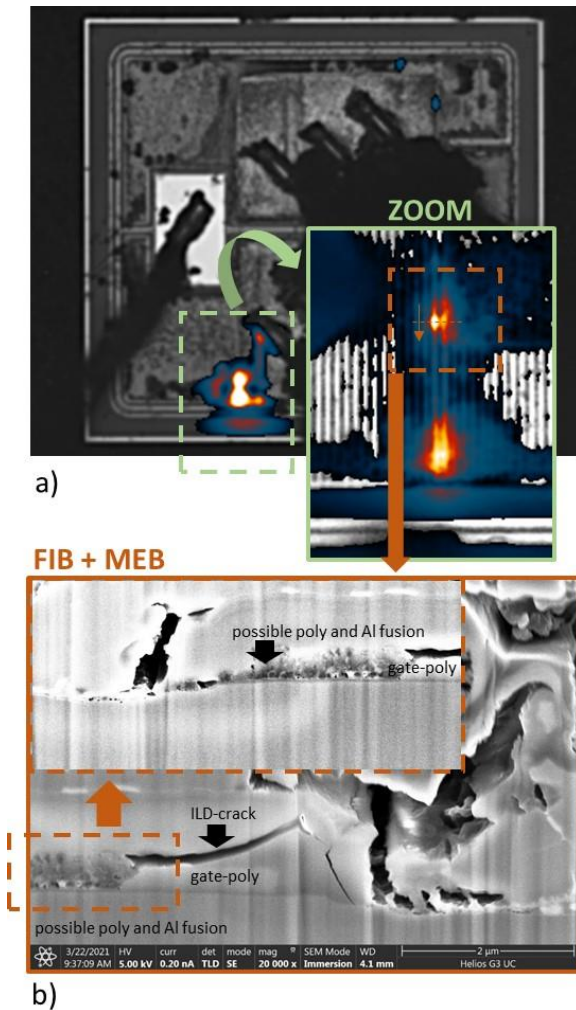


Fig. 12. ILD-crack and Al-gate-Poly fusion of DUT#2 ( $V_{ds}=600V/V_{gs}=10V/T_{sc}=22\mu s$ ) LIT (26Hz /  $V_{gs}=10V / I_{gs}=11mA$ ) and FIB+MEB failure analysis. @Ncycle=500.

carried out a failure analysis of aged DUT#2 @  $V_{ds}=600V / V_{gs}=10V / T_{sc}=22\mu s$ , @Ncycle #500 as illustrated in Fig. 9b). Fig. 12 a) shows a magnitude Lock In Thermography analysis (LIT) @26Hz on one of the two failure zones on the surface along a gate line, localized close one edge of the chip. Through a phase mode of the same LIT analysis, we have chosen to further analyze the zone with the most intense and rapid heating. Fig. 12b) shows an example of micro section, FIB and MEB analysis in the cross-sectional plane of the gate line zoom. The presence of significant through cracking of the ILD between the Al source plan and the polysilicon gate contact is clearly

demonstrated, as well as a possible melting region between the gate polysilicon and the aluminum layer.

#### 5. Conclusion

This paper presents the impact of repetitive short-circuit operation on a commercial SiC MOSFET. The device performance under repetitive stress is analyzed under two protocols. The first one aims at studying the effect of the gate-source voltage ( $V_{GS}$ ) and the second one aims to evaluate the impact of the SC duration ( $T_{SC}$ ) reduction.

The first approach ( $V_{GS}$  depolarization) at  $(T_{SCmax}-1\mu s)$  shows that, despite this technique ensured a safe failure mode (FTO) and a short circuit duration exceeding  $10\mu s$ , has no beneficial impact on the number of cycles for the degradation initiation. Since these degradations occur for high and low  $V_{GS}$  ( $V_{GS}=20V$  and  $V_{GS}=10V$ ) at the same number of cycles. The aged devices at repetitive SC test under low  $T_{SC}$  ( $(T_{SCmax}-1\mu s)/2$ ) shows obviously a better robustness compared to  $(T_{SCmax}-1\mu s)$ .

The simulation results highlight two main degradation behaviors. Both degradations are related to thermal stress. The first one is initiated when the temperature reaches around 600K which is related to the mechanical failure at the ILD-SiO<sub>2</sub>. The second one is related to metallurgical phase transition where the junction temperature reaches the Al melting, leading to partial cracks short between gate-source terminals (shorting gate-source). The ageing of the gate at  $(T_{sc}-1\mu s)/2$  can also occur even if the source metal has not reached the melting temperature as we can see when  $V_{GS}$  voltage drops. Hence the need to monitor other electric parameters such as gate source capacitance ( $C_{GS}\cdot V_{GS}$ ) and static gate leakage current ( $I_{GSS}$ ) to have other degradations signatures and reveal the failure mechanism.

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