



Fast cut-off, low I² T and high temperature monolithic on-chip fuse on silicon substrate for new fail-safe embedded power switch

Amirouche Oumaziz, Emmanuel Sarraute, Frédéric Richardeau, Abdelhakim Bourennane, Céline Combettes, Vincent Bley, Ayad Ghannam

► To cite this version:

Amirouche Oumaziz, Emmanuel Sarraute, Frédéric Richardeau, Abdelhakim Bourennane, Céline Combettes, et al.. Fast cut-off, low I² T and high temperature monolithic on-chip fuse on silicon substrate for new fail-safe embedded power switch. Microelectronics Reliability, 2021, pp.114240. 10.1016/j.microrel.2021.114240 . hal-03381413

HAL Id: hal-03381413

<https://hal.science/hal-03381413>

Submitted on 16 Oct 2021

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Fast cut-off, low I^2t and high temperature monolithic on-chip fuse on silicon substrate for new fail-safe embedded power switch

Amirouche Oumaziz^{1,2,3}, Emmanuel Sarraute^{1,3}, Frédéric Richardeau^{1,3}, Abdelhakim Bourennane², Céline Combettes³, Vincent Bley³, Ayad Ghannam⁴

¹ University of Toulouse; INP; UPS; LAPLACE (Laboratoire Plasma et Conversion d'Energie) ENSEEIHT

² LAAS-CNRS, University of Toulouse, CNRS, UPS, Toulouse, France
2 rue Charles Camichel, BP 7122, F-31071 Toulouse cedex 7, France

³ CNRS; LAPLACE; F-31071 Toulouse, France

⁴ 3DiS Technologies, Miniparc, 478 Rue de la Découverte, 31670 Labège, France

Abstract— In this paper, a first concept of monolithic semiconductor fuses on silicon substrate, is realized and experimentally characterized. These new compact devices are, able to perform fast and irreversible current cut-off at medium voltage (200V), relatively high current (10A), with very low pre-arcing time ($\sim 4 \mu s$ to $5 \mu s$). The fuses are intended for fail-safe power converter capabilities applications. Design and 3D simulation by finite elements method, taking into account static and dynamic specifications have been carried out. Thermal management in steady state is improved by dielectric epoxy thermal insulation under each constriction of the fuse. Implementation and practical tests are reported.

Keywords— *On-chip fuse, Power Converters, fuse design, 3D finite elements method.*

I. INTRODUCTION

Power electronic devices are widely used in different applications requiring high reliability, like automotive. Then, it is very important to improve the availability in order to guarantee fault tolerance and continuity of service. Fuses are simple, passive and inexpensive components, capable if they are well designed to protect electrical devices in the event of short-circuits. In this paper, a new concept of fuses is presented, for power semiconductor devices protection. These fuses could be monolithically integrated within active power devices [1] [2], in fail-safe power inverters capabilities [3] [4] [5] using SMD commercial fuses or PCB fuses prototypes. An example of a fail-safe capability is presented in Figure 1. The configuration considers a back-up half-bridge, allowing inverter's post-fault reconfiguration at full power.

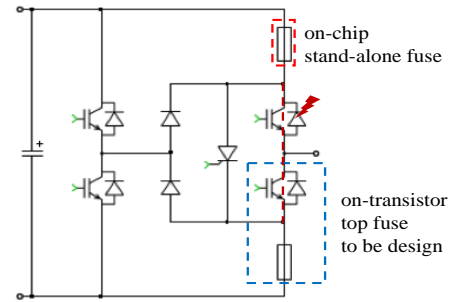


Figure 1 :Fail-safe topology

Monolithic association of a top fuse on RC-IGBT (Figure 1, blue dashed box) would be very interesting, more secure IGBT can be provided, increasing their global reliability and applications.

II. FUSES CHARACTERISTICS & DESIGN

A. Characteristic of the targeted monolithic fuses

Usually, to protect semiconductor components, fuses are made from thick or thin metal films (copper or aluminum) on commercial SMD fuses [6], Printed Circuit Board (PCB) substrates [5] [7] [8] or printed on PCB using conductive composites (silver) [9] for low power applications. The proposed fuses (Figure 2) consist of a thin ($18 \mu m$) film of copper deposited on a massive $400 \mu m$ silicone substrate. When the energy let-through (I^2t in $A^2.s$) is exceeded, in case of a short-circuit occurrence, the metal constituting the constrictions evaporates. The distance across the pads must be sufficiently long (1mm here) to withstand the supply voltage (up to 400 VDC). The evaporation must be irreversible in order to minimize the presence of metallic particles, which could cause re-arcing phenomena.

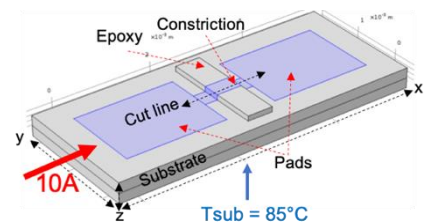


Figure 2 :On-chip fuse design

A major difficulty of fuse technology is to create an insulating coating to trap the vaporized metal particles and passivate them in order to maintain a recovery voltage at least equal to that of the power supply without the risk of current leakage and arc recovery. The choice of material and its deposition mode is essential. This aspect is the subject of this article. Another important point is the control of the cut-off speed to limit the overvoltage and to avoid breakdown other components in parallel. This aspect is even more complex and will not be dealt with in this article.

The fuses design simulations have been carried out using “Comsol Multiphysics™ (software version 5.3a)”. The

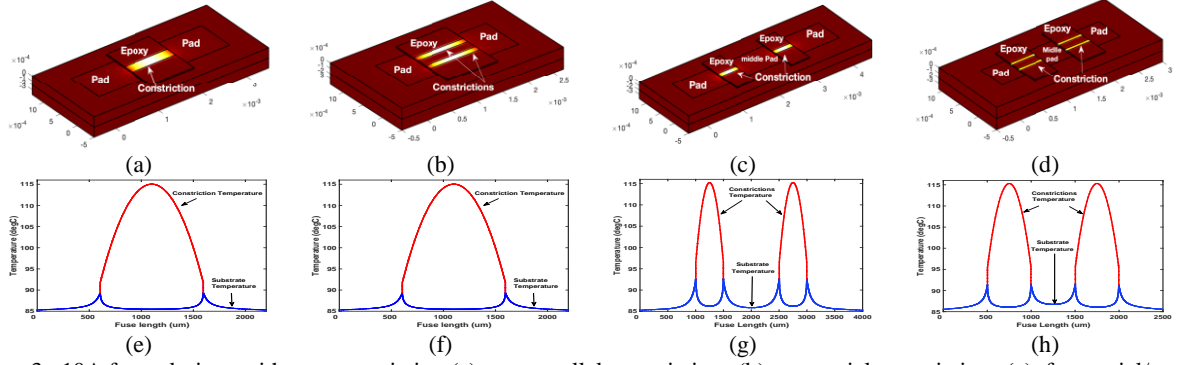


Figure 3 : 10A fuses designs with one constriction (a), two parallel constrictions (b), two serial constrictions (c), four serial/parallel constrictions (d) and their respective temperature profile (blue for the substrate and red for the constrictions) (e)-(h)

from the substrate (higher thermal conductivity), which allows to focus the energy on its center, optimizing constriction’s evaporation.

B. Design and electro-thermal simulations

Geometrical, electrical, physical, thermal and mechanical parameters, like constrictions length and thickness, materials thermal and electrical conductivity, rating current, temperature, are combined and built up in Comsol simulations to adjust the constrictions maximum temperature by processing their widths. Four fuses topologies were designed, depending on the number of serial (N_s) and parallel (N_p) constrictions. Fuses topologies, constriction and longitudinal substrate temperatures distribution are shown in Figure 3.

A preliminary theoretical calculation from the Fourier’s law, allowed us to set up the initial constriction’s width value for the mono-constriction design, with respect to the maximum allowed temperature (115 °C).

$$\Phi = -\lambda \frac{\Delta T}{\Delta x} \quad (1)$$

Where Φ represents the heat flux density, λ the thermal conductivity and $\frac{\Delta T}{\Delta x}$ the thermal gradient.

The reference design ($N_s=N_p=1$, Figure 3.a) required a constriction’s width of 240 μm to fit the temperature parameter (115 °C). Furthermore, the optimized epoxy’s thickness (25 μm) ensures thermal decoupling between the constriction (red line) and the silicon substrate (blue line) (Figure 3.e). Power losses through the constriction are estimated to 394 mW, which is comparable with the average losses in commercially available substrate fuses for the rated current. In order to minimize the fuse’s chip area, we added a parallel constriction ($N_s=1$ $N_p=2$, Figure 3.b) to the first model. As a consequence, power dissipation has been

fuses have been designed for 10 A nominal current at 85 °C substrate’s maximum temperature, allowing 115 °C maximum constriction’s temperature, because electronic power devices could operate in extreme temperature conditions [10]. Substrate’s passivation is ensured by using thin film of Nitride below the copper layer in order to avoid leakage currents after the constriction’s blows. Optimized epoxy (low thermal conductivity, 1.16 W.m⁻¹.K⁻¹) thickness (25 μm), thermally insulates the constriction

improved, due to an improved heat distribution. To fit the specification of 115 °C constriction’s maximum temperature at the rated current, a 117 μm constriction’s width was required. The spacing between the two parallel constrictions is chosen so the substrate’s temperature distribution between them, is close enough to set-up temperature (85 °C), to avoid thermal coupling (Figure 3.f). This improved configuration afforded an area gain of 37 % as compared to the reference fuse design described above, with approximatively the same power losses (404 mW). A serial constriction is added to the reference design to build up a two serial constrictions fuse ($N_s=2$ $N_p=1$, Figure 3.c). The idea is to split the initial constriction’s length (1 mm) in two equal constrictions of 500 μm length, which will split the electrical and mechanical constraints on the silicone substrate during the constrictions break-up and improve the thermal dissipation through the substrate. A shorter track has a reduced thermal deflection and therefore allows an even smaller thickness at maximum iso-temperature. To separate the constrictions, a middle pad is added, which unfortunately increases the fuses area, but it is size optimized to insure thermal decoupling between them. Figure 3.g shows a dissociate constrictions temperatures profile thanks to the middle pad. The estimated area loss is about 15 % compared to the reference design. Only 138 μm constriction’s width is required to reach the constriction’s maximum temperature specification with power losses estimated to 684 mW. The last configuration combines the advantages of parallelization and serialization in a structure made of four constrictions ($N_s=N_p=2$), as shown in Figure 3.d. Parallelizing and serializing give noticeable improvement on the fuses area. Indeed, the estimated area gain is about 73 % as compared to the reference design ($N_s=N_p=1$). Only 67 μm constriction’s width was required to reach the maximum allowed temperature of 115 °C. This configuration shows an estimated power loss about

705 mW, which is still in the average as compared to the commercially available substrate fuses.

In the case of fault occurrence, the current ($I_{cc}(t)$) increases through the stray inductance to reach the maximum value ($I_{cc\max}$) that results fuse melting. Given the expression of the I^2T_p quantity in relation (2) and the current curve expression ($I_{cc}(t) = \left[\frac{di}{dt}\right]t$), the expression (3) of the pre-arcing delay time T_p can be obtained:

$$I^2T_p = \int_0^{T_p} I_{cc}^2(t)dt \quad (2) \quad T_p = \left(\frac{3[I^2T_p]}{\left[\frac{di}{dt}\right]^2}\right)^{1/3} \quad (3)$$

Where I_{cc} represents the maximum default current through the fuse element defined by the relation (4):

$$I_{cc\max} = \left(3 \frac{di}{dt} [I^2T_p]\right)^{1/3} \quad (4)$$

Designs improvements made very fast fuses, Figure 4 shows actual fuses areas and I^2T value for each fuse configuration.

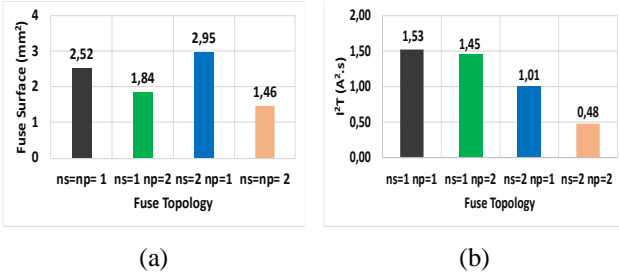


Figure 4 : 10 A fuses surfaces (a) and I^2T_p (b) versus fuses topologies @ $I_{\text{Nominal}}=10$ A, fuse's maximum temperature=115 °C, substrate's maximum temperature=85 °C, copper's thickness=18 μm and epoxy's thickness=25 μm

Both parallelization and serialization made very fast fuses (2.8 and 3.1 μs at 1420 A and 630 A respectively) with lower I^2T_p (1.45 and 1.01 $\text{A}^2.\text{s}$ respectively) melting energy requirement compared to the reference design (1.53 $\text{A}^2.\text{s}$). The serial configuration presents more occupied area, because of the middle separation pad. The highest improvement is achieved when both parallelization and serialization are combined simultaneously. The last design shows improvements in both occupied area and energy breakup requirements I^2T_p (0.48 $\text{A}^2.\text{s}$) with mainly low pre-arcing time (1.9 μs at 770 A). These integrated fuses occupy at least four times less area, and are three times faster, than one of the compact [11] and faster [12] commercially available fuses.

Such a low value suggests the possibility of directly protecting a transistor device in short-circuit operation with a fuse, provided that the fuse can be replaced.

III. FUSES REALIZATION

The monolithic on-chip fuse devices are fabricated using conformal 3D-RDL technology [13]. This technology consists on forming 3D conformal interconnects over ICs or packages using wafer-level processing. It enables forming 3D interconnects, both horizontal and vertical parts simultaneously, using a single electroplating step. Hence, no multiple planar RDL with vias are involved, reducing thus the number of processing steps. In general, the technology involves forming first a 3D re-passivation layer over 3D

topography (i.e. a die or a 3D feature) to isolate the 3D interconnects from their surrounding environment while keeping openings in desired locations for electrical connection with underlying device [14]. Then, the 3D interconnects are formed using 3D copper electroplating inside a photoresist. The particularity of this technology is its capability of forming high aspect ratio 3D-RDL/3D Interconnects over a vertical sidewall [14].

In the current work, fabricating the devices involved the following steps: 1/ a nitride layer was deposited on the silicon substrate to electrically isolate it from the 3D interconnects; 2/ a 25 μm -thick epoxy layer was formed above the substrate. This layer serves as a core to form the constriction of the fuse using 3D-RDL technology. No re-passivation layer was needed as the core was already insulative; 3/ a seed layer was sputtered above the substrate; 4/ a photoresist was deposited and 3D patterned; 5/ 20 μm -thick 3D copper interconnects were electroplated inside the photoresist. For the presented device, the copper laid-out partly on the epoxy core and on the substrate, without electrical connection to the later as it was passive; 6/ etching and cleaning. These steps are shown on Figure 6. When integrating the monolithic fuses above an active chip, the same processing steps could be applied. The first step of depositing a nitride layer can be omitted if the chip has one above it that answers design requirements. On the other hand, an organic re-passivation layer can be applied for electrical shielding from unwanted areas and/or to increase the separation distance between the fuse and some sensitive parts of the chip, such as RF areas. Given the small number of processing steps, the proposed herby solution is very advantageous for fabricating at wafer-level high-Rel active devices with fuses on-chip.

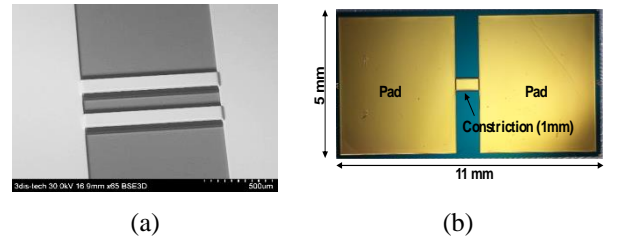


Figure 5 : Microscopic view of a parallel fuses constrictions (a) and microphotography of the realized 10 A mono-constriction fuse (b).

The fuses have been realized in collaboration with 3DiSTM [15] using facilities of the micro and nanotechnology platform of LAAS-CNRS laboratory. The pads are oversized (5x5 mm^2) in order to ease the measurements and experiments. A microscopic view of a parallel fuse constrictions and a mono-constriction fuse picture are shown in Figure 5.c and Figure 5.d.

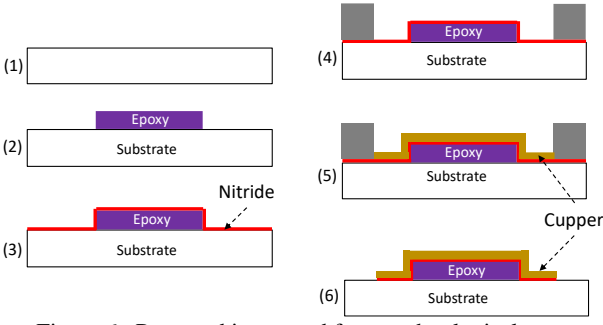


Figure 6 : Proposed integrated fuses technological steps

IV. EXPERIMENTS AND RESULTS

A. Fuses characterization

The characterization process and experimental tests were carried out at Laplace laboratory. A four wires method was used for fuses characterization. Table 1 summaries fuses theoretical and measured nominal resistances. The theoretical values comprise only the constriction part resistances, but we can see that the tendency is respected. Even though the measured values comprise wire bonds, fuses pads (oversized for the experiments) and external contacts pads resistances, they still very low or at least even, compared to commercially available fuses, like compared in [16]. The specific resistance of the fuses is calculated using the relation (5), where R_{pads} and $R_{Constriction}$ represent the fuse pads and constriction resistances, S_{fuse} the actual fuse's occupied surface.

$$R_{fuse} \times S_{fuse} = (R_{pads} + R_{Constriction}) \times S_{fuse} \quad (5)$$

$$R_{fuse} \times S_{fuse} = (2.28 \text{ m}\Omega + 3.98 \text{ m}\Omega) \times 2.52 \cdot 10^{-2} \text{ cm}^2$$

The fuse's specific resistance ($0.157 \text{ m}\Omega \cdot \text{cm}^2$) is at least 60 times less important than specific resistance ($10 \text{ m}\Omega \cdot \text{cm}^2$) of commercially available power switches. Meaning that the fuses will not induce any important power losses when integrated on power switch.

Table 1: Fuses measured nominal resistances

Design \ Nom. Resistance ($\text{m}\Omega$)	ns=np=1	ns=1 np=2	ns=2 np=1	ns=np=2
Theoretical	3.98	4.08	6.92	7.13
Measured	6.23	6.74	12.87	12.83

Measured at 10% of rated current

B. Preliminary experimental test without passivation

The experimental test circuit (Figure 7) is mostly composed of a current-limited voltage source, four parallel capacitors which makes a total capacitance of $1880 \mu\text{F}$. A crowbar thyristor is used to trigger the short-circuit. It is used to take advantage of its very high overcurrent capacity without being destroyed unlike a transistor. In order to limit the energy and to limit the di/dt max value, a 700 nH snubber inductance was added. When triggered, the serial thyristor creates a current path through the fuse, like a short-circuit. A freewheeling diode is included in parallel with the

inductance as in real switching cell. This diode is important, it prevents the fuse from having to dissipate all the energy stored in the snubber inductance. Only the energy dissipated in the stray inductance, around 50 nH , will be dissipated in the fuse as in a real switching cell.

When the thyristor is triggered, the capacitors stored energy is partially discharged through the fuse, which increases its voltage and current until the required constriction's melting point energy is reached, resulting in its interruption. Finally, the initiated arc persists until the current reaches zero. This current cancellation must remain indefinitely and must not restrike. The primary fuses interruption process studies were carried out on non-passivated mono-constriction fuses in order to study the electrical behavior. The results of the interruption, obtained for 50 V , microphotograph of the interrupted constriction and the measured leakage current are presented in Figure 8. Unfortunately, the results (Figure 8.a) showed current restrike during the arcing period. As a result, both pads adjacent to the constriction were damaged (Figure 8.b). That could be attributed to an excess of energy and without any top fuse passivation, it spreads over the pads. In order to achieve a satisfactory and controlled interruption without any pads damages, fuses passivation is required. To accomplish the passivation process, silicone gel, like used in power inverters modules, to help reduce mechanical stress, electrical breakdown, moisture, etc. seems to be the appropriate passivation product. Methods and technological passivation process are described below.

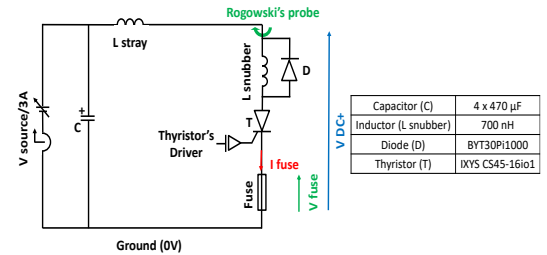


Figure 7 : electrical schematic of the fuse's test circuit (a) and a picture of the experimental bench (b)

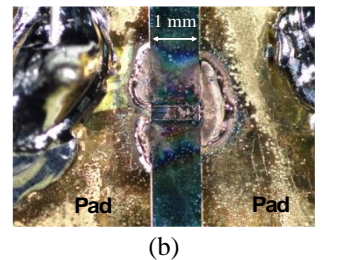
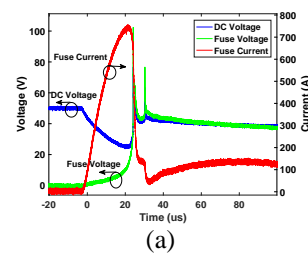


Figure 8 : results of the interruption tests from mono-constriction fuses at 50 V (a), microphotography of the interrupted constriction (b).

C. Fuses passivation technological process

During the fuses cut-off sequence at voltages higher than 100 V, the fuses have to be soldered on the bottom face, otherwise, the mechanical stresses induced by the electrical energy cause silicone substrate breakdown. The fuses were soldered on a FR4 substrate (Figure 9.a). Then, the wire bondings, made of aluminum (254 μm diameter), were designed with an I^2T value, 200 times higher than the devices I^2T values. This is a safety parameter, to support the rated current (10 A), measure the voltage across the constrictions and avoid current variations sensitivity. A specific PTFE mold, comprising a middle cavity, was designed (Figure 9.b) using a 3D printer in order to cast the silicone gel on the chip-fuse.

As a passivating silicone gel, Wacker SilGel 612 A/B, dedicated for electronic components and power electronics industries, is used. Wacker SilGel 612 A/B has a flame retardancy classification of UL 94 HB [17]. Air impurities introduced during the dispensing sequence, are eliminated using vacuum machine.

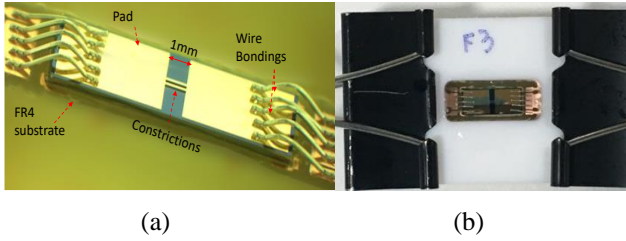
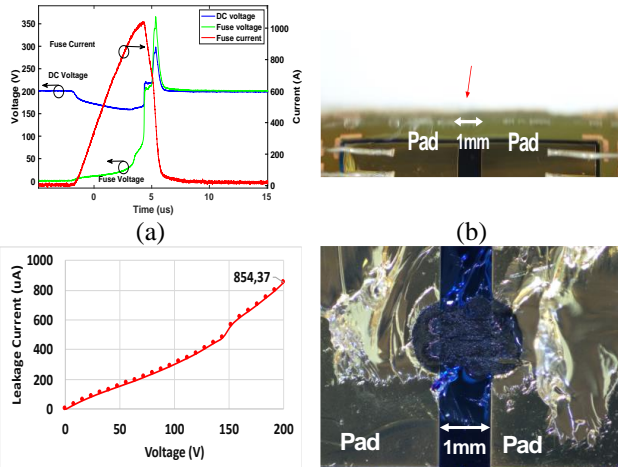


Figure 9 : microphotography of a bonded two parallel constrictions fuse (a), encapsulation process using PTFE mold (b).

D. Results and discussion

Using the experimental test circuit presented above (Figure 7), fuses cut-off tests have been carried out on the different topologies ($n_p=2$ $n_s=1$, $n_p=1$ $n_s=2$, $n_s=n_p=2$). Figure 10 presents the cut-off sequence results for a two parallel constrictions fuse, with associate leakage current measure at rated voltage (200 V).



(c)

(d)

Figure 10 : Electrical characteristics of a two parallel constrictions fuse ($n_s=1$ $n_p=2$) cut-off (a), photography before the cut-off test (b), leakage current at rated voltage (c) and observed constrictions zone after fuse cut-off (d).

The fuses cut-off electrical characteristics (Figure 10.a) are very interesting, no current restrike is observed. Satisfactory cut-off is achieved at 1000 A after a pre-arcing time of $\sim 5 \mu\text{s}$. The silicone gel contained the vaporized constrictions metal (Figure 10.d) by absorbing the excess of energy after the constrictions blew-up. No serious pads damaging was observed. The leakage current (Figure 10.c) is a little high (854 μA , 171 mW) for this fuse version, but the insulation resistance after opening still acceptable (230 k Ω) at rated voltage (200 V).

Serial constrictions fuse configuration ($n_s=2$ $n_p=1$) (Figure 11) showed less current leakage (170 μA , 34 mW) at rated voltage (Figure 11.c). Well fuse cut-off is performed after a pre-arcing time of $\sim 5 \mu\text{s}$ at 720 A. No sign of pads damaging (Figure 11.d) is observed after removing the silicone gel. The insulation resistance (after opening) is very high, about 1.17 M Ω at rated voltage.

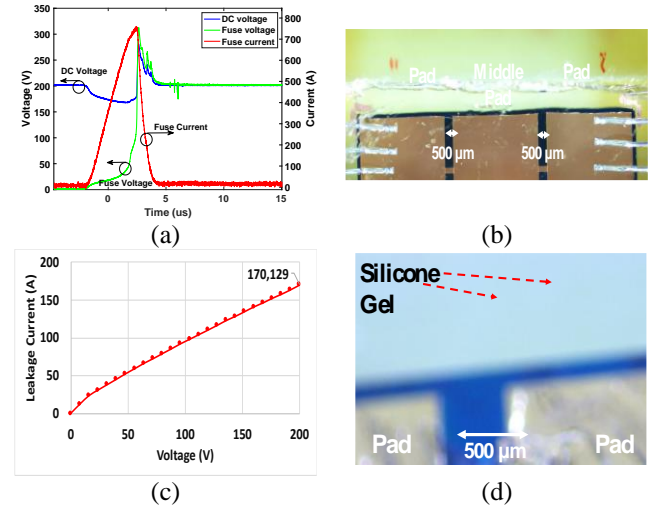


Figure 11 : Electrical characteristics of a two parallel constrictions fuse ($n_s=1$ $n_p=2$) cut-off (a), photography before the cut-off test (b), leakage current at rated voltage (c) and observed constrictions zone after fuse cut-off (d).

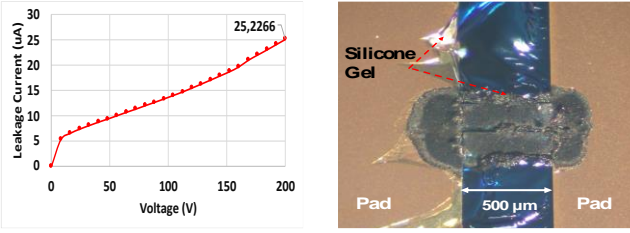


Figure 12 : Electrical characteristics of a four serial/parallel constrictions fuse (ns=2 np=2) cut-off (a), photography before the cut-off test (b), leakage current at rated voltage (c) and observed constrictions zone after fuse cut-off (d).

The last fuses configuration (ns=np=2) showed very interesting results compared to the others. A perfect cut-off is achieved after a pre-arcing time of only $\sim 4 \mu\text{s}$ at 720 A, without any current restrike (Figure 12.a) and no pads damaging (Figure 12.d). Measured leakage current (Figure 12.c) at rated voltage is very low (25 μA , 5 mW), providing an insulation resistance of 8 M Ω . This technology and structure therefore seem promising for a voltage rise and to be compatible with 600 V or even 1200 V rated components used under 300 V and 600 V respectively.

E. I^2T theoretical and experimental comparative

In order to assess the process tolerance, theoretical and experimental I^2T values are compared (Table 2). As expected, the required breaking energies (I^2T) are very low.

Table 2 : Theoretical and experimental I^2T comparative

Design $I^2T(\text{A}^2.\text{s})$	ns=np=1	ns=1 np=2	ns=2 np=1	ns=np=2
Theoretical	1.53	1.45	1.01	0.47
Measured	1.93	1.71	0.7	0.55

Theoretical and measured I^2T values are quit even, with a slight difference only. This could be attributed to the process tolerance and the pre-arcing time calculation. Depending on components placement on the wafer, a process tolerance between 2.7% to 7% has been reported. Figure 13.a shows a four serial/parallel constrictions fuse cut-off results, with color identification of the pre-arcing period (green) and the arcing period (blue). Although, there is time lap (Figure 13.b, orange area) during the pre-arcing period, where the fuse current didn't reach yet its maximum value, meanwhile, the voltage across the fuse suddenly increases in non-linear way. This behavior means that the fuse is no longer in its ohmic state, thus the pre-arcing time definition (until the fuse current reaches its maximum value) no longer applies. During this time lap, the constriction metal is in liquid then gas state, which means the arcing period (blue area) has started. The presented measured values are calculated respecting the pre-arcing period definition (excluding the orange area). In addition, these fuses I^2T values can be at least five times smaller than commercially available fuses (same rated current). It means that the fuses, in case of fault occurrence, will provide a safe current path cut-off, while avoiding circuit's healthy parts damages.

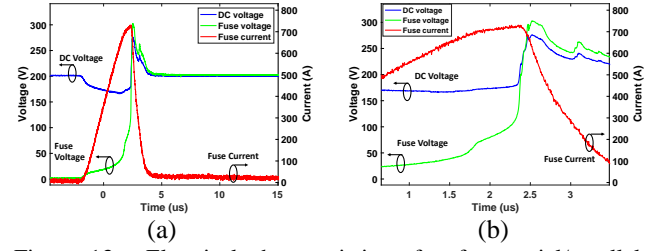


Figure 13 : Electrical characteristics of a four serial/parallel constrictions fuse (ns=2 np=2) cut-off (a) and zoom on the pre-arcing and arcing periods (b)

In case of short-circuit occurrence, a power switch can withstand a designed saturation current for only few tens of microseconds. During a short-circuit fault, the switch component will withstand a saturation current (50 A), for example, five times the rated current (10 A), during $\sim 10 \mu\text{s}$. Even with very low fuses I^2T values (Table 2), the I^2T values of a power switch are even smaller (0.025 $\text{A}^2.\text{s}$ here), meaning that the proposed fuses (even market fuses) cannot be blown first instead of the power switch, but are intended to isolate the power switch fault from spreading and causing further damages (source, load...etc).

V. CONCLUSION

In this paper, a new concept of monolithic on-chip fuses, based on silicone substrate, is simulated and experimentally characterized for the first time. Several fuses topologies were studied under medium voltage (200 V) and showed very good results. The devices are able to perform, fast and safe cut-off, with very low I^2T energy. Especially the four serial and parallel configuration (ns=np=2) version, with very compact occupied area (1.46 mm^2). The insulation resistances after opening are very high (between 230 k Ω and 8 M Ω , depending on the fuses topologies), which guarantee very low leakage current at rated voltage (200 V). Fuses passivation process, using silicone gel, improved the cut-off process by absorbing excess energy. In addition, since power inverters mass production already uses this product, the passivation process using silicone gel will not require more expenses. These good results suggest that design of more compact fault-tolerant inverters, combining active components (IGBTs, SJ-SiC-Mosfet) and on-chip fuses, monolithically, is possible for medium voltage and medium power applications. Future work will focus on the lateral integration of these fuses on top-side connection-diodes for back-up phase-leg link. A 3D structure extension with low size is also in progress.

REFERENCE

- [1] S. E. Berberich, M. März, A. J. Bauer, S. K. Beuer, and H. Rysse, "Active fuse," *Proc. Int. Symp. Power Semicond. Devices ICs*, vol. 2006, pp. 0–3, 2006.
- [2] J. Vom Dorp, S. E. Berberich, A. J. Bauer, and H. Rysse, "DC-arc behavior of a novel active fuse," *ESSDERC 2008 - Proc. 38th Eur. Solid-State Device Res. Conf.*, pp. 67–70, 2008.
- [3] F. Richardeau, Z. Dou, J. M. Blaquiere, E. Sarraute, D. Flumian, and F. Mosser, "Complete short-circuit failure mode properties and comparison based on IGBT standard packaging.

- Application to new fault-tolerant inverter and interleaved chopper with reduced parts count,” *Proc. 2011 14th Eur. Conf. Power Electron. Appl. EPE 2011*, pp. 1–9, 2011.
- [4] M. Gleissner and M. M. Bakran, “Fault-tolerant B6-B4 inverter reconfiguration with fuses and ideal short-on failure IGBT modules,” *PCIM Eur. 2016; Int. Exhib. Conf. Power Electron. Intell. Motion, Renew. Energy Energy Manag.*, no. May, pp. 683–690, 2016.
- [5] Z. Dou *et al.*, “PCB dual-switch fuse with energetic materials embedded: Application for new fail-safe and fault-tolerant converters,” *Microelectron. Reliab.*, vol. 52, no. 9–10, pp. 2457–2464, 2012.
- [6] M. Labrousse, B. Antoine, C. Suzan, and H. Daniel, “First Practical evaluation of a complete fail-safe and 100 % fault-tolerant inverter for critical load in aerospace application,” in *8th International Conference on Recent Advances in Aerospace Actuation Systems and Components (R3ASC)*, 2018.
- [7] Y. Ishikawa, K. Hirose, M. Asayama, Y. Yamano, and S. Kobayashi, “Dependence of current interruption performance on the element patterns of etched fuses,” in *8th International Conference on Electric Fuses and their Applications, ICEFA*, 2007, pp. 51–56.
- [8] M. Tsuchiya, Y. Yamano, S. Kobayashi, and K. Hirose, “Basic research on the fuse element pattern changing a current pathway in the process of current interruption,” in *2013 2nd International Conference on Electric Power Equipment - Switching Technology, ICEPE-ST 2013*, 2013, pp. 1–4.
- [9] R. Yang *et al.*, “Low-Temperature Fusible Silver Micro/Nanodendrites-Based Electrically Conductive Composites for Next-Generation Printed Fuse-Links,” *ACS Nano*, vol. 11, no. 8, pp. 7710–7718, 2017.
- [10] V. Smet *et al.*, “Ageing and failure modes of IGBT modules in high-temperature power cycling,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4931–4941, 2011.
- [11] Eaton, “Eaton Fast-Acting SMD BrickFuses CB61F Series.” pp. 1–4.
- [12] Mersen, “Fusibles Protistor Standard 250 V- URE-URZ calbres 5 a 180 A.” pp. 1–4.
- [13] A. Ghannam, D. Bourrier, L. Ourak, C. Viallon, and T. Parra, “3-D multilayer copper interconnects for high-performance monolithic devices and passives,” *IEEE Trans. Components, Packag. Manuf. Technol.*, vol. 3, no. 6, pp. 935–942, 2013.
- [14] A. Ghannam *et al.*, “Ultra-thin QFN-like 3D package with 3D integrated passive devices,” in *Electronic Components and Technology Conference (ECTC) 2019*, 2019, vol. 2019-May, pp. 1789–1795.
- [15] A. Ghannam, “3Dis technologies.” [Online]. Available: <https://www.3dis-tech.com/>.
- [16] A. Oumaziz, Amirouche, Sarraute, Emmanuel, Richardeau, Frédéric, Bourennane, “Fail-safe switching-cells architectures based on monolithic on-chip fuse Keywords Fail-safe topologies using single-fuse or dual-fuse function,” in *European Conference on Power Electronics and Applications (EPE 2020 ECCE Europe)*, 2020, p. 10.
- [17] Wacker, “Creating tomorrow ’ s solutions today,” 2013.