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Yazan Barazi, Frédéric Richardeau, Nicolas Rouger, Jean-Marc Blaquière. Robustness study of a fast protection method based on the gate-charge dedicated for SiC MOSFETs power device. *Microelectronics Reliability*, 2021, pp.114246. 10.1016/j.microrel.2021.114246 . hal-03381405

HAL Id: hal-03381405

<https://hal.science/hal-03381405>

Submitted on 16 Oct 2021

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Robustness study of a fast protection method based on the gate-charge dedicated for SiC MOSFETs power device

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Abstract

This paper focuses on the extensive robustness validation of a gate charge detection method designed for SiC MOSFETs under short-circuit operation, and, in terms of failure-modes. The benefits of having a fast (sub-microsecond – 150ns) detection method is illustrated by a 1D thermo-metallurgical simulation. This method is integrated owing to an optimized SMD/PCB technology (Surface-Mount Device/ Printed Circuit Board).

1. Introduction

The silicon carbide (SiC) MOSFETs have much better physical characteristics than Silicon. And, SiC MOSFETs offer several advantages such as low switching losses, higher switching frequencies, and high temperature stability, which makes them an alternative solution of Silicon IGBTs or SJ-MOSFETs [1]. SiC MOSFETs are taking over different markets, where they are found in different applications, especially automotive applications. However, short-circuit (SC) robustness is a key application requirement for power semiconductor devices. The short-circuit (SC) withstanding time (T_{SCWT}) of SiC MOSFETs is lower than silicon devices [2], within $t_{sc}=2\mu s$, [3] against $t_{sc}=10\mu s$ for Si IGBTs.

Many kinds of SC detection methods have been demonstrated for Silicon IGBTs [4] and SiC MOSFETs [5,6]. Most of the proposed techniques rely on the drain-source high-voltage or direct current sensing. Those techniques are more suitable for bipolar transistors such as IGBTs, and on the other hand they are limited due to the use of a high-voltage rating diode or using special sense-FET SiC devices [7].

This detection method is proposed in order to pile on exciting detection methods and to fill the present gap, as well as, to answer to several problematics faced nowadays by SiC MOSFETs. This paper proposes an original 2D diagnosis [8] detection method which is the best candidate to minimize the detection timing. The studied method depends on the fast integration of the gate current, the gate charge sequence at turn-on. The gate charge method already proved interesting results for Si IGBTs [9] but unclear results for SiC MOSFETs in terms of performances and practical PCB integration [10]. This study validates experimentally the gate charge method and fault-management for SiC MOSFETs embedded circuit in real full-voltage operation. This method is an adapted detection method, which

depends on the gate charge variation on the switching cycle, between normal operation and short-mode. This method detects as early as possible the SC and turn softly the device off.

Power semiconductor devices are exposed to several types of short circuits. In summary, internal Hard switching fault (HSF, SC type1) and external fault under load (FUL, SC type2) are the two main fault behaviors. HSF occurs when the switch turns on with a permanent full bus voltage across itself typically caused by faulted control signals. FUL occurs when the device is already in on-state and an external short-circuit occurs. HSF and FUL can be distinguished by the presence or not of a dv/dt on the drain source of the MOSFETs. In all cases, MOSFETs saturates at high current density leading to a thermal dynamic source of heat in a few microseconds for the least robust components. The scope of this study is limited to HSF mode.

2. Fast detection method

2.1. The benefits of a sub-microsecond detection

In fact, the detection methods used nowadays in the industry require the measurement of V_{DS} . Therefore, the measurement of a high voltage involves different problems such as noise, high dv/dt , high-voltage components and over-cost to protect the control circuit, etc... The well-known detection method is the desaturation method and it requires a high-voltage diode for sensing, as well as, a blanking time. Moreover, the blanking time increases the protection time, which can cause the device to undergo more thermal stress at high short-circuit SC drain current. In order to support this, a thermal modelling and simulation of the chip temperature is carried out, Fig.1., which shows different thermal levels where the device undergoes different stress levels and corresponding failure-modes. The important stress level is the first one where the SiO_2 strength is reached around 600K and the device goes through mechanical stress, or even visible mechanical

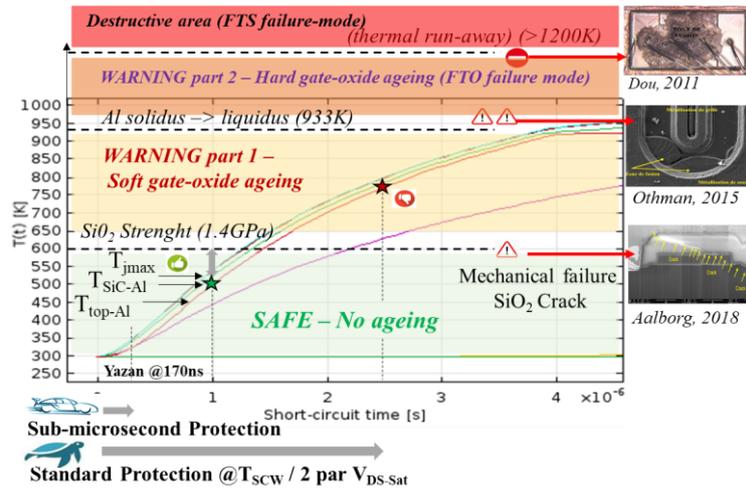


Fig. 1. 1D electro-thermal-metallurgical (Al) simulation highlighting different stress levels. [11,12,13]

failures [11]. Afterwards the device enters an ageing region, where the gate starts to weaken until the device reaches Al solidus to liquidus temperature range, 933K. Above this temperature, the device shows two failure modes: gate-damage also called Fail-to-open 'FTO' mode or thermal-runaway and BJT region latch-up giving the Fail-to-short 'FTS' mode.

Using the desaturation method; which detects the presence of the SC around 1-2 μ s; can lead the device into the ageing region. Therefore, even if the power device is protected, the device will not withstand several SC due to the accumulation of the non-visible damage brought by the thermal and physical stress. On the other hand, by protecting rapidly the device under 1 μ s, it reduces the physical and thermal stress on the oxide of the SiC MOSFET, which allows a longer operation lifetime.

2.2. Gate charge method under Hard Switch Fault

This study is focused in short-circuit under Hard Switch Fault 'HSF', whose fault dynamic is faster than Fault Under load 'FUL' one. In the literature there are different architectures proposed for the gate charge method. In this study the circuit is quite the same in the concept. This gate charge method does not require high voltage diode for sensing or setting a detection period as the desaturation method. Moreover, this method has also, potentially, a high SNR. In the principle, this method requires a resettable integrator to estimate the amount of gate charge Q_G ; and two comparators. The first comparator is to distinguish the difference between the charge amount under short circuit Q_{G-SC} and normal turn-on (NTO) Q_{G-NTO} ; the second comparator comes to create a reading flag using only V_{GS} signal threshold crossing [14] and therefore a blanking time is not required. Fig.2.(a). summarizes in a 2D diagram the gate charge amount under NTO and SC-HSF as a function of V_{GS} .

The validation of the gate charge method has been presented in [15]. And in order to furthermore study the robustness of the designed circuit, the same test Barazi *et al.* - 2021

presented in Fig.2.(b) has been led. The circuit in fig.2(b) was proposed using on the low side a 1.2kV-80m Ω , C2M0080120D gen. II SiC MOSFET transistor, and on the high side a SiC 600V SBD (Schottky barrier diode) with a coreless inductor of 270 μ H as the load for the normal operation. A copper short-strap across the high side switch is used in order to get the HSF mode. The gate driver used is a 3-state fast buffer, which allows a high impedance configuration. The dedicated and optimized SMD/PCB circuit was implemented in the power test bench as a plugging board. Low voltage signals (as V_{GS} and V_{Drv}) are mostly measured with self-compensated voltage probes (300V and 1 GHz bandwidth (BW) Tektronix TPP1000). High voltages (as V_{DS}) are typically measured with a probe (1000V and 800MHz BW Tektronix TPP0850). The current is measured through a 2GHz coaxial shunt.

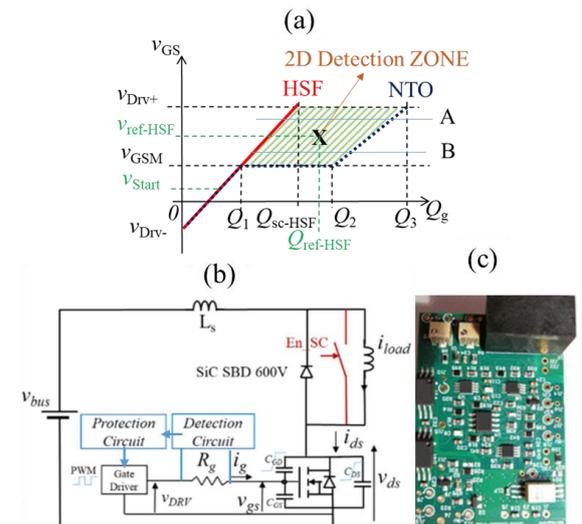


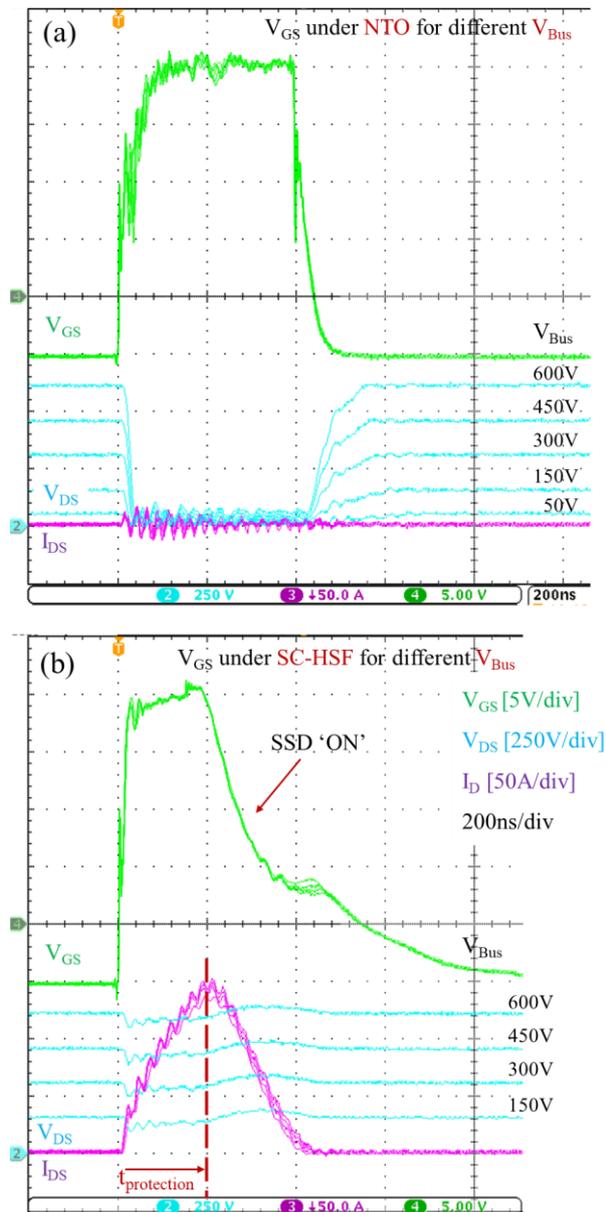
Fig.2. (a). Gate Charge characterization under NTO and HSF. (b). Circuit under test. L_S : Stray inductance. (c). view of the detection circuit, 3.5cm*5.3cm.

3. Robustness study under different parameters

3.1. V_{Bus} variation:

For the first robustness test, R_G is fixed at 10 Ω and V_{BUS} was increased with a 150V step towards 600V, as shown in Fig.3. As presented in Fig.3. (a) under

NTO, the device behaves normally with no interferences from the gate charge circuit. The drain current is around 15A (The current scale is big in order to be able to compare the waveforms under SC), and dV/dt is equal to 32V/ns. On the other hand, under SC-HSF the detection and protection are assured for different V_{Bus} . The protection time under 50V, 150V and 300V is around 171ns, where under 450V and 600V is around 158ns. One should note as well, that I_{SC-MAX} @ 600V is limited to 151A (68%) instead of 220A without any protection, as presented in fig.4, Tab.1. In order to illustrate the difference in gate charge amount under SC-HSF and NTO, Fig.5 is presented. The figure displays the image of V_{GS} , which represents the voltage V_{GS} adapted to 5V supply functions, therefore this voltage is compared with a reference level V_{Ref} higher than the Miller plateau. The figure presents as well the gate charge quantity under SC-HSF and NTO, and in order to differentiate between both operations a threshold level is set Q_{Ref} . This configuration set of the references will activate the detection.



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Fig. 3. Oscilloscope waveforms of the gate charge detection circuit with protection (a). under NTO. (b). under SC-HSF. @600V, $R_G=10\Omega$, $V_{Drv}=-5/20V$.

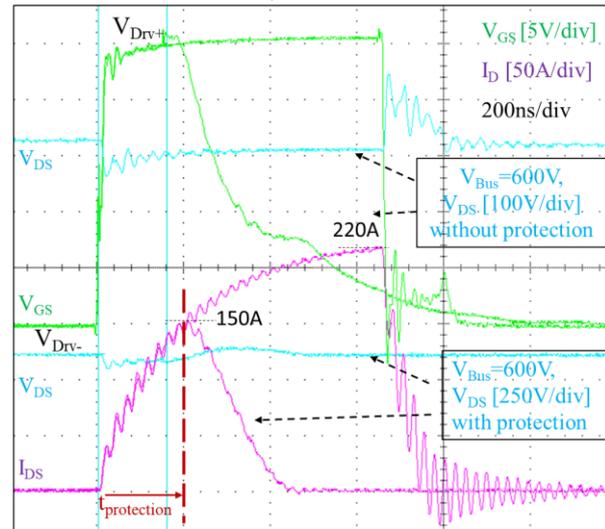


Fig. 4. Oscilloscope waveforms of the device under SC with and without protection. @600V, $R_G=10\Omega$, $V_{Drv}=-5/20V$.

Table 1. I_{SC-Max} under different V_{DS} .

V_{DS}	I_{SC-Max} without protection	I_{SC-Max} protection	Ratio %	Protection time
50V	133A	110A	82%	183ns
150V	180A	135A	75%	171ns
300V	202A	139A	69%	171ns
450V	213A	139A	65%	158ns
600V	220A	151A	68%	158ns

*Ratio%: $I_{SC-Max-Protection} / I_{SC-Max-Without-Protection} * 100$

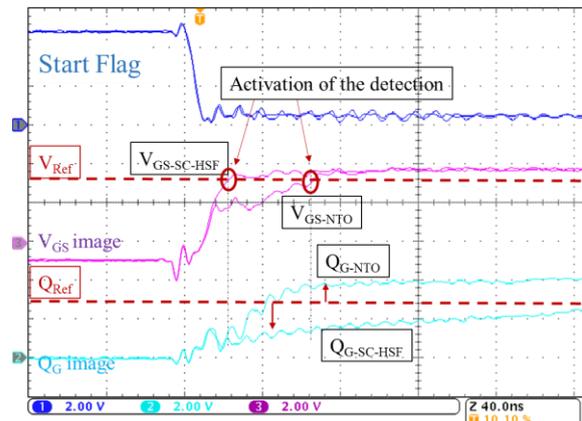


Fig.5. Integrator output "QG" under NTO and SC-HSF operation @600V, $R_G=10\Omega$, C2M0080120D, $V_{Drv}=-5/20V$, $I_{Load-NTO}=15A$.

3.2. I_{Load} variation: (robustness in normal operation: no unwanted detection)

In order to increase the drain current, the pulse is increased. The used test in this configuration is a double pulse method. As presented in Fig.6. the device does not show any false protection/detection. Different inductances have been tested as well. dV/dt at 600V decreases to 23V/ns. And the drain current

in the second pulse increases as well with the bus voltage increase: ($I_{D-Max}= 10A @50V$, $I_{D-Max}= 20A @150V$, $I_{D-Max}= 31A @300V$, $I_{D-Max}= 46A @450V$, $I_{D-Max}= 60A @600V$).

The evolution of the gate charge amount of the second pulse at different V_{Bus} is presented in Fig.7. The increase of the plateau Miller does not affect the detection: no unwanted detection appears that's confirm the global robustness in normal operation. Analytical Gate charge characteristics under different parameters variations are presented (fig.8, [16]) in order to support the study of fig.7.

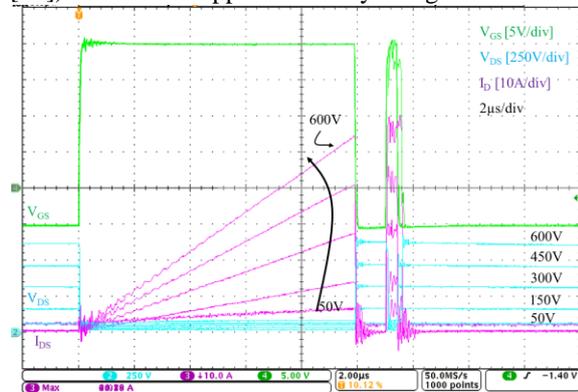


Fig.6. Oscilloscope waveforms under NTO, double pulse and different V_{Bus} . @600V, $R_G=10\Omega$, $V_{DrV}=-5/20V$.

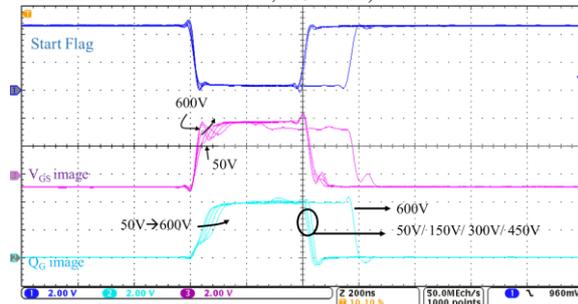


Fig.7. Q_G and the image of V_{GS} oscilloscope waveforms of the second pulse associated to Fig.6, different V_{Bus} & I_{Load} .

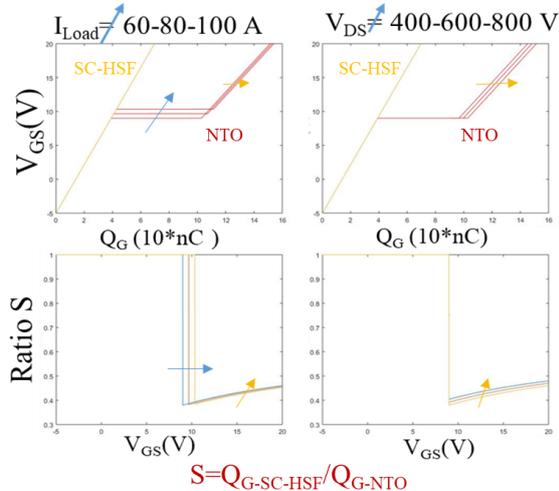


Fig.8. Analytical Gate charge characteristics under different parameters variations. [16]

3.3. R_G variation:

Fig.9. (a). presents oscilloscope waveforms from the power device side (V_{DS} , V_{GS} , I_D) at 600V under NTO

and SC-HSF using the same device 'C2M0080120D' with a different external gate resistor $R_G=5\Omega$ (previous tests have been led for $R_G=10\Omega$). And Fig.9. (b) illustrate oscilloscope waveforms from the gate charge circuit side, illustrating the gate charge amount and the image of V_{GS} .

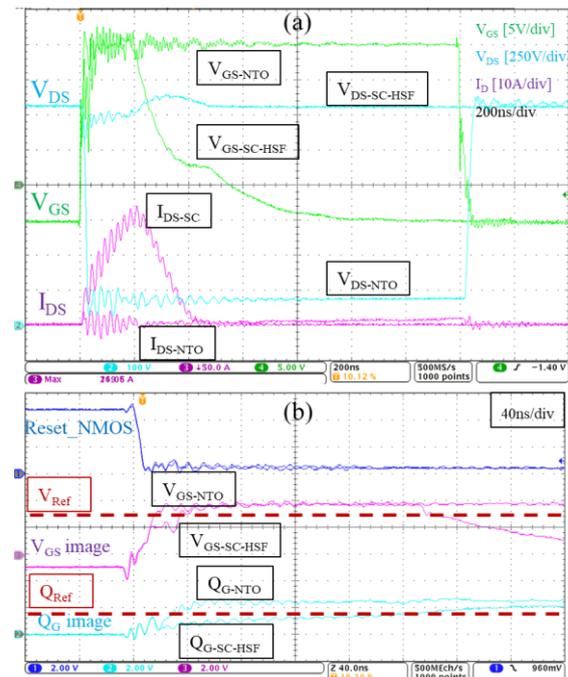


Fig.9. Oscilloscope waveforms under NTO and SC-HSF @600V, $R_G=5\Omega$, $V_{DrV}=-5/20V$.

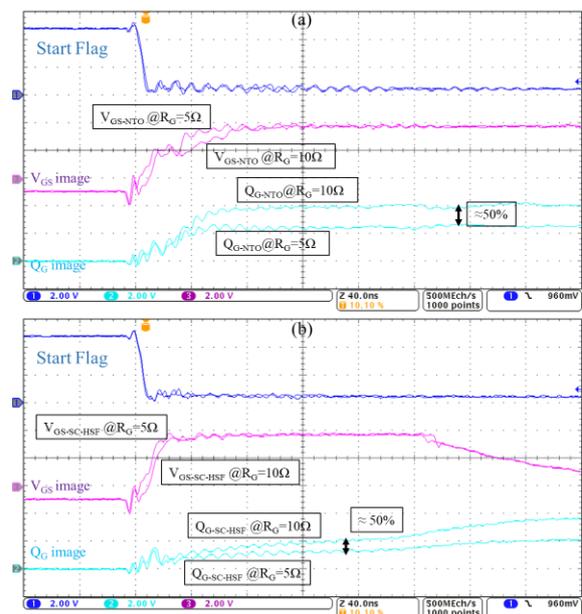


Fig.10. Oscilloscope waveforms comparison between $R_G=5\Omega$ and $R_G=10\Omega$ under (a). NTO (b). SC-HSF @600V, $V_{DrV}=-5/20V$.

As one can see the amount of the gate charge is reduced with the reduction of R_G . The reduction is proportional to the created split on R_G , which is around 50%. Mainly, the origin is due to the increase of the Miller plateau indirectly by he increases of dv/dt when R_G is decreased, which decreases the gate charge quantity when C_{iss} is max

and thus Q_{Total} is decreased. Fig.10. shows this respective proportionality between the gate resistor values under NTO (a) and SC-HSF(b). Using a gate resistor equal to 5Ω requires a new set of the gate charge threshold level $Q_{Ref}=1.5V.$, where, the previous Q_{Ref} is equal to $3V$ for $R_G=10\Omega$. Therefore, with the new reference set the detection circuit properly detect and protect the device under SC-HSF, and does not show any false triggering under NTO. The circuit shows robustness as well for different dV/dt , in this case $dV/dt=36V/ns$ @ $600V$. Different bus voltages have been tested as well with a 5Ω gate resistor.

3.4. Device generation variation:

Different devices have been studied in order to test the robustness of the method. In this section a 3rd generation device C3M0065090D is considered. Since the recommended gate to source voltage between both transistor of different generations (G2 & G3) differ, respectively $-5/20V$ and $-4/15V$, the reference level V_{Ref} should adapt for each generation (and not each transistor), Fig.11. Fig.12 presents the gate charge quantity under SC-HSF and NTO for both components (Gen.II) C2M00800120D device and (Gen.III) C3M0065090D device respectively, Fig.12.a and Fig.12.b. As one can see, the quantity under NTO and SC-HSF for each component is nearly proportional to 42%. The major difference between both component is the total gate charge and the input capacitance of the power device $C_{iss}=1.17nF$, $C_{iss}=0.76nF$ (-35%). Therefore, in order to safely protect the device and insure the detection, both references set (Q_{Ref} , V_{Ref}) should adapt. In this case Q_{Ref} can be set as well at $1.7V$, due the 50% proportionality between the input capacitances. And, V_{Ref} can be set at $2.7V$, instead of $3.3V$ for Gen.II.

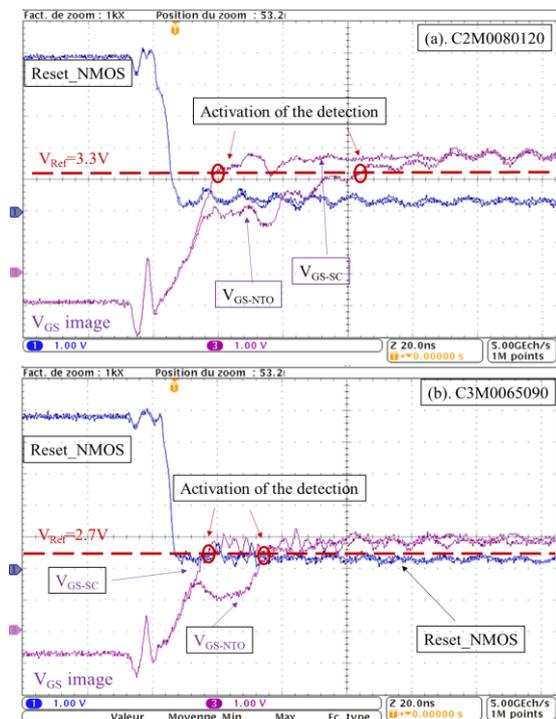


Fig.11. “V_{GS} image” under 400V NTO and SC-HSF Barazi *et al.* - 2021

operation for two power devices, (a). C2M0080120 $V_{Drv}=-5/20V$ (b).C3M0065090 $V_{Drv}=-4/18V$. @ $R_G=10\Omega$. [15].

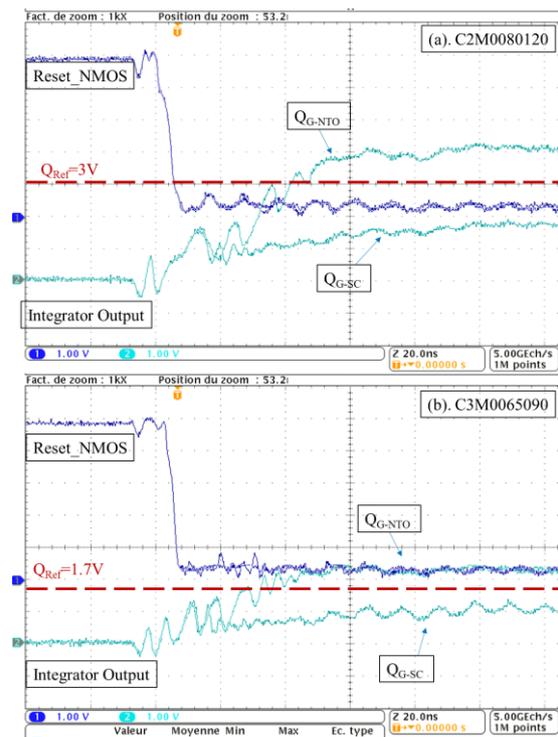


Fig.12.Integrator output “Q_G” under 400V NTO and SC-HSF for two power devices, a).C2M0080120 $V_{Drv}=-5/20V$ (b).C3M0065090 $V_{Drv}=-4/18V$. @ $R_G=10\Omega$. [15]

4. Discussion and analysis

After the detection of a SC fault, the SiC MOSFET must be turned off safely, to limit I_{DS} from increasing to a thermal stress point, as well as to avoid dangerous over-voltages. Therefore, to protect the circuit safely, a Soft Shut Down SSD system is included in the circuit. If the protection is not well designed it can lead to breakdown voltage by the total stray inductance due to high negative dI_{DS}/dt imposed by the transistor's channel dynamic, the protection should be soft to prevent this phenomenon. A high impedance (HZ) state is required before the activation of the SSD to avoid the driver to be short circuited by the SSD circuit. The observed plateau in the gate-source voltage V_{GS} under protection is due to the inductive effect through the kelvin inductance L_{SK} (parasitic inductance of package and terminal pin on PCB in the presence of a $di/dt < 0$).

The protection is activated between 150ns and 180ns depending on the test condition, limiting the drain current around 110A - 151A instead of respectively 130A - 220A. In such a short time and at such a low current value, the dynamic temperature of the chip remains lower than the melting temperature of the aluminum to metal of the die, which would allow a large number of repeated short circuits without ageing effect [17]. One should note that optimization can be realized in order to protect earlier and limiting the drain current to lower value, therefore reducing furthermore the physical and

thermal stress on the device.

The robustness of the circuit has been tested for several pulses, V_{DS} values, I_{load} values, R_G values and different components. Detection at lower bus voltages is more critical between SC-HSF and NTO, where the circuit showed high performances at 50V and lower.

Regarding the gate side variation, a different threshold set is required for values higher than 50% of the defined gate charge amount. On the other hand, one can set a trade-off between the integrator capacitor/resistor (C_1/R_1) and the gate resistor/gate input capacitance of the device (R_G/C_{Eq}). Fig.13. presents a 3D plot of the output of the integrator, V_{Out} , under different variation, where this trade-off can be met. On the figure, two representative equivalent capacitors define a plateau of C_1/R_1 choices. The equivalent capacitors represent the input capacitance of the power device under NTO and SC-HSF. Since the gate charge amount ratio under NTO and SC-HSF is 50%, the same ratio is respected for the equivalent capacitors. Therefore, the one can easily define the threshold set Q_{Ref} in order to differentiate between NTO and SC-HSF gate charge amount. As well, one can define different family sets for the gate variations (Gate resistor, input capacitance) in order to have a programmable threshold level set.

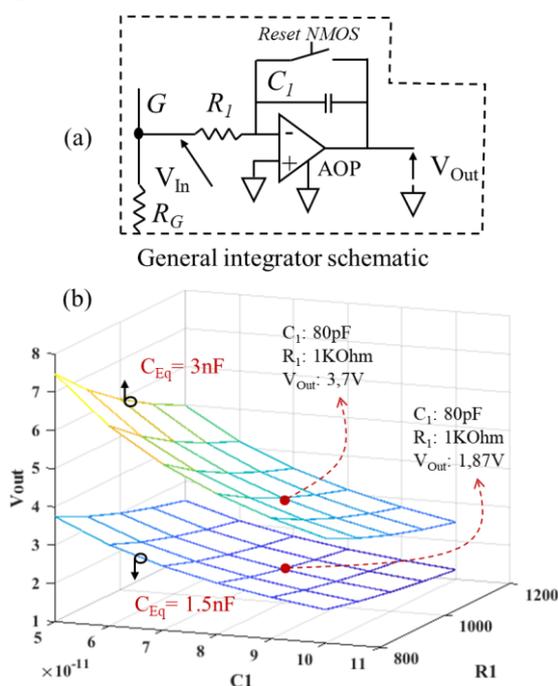


Fig.13. (a). Basic integrator schematic (b). 3D plot of the integrator output V_{Out} under different variation. [16], with $R_1 \gg R_G$ & $C_1 \gg C_{Stray}$

5. Conclusion

2D diagnosis once again proves it is the perfect candidate for fast short-circuit detection and protection. The original gate-charge method (2D diagnosis) detects as fast as possible the behavior of the circuit, within 155ns. High robustness have been observed for main parameters variations. Moreover,

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the detection circuit can be further optimized and the delays can be strongly reduced. At the end, the goal is to integrate all the functions in a dedicated gate driver. Avoiding the drain side of the device facilitate the integration of the detection method within the gate driver. A programmable reference set should be carefully designed.

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