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Introducing 3-nm Nano-Sheet FET technology in Microwind

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Abstract: This paper describes the implementation of the novel Nano-sheet FET (NS-FET) for the 3-nm CMOS technology node in Microwind. After a general presentation of the electronic market and the roadmap to the atomic scale, design rules and basic metrics for the 3-nm node are presented. Concepts related to the design of NS-FET and design for manufacturing are also described. The performances of a ring oscillator, basic cells, sequential cells and a 6-transistor RAM memory are also analyzed.

Keywords: Nano-Sheet, NSFET, CMOS design, 3-nm, Ring oscillator, interconnects, SRAM, logic gates

Introduction

Manufacturing smaller circuits begets the integration of more complex components to comply with a demand for an increased operating frequency and reduced power consumption. Continuous advances in process fabrication are enabling a vision of future nodes such as 5, 3.5, 2 and 1.5 nm for the next decade, reinforced by prospective roadmaps from giant semiconductor foundries such as Intel, TSMC & Samsung. Through 9 application notes, we have tried to illustrate the increased performances of devices, specifically for the 14-nm, 7-nm nodes [Sicard 2017] and more recently the 5-nm node [Sicard & Trojman 2021].

Technology node	Year of introduction	Key Innovations	Application note
180nm	2000	Cu interconnect, MOS options, 6 metal layers	
130nm	2002	Low-k dielectric, 8 metal layers	
90nm	2003	SOI substrate	[Sicard2005]
65nm	2004	Strain silicon	[Sicard2006]
45nm	2008	2nd generation strain, 10 metal layers	[Sicard2008]
32nm	2010	High-K metal gate	[Sicard2010]
20nm	2013	Replacement metal gate, Double patterning, 12 metal layers	[Sicard2014]
14nm	2015	FinFET	[Sicard2017]
10nm	2017	FinFET, double patterning	[Sicard2017]
7nm	2019	FinFET, quadruple patterning	[Sicard2017]
5nm	2020	FinFET enhancement, EUV	[Sicard2021]
3nm	2021	Nano-Sheet FET, EUV	This application note
20A	2023	Nano-Sheet FET, buried supply	
15A	2025	3D NS-FET, n/p co-engineering	

Table 1: Most significant technology nodes over the past 20 years and prospective vision for 2023-2027

Two major silicon foundries, namely TSMC from Taiwan and Samsung from South-Korea have introduced 3-nm technologies in 2021, one of them implementing the novel nano-sheet approach, considered to be the successor of the FinFET, first introduced by Intel for its 22-nm technology. In this application note, we describe the main characteristics of the 3-nm node, by exploiting available scientific literature and information released by semiconductor manufacturers, with focus on the Nano-Sheet FET. We take the opportunity of this publication to outline the electronic market growth, the motivation for 3-nm process. Then, we review the basic design rules, describe the transistor characteristics, and detail the implementation of basic cells such as the inverter, the ring oscillator, and the static memory. We conclude this document by discussing the switching performances of this node. We recall in table 1 the main innovations over the past recent years.

Moving to nanosheet FETs varies depending on the foundries, a situation somehow similar to the transition from MosFET to FinFET initiated by Intel in 2011, soon followed by other major silicon companies. Samsung has announced it would introduce nanosheets for its new 3-nm process, with a mass production starting in 2022. In contrast, TSMC has announced it would extend the FinFET to 3-nm node, and then move to nanosheet starting 20-Angstrom node (20A or 2nm), around 2025. From its side, INTEL has announced that its Intel 3 process would use while Intel 20A (A for “Angstrom”) would use its own version of nano-sheet FET named RibbonFET starting 2024 [Intel2021].

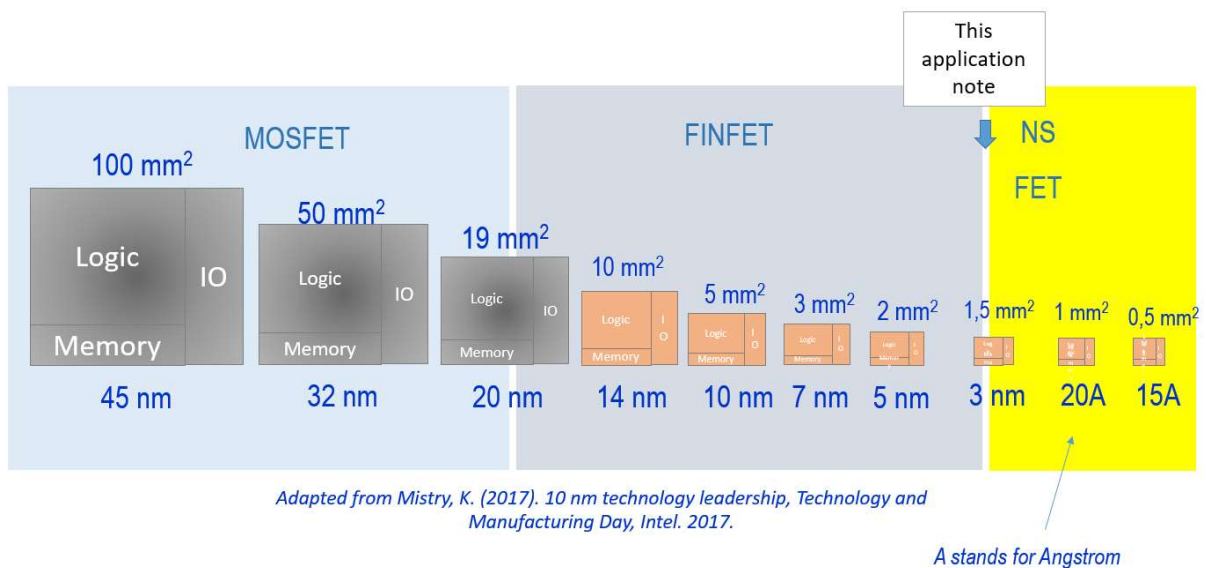


Figure 1 : The processor die size has been reduced over the past node generations

As shown in figure 1, the processor die size has been steadily reduced over the past node generations. The same trend towards silicon surface reduction is anticipated for the next upcoming nodes. The main reason for introducing the Nano-Sheet (NS) FET is related to this quest for a more efficient device in a smaller area. The device has been called Gate-All-Around (GAA), Muti-Bridge-Channel (MCB) or RibbonFET depending on the manufacturers & researchers, but the principles for stacking channels fully surrounded by the gate is the same for all devices.

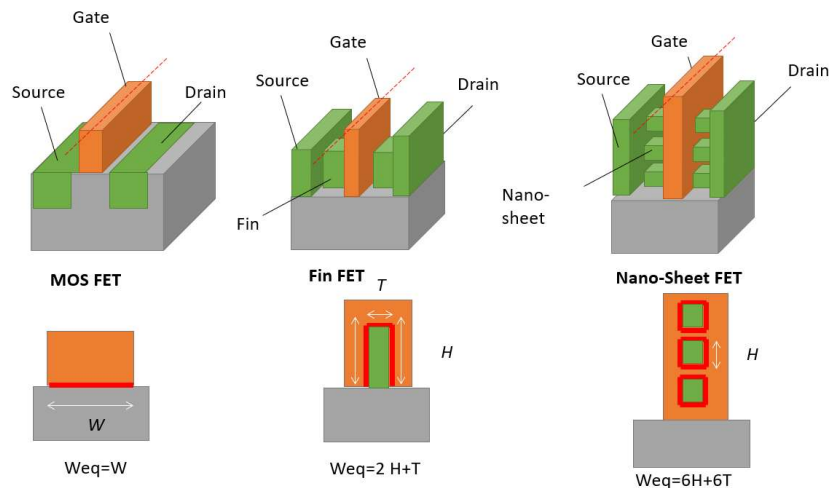


Figure 2 : MosFET, FinFET & Nano-Sheet FET, with corresponding equivalent channel width

It can be seen from Figure 2 that within a reduced silicon surface, process engineers have been able to fabricate much more efficient devices than the original MosFET, mainly in terms of equivalent channel width (W) that is nearly proportional to the switching current. Stacking nano sheets enable an equivalent channel width more than 3 times more area-efficient than the MosFET, in its 3 stacked nano-sheet configuration.

Introduction of Nano-Sheet FET in industry

The adoption of nano-sheet FET should follow the adoption of FinFET with a 10-years shift. Is it anticipated that the 3-nm node will announce the start of a migration from FinFET to NsFET, to enable further gains in current drive while reducing the device surface, thus enabling smaller, faster and more energy-efficient chips (Figure 3). The three different categories of applications should remain: high performance computing (servers, data centers), general purpose (laptops, gaming), and low power (mobile, IoT) with significant differences in terms of acceptable leakage current (IOFF).

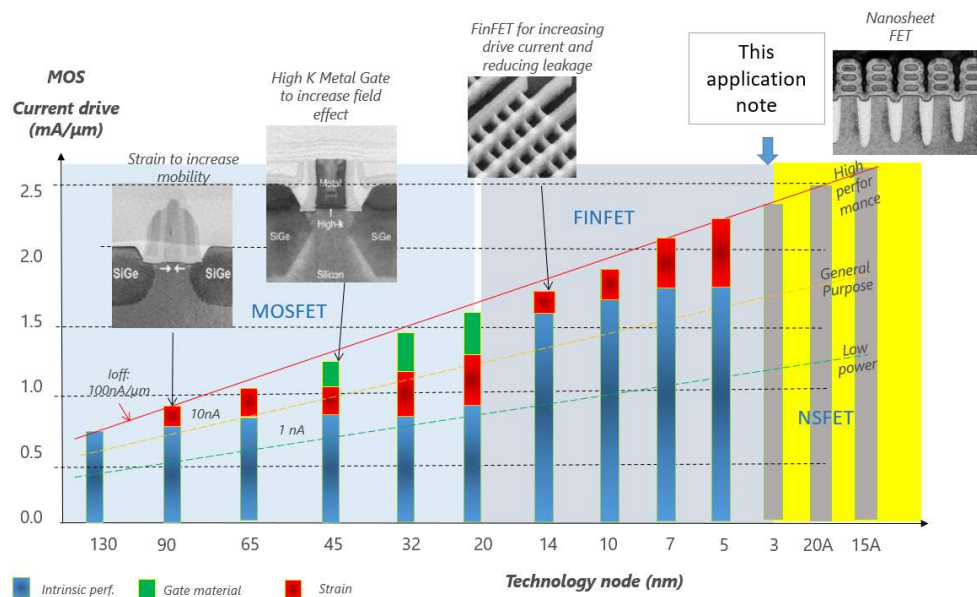


Figure 3 : Increased current drive over 13 technology nodes including MosFET, FinFET & Nano-Sheet FET

The demonstration of the full control of the channel was originally published by [Sung-Young Lee 2004] from Samsung, who described a “novel multi-bridge-channel MOSFET (MBCFET) with extremely high performance”. However, the true industrial adoption of this novel device was shifted nearly 20 years after this publication. In more details, the industrial deployment is scheduled by Samsung for 3GAP node (an acronym which could stand for 3-nm Gate All Around – Production) in 2023. Two other IC suppliers should follow: TSMC for its future 2-nm “2N” node, with a device named Gate-All-Around FET (GAA), and Intel for its 2-nm “20A” node, with a device called RibbonFET [Intel 2021].

COMPANY	NANO-SHEET DEVICE NAME	TECHNOLOGY NODE	YEAR OF INTRODUCTION
SAMSUNG	Multi Bridge Channel FET (MBCFET)	3-nm (3GAP)	2023
TSMC	Gate-all-around FETs (GAAFETs) a	2-nm (2N)	2024
INTEL	RibbonFET	2-nm (20A)	2024

Table 1 : Introduction of the Nano-Sheet FET according to 3 semiconductor giants Samsung, TSMC & Intel

Limited scale down

One simple rule that drove the semiconductor industry over the past 40 years was to associate (at least in a first-order approximation) the technology with the minimum feature size. For example, in 90-nm technology, the narrowest feature such as the MOS gate was around 90 nm. Starting 32-nm node, the manufacturing of nano-scale patterns became so challenging that advanced patterning failed to enable further linear scaling. Therefore, the node generation could not be linked anymore with the minimum feature size. For example, concerning the 3-nm node, the minimum feature size is around 8-10 nm, that is nearly 3 times larger than what the node number would mean (Figure 4).

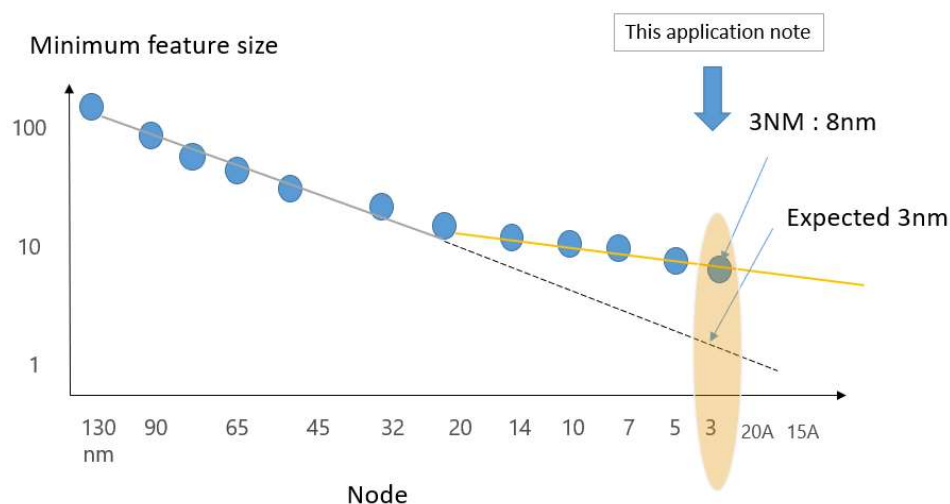


Figure 4 : Saturation effect in the technology scale down, the minimum feature size is no more related to the technology number

Improving performances by all means

Improving the performances in a significant manner at each new node generation is enabled by gaining silicon space, improving speed and saving power. As a significant shrink of the features is no more feasible, time has come to shrink the cell size by design, improve the device, and reduce parasitic capacitance & resistance, therefore improving speed and/or reducing power.

Reducing the cell height

The concept of cell height reduction with nearly no change of the cell width is illustrated in Figure 5 [Weckx 2019]. The “Contacted Gate Pitch” (CGP) refers to the distance between 2 active gates, and this distance is the hardest to reduce from 14-nm (N14) to 2-nm (N2) node. It can be seen that no significant gain may be expected in terms of distance between vertical gates (in red in the figure, an heritage of the good old polysilicon that appeared light red in the microscope). In other words, the cell width cannot be shrunk significantly.

In contrast, the vertical dimension of the cell may be significantly reduced by replacing the FinFET by the Nano-sheet FET, which is more compact, and placing N & P devices closer to each other thanks to the suppression of n-well design rule constraints. In the future, replacing the power metal tracks by buried power rails would restore horizontal routing channels, a strategy already announced by Intel for node 20A (2-nm, 2024) and referred as PowerVia™ [Intel2021].

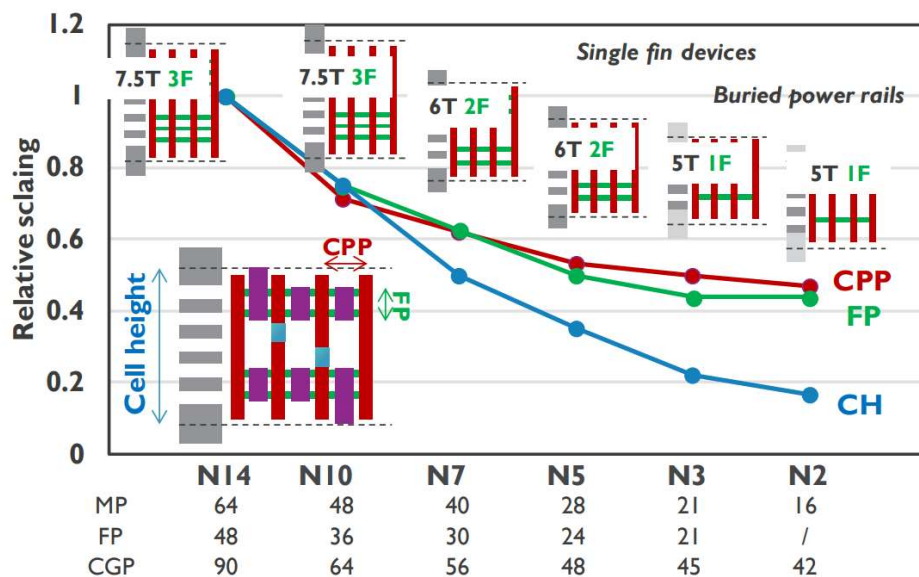


Figure 5: Illustration of the limited contacted gate pitch scale down over the 14-nm to 2-nm node generations, and the aggressive scale down of the cell vertical dimension (7.5T to 5T) [Weckx 2019]

Improving Area Efficiency

Replacing the FinFET by the Nano-sheet FET has many advantages: the device is smaller for an equivalent current, the distance between N & P devices can be reduced as no n-well and no polarization is required, the intra-cell interconnects are shorter and lead to a capacitance & resistance reduction, and the full control of the 4 sides of the channel gives better Ion/Ioff performances than FinFET or MosFET. Given a 1mA ION current, nano-sheet FET require 50% less silicon as compared to FinFET, which was already 30% more area-efficient than the MosFET (Figure 6). The major step forward should be to stack the p-device over the n-device to decrease the device surface by 75% [Wang 2021].

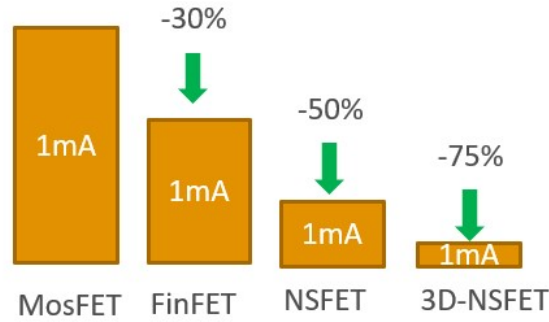


Figure 6: Illustration of silicon surface benefits using innovative devices such as FinFET, NsFET, and stacked N-P NsFET, for the same switching current.

The NsFET has a much more complex structure than the MosFET due to the stacking of nano-sheets. Instead of growing a single channel, a superlattice of alternating Si and SiGe layer must be formed, followed by the selective removal of the sacrificed SiGe layer. The empty space in between the Si channels must be filled with the gate dielectric (usually a combination of SiO₂, Si₃N₄ and high-K dielectric such as Hafnium oxide HfO₂) and metal gate that will completely surround the nanosheets.

Equivalent channel width

Knowing the width W and nanosheet thickness TNS , and the number of nanosheets ns , we can get the effective channel width W_{eff} using equation 1. The comparison between the NsFET (top) and MosFET (bottom) layouts with the same equivalent channel width and length is reported in Figure 7.

$$W_{eff} = ns \times (2W + 2TNS) \quad (\text{eq. 1})$$

The illustration of the improved switching performances is illustrated in figure 8. Considering the logic levels 0 and 1 ($0=V_{SS}=0V$, $1=V_{DD}=0.65V$), two important current values are often considered:

- IOFF (no channel but a parasitic leakage current)
- ION (maximum current at maximum gate voltage)

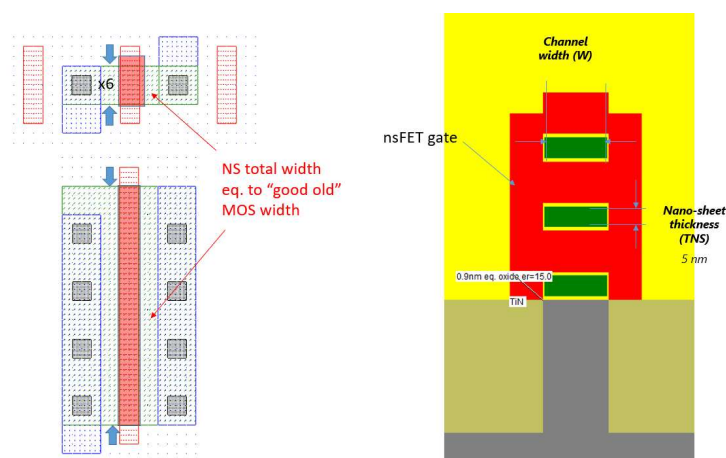


Figure 7: the equivalent channel width is more than 3 times the MOS width thanks to a 4-side control of the channel, leading to very small footprint

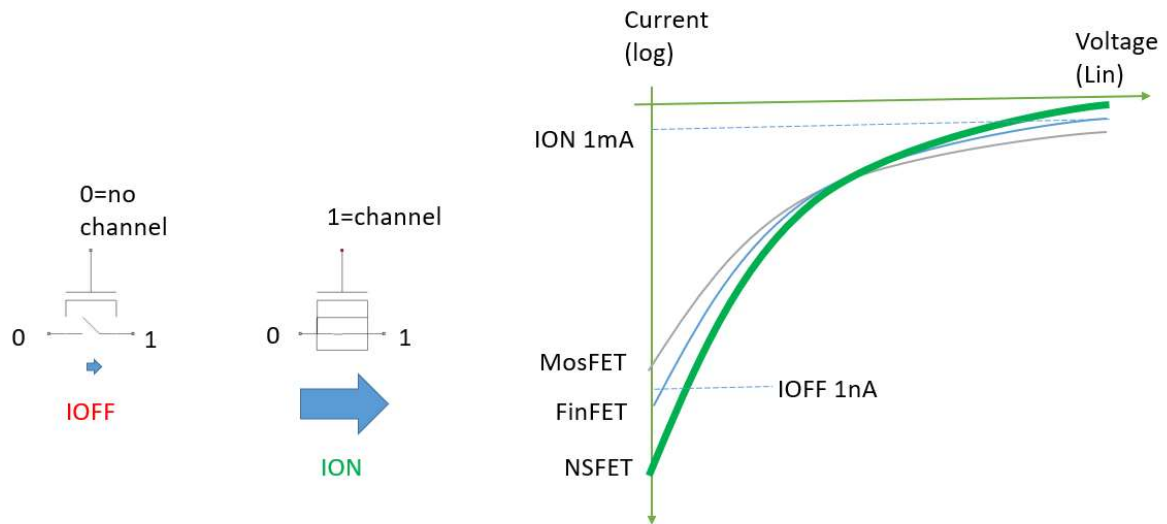


Figure 8: Comparing ION/IOFF trade-off for MosFET, FinFET, & NsFET

The ratio I_{ON}/I_{OFF} is around 10^6 . Given a $1\mu\text{m}$ width, I_{ON} is within the 1mA range, I_{OFF} the nA range. The successive introduction of FinFET and later on NsFET have improved or at least maintained a satisfactory I_{ON}/I_{OFF} ratio although the device dimensions have been drastically reduced. Some scientific publications define the current in $\text{mA}/\mu\text{m}$, some others refer to the device current itself.

Restoring the fine current tuning

One major drawback in the FinFET-based design is the discrete nature of fins, which do not give much choice for cell design: in the latest 5-nm FinFET technology [Sicard 2021], the choice was limited between 1 or 2 fins, 1 for the “slow” device (or high-density), and 2 fins for “fast” devices (or high performance). Still, more fins could be added for increased current capabilities, for large drivers or power amplifiers for example.

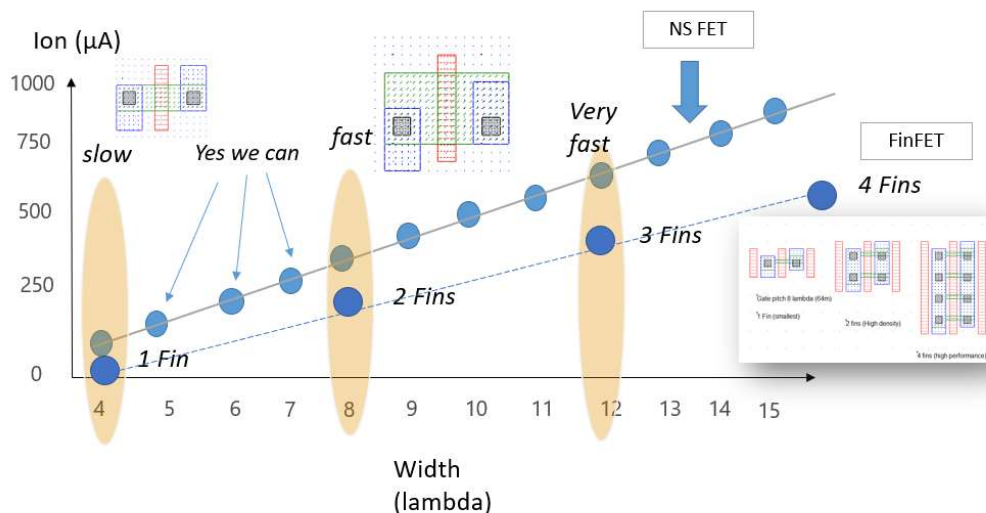


Figure 9: The discrete nature of fins limits the current tuning of FinFET, while the width of NsFET can be adjusted to the exact current needs

The continuous aspect of the NsFET restores the ability to adjust precisely the device I_{ON} according to the needs, which enable a more efficient design in terms of power consumption and speed, as compared to FinFET (Figure 9).

What about the supply

While the supply voltage has been steadily reduced from 0.35 μ m to 32-nm (3.3V down to 1V), the trend towards significant supply reducing is not valid anymore. What we observe from publications related for FinFET & NsFET is a saturation around 0.6-0.7 V (Figure 10).

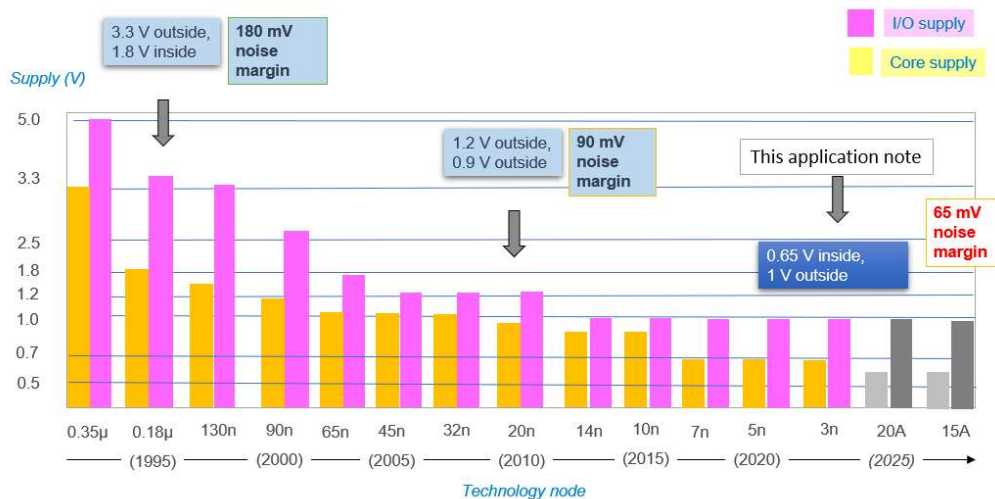


Figure 10: The supply voltage is around 0.7 V for 7-nm, 5-nm & 3-nm nodes

The end of n-well

No n-well layer is required anymore as the device channel is totally surrounded by the gate, without any influence of the substrate as for MosFET & FinFET. Therefore, no polarization is required too, which enables to place n & p devices much closer to each other than previous technologies. In Microwind's 3-nm implementation, the p-well layer is deactivated (Figure 11).

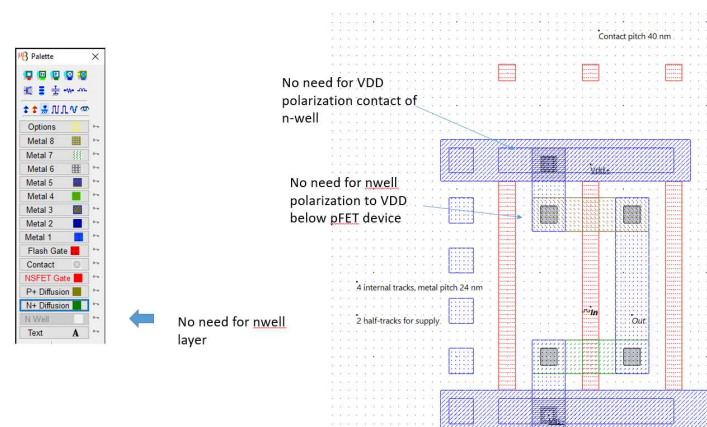


Figure 11: The 5-track implementation of the inverter do not include nwell layer nor associated polarization

A brief review of Nano-Sheet dimensions

We select 5 publications for which explicit values of the nanosheet FET dimensions are provided, as well as ION/IOFF performances. These parameters are listed in order to orient our own choices (last column of Table 2).

DESIGN PARAMETER	UNIT	[KIM 2021]	[WECKX 2019]	[DAS 2020]	[JEONG 2020]	[YOON 2020]	OUR CHOICE
DEVICE HEIGHT	nm	55	60	43	60	50	45
GATE LENGTH	nm	11	15	8, 10	12	12	8
NANOSHEET THICKNESS	nm	5	5	5	5	5	5
NANOSHEET SPACING	nm	10	10	5	10	10	10
NANOSHEET WIDTH	nm	24	13	20	42	26	16 (Slow) 32 (Fast)
NUMBER OF NANOSHEETS		3	4	4	3	3	3
VDD	V	0.7	0.7	0.6	0.7	0.7	0.65
IEFF NFET	μA	90 (LP)	70	20 (LP)	233 (HP)	30 (LP)	100 (LP-slow)
		180 (HP)		40 (Overdr)		60 (HP)	125 (HP-slow)
SUBTHRESOLD SLOPE	mV/Dec	70	75	60-70	100	n.a	60

Table 2: Comparing the device dimensions & electrical characteristics for a selection of scientific publications

Summary of design rules

Depending on the publications, the number of nano-sheets oscillate between 2 and 7 stacked layers. Until recently, Samsung & TSMC did not give much details on the physical dimensions of their nano-sheet device. We have chosen to define 3 stacked layers, which is the most common number used in scientific publications regarding nano-sheet devices involved in the 3-nm node.

DESIGN PARAMETER	UNIT	CODE	NAME IN RULE FILE	VALUE IN 3-NM PROCESS
LAMBDA	nm	λ	lambda	4.0
CORE SUPPLY	V	VDD	Vdd	0.65
DEVICE TYPE		NanoSheet	nsfet	3
WIDTH FAST	λ	W	nswhp	8
WIDTH SLOW	λ	W	nswlp	4
DEVICE HEIGHT	nm	HNS	thpoly	55
THICKNESS NS	nm	TNS	tns	5
SPACING NS	nm	TSP	tsp	10
NUMBER OF NS		NS	nsfet	3
GATE LENGTH	λ	GL	R302	2
GATE PITCH	nm	CGP	cgp	40
SPACER WIDTH	nm	SW		10
CONTACT SIZE	λ	CS	R401	2
EOT	nm	EOT	b4toxe	0.95
M1 WIDTH	λ		R501	3
M1 SPACING	λ		R502	3
METAL PITCH	nm	MP	R501+R502	24
METAL TRACKS		5T	tracks	4
RULE FILE				cmos3n.rul

Table 3: basic parameters of the 3-nm process implemented in Microwind (cmos3n.RUL)

Table 3 summarizes the main characteristics of the 3-nm design rules implemented in Microwind. The lambda unit is the same as for 7-nm & 5-nm node. VDD also remains at 0.65V. The number of nanosheets is defined as 4 stacked layers, with 5-nm thickness (TNS) and 10-nm spacing (TSP). The total device height is 60 nm. The number of nanosheets is defined in `cmos3n.rul` using parameter *nsfet*. Although any value between 1 and 7 is allowed, we assume the industry will use devices with 3 nanosheets. The nanosheet stack is constructed based on the nano-sheet thickness (*tns*) and the nano-sheet spacing (*tsp*). The layout of two versions of the nsFET, one in “slow” mode ($W=4\lambda$), the other in “fast” mode ($W=8\lambda$) is shown in Figure 12, with the associated cross-section showing the 3 stacked nano-sheets.

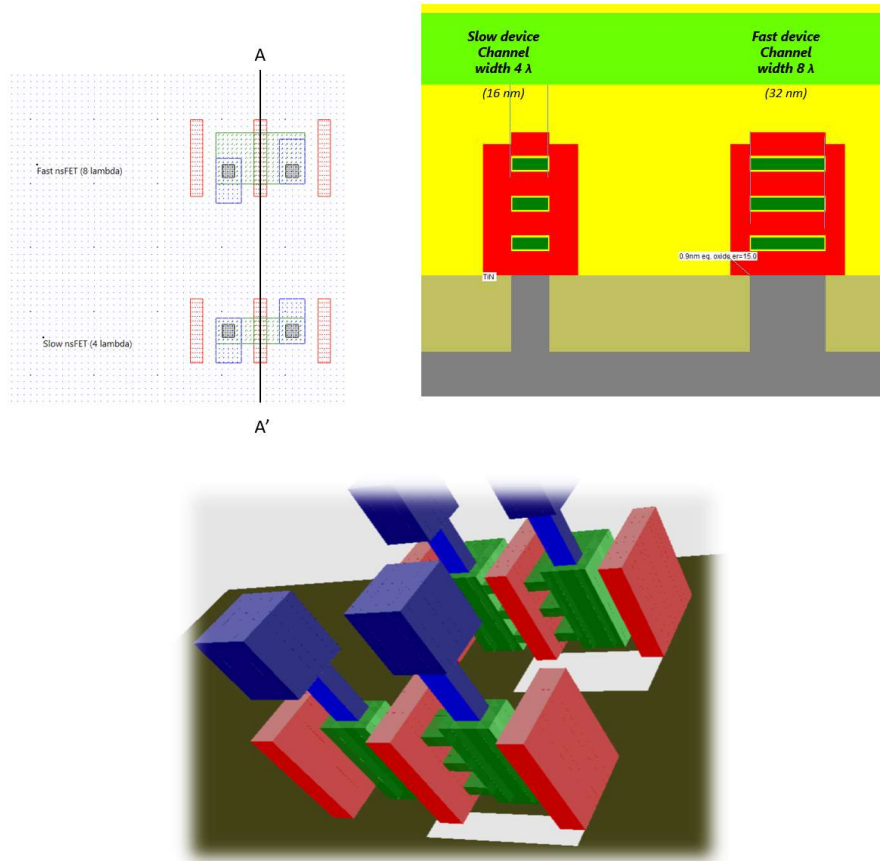


Figure 12: Slow and fast devices, layout view, cross-section & 3D view (*nsFET.msk*)

Nano-Sheet device

Layout design in Microwind uses integer units called lambda (λ). This strategy is not optimum in terms of silicon area but makes the layout nearly independent of the technology. Design rules have remained nearly the same for the past 30 years. In our 3-nm implementation, λ is kept at 4 nm, the same value as for 7-nm and 5-nm nodes. In other words, no scale down has occurred, the space, speed and consumption benefits come from design & device innovations.

The minimum channel length is 2λ as always, the contacted gate pitch (CGP) is 10λ (quite similar to FinFET & MosFET nodes), and the metal pitch (MP) is 6λ ($3+3$), same as always. In 3-nm technology, dummy gates are activated by default and added on both sides of the active device, with a gate pitch of around 10λ (40 nm). The default width is 4λ (16 nm). It corresponds to the slow speed. Notice that the effective width W_{eff} is much larger than W , as the effective channel is more than 6 times higher, according to eq. 1 seen previously.

nsFET Parameter	Slow	Fast
Width (W)	4 λ	8 λ
Length (L)	2 λ	2 λ

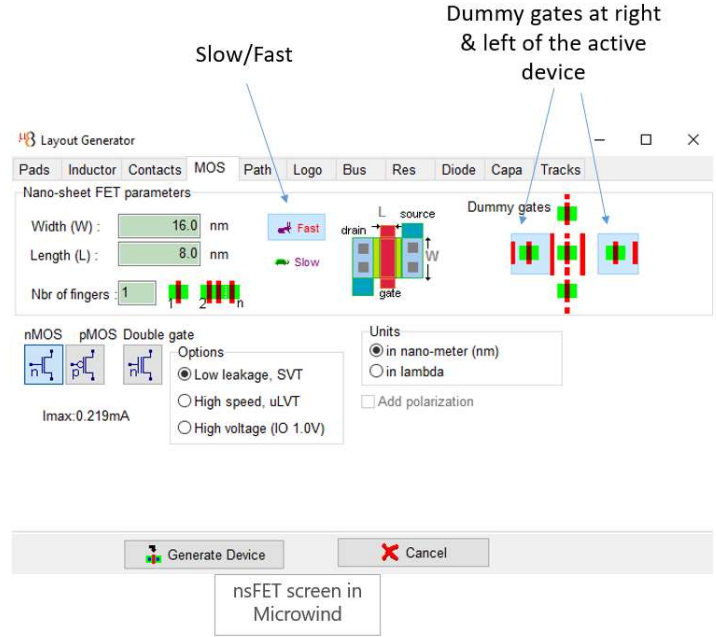


Figure 13: in 3-nm nano-sheet technology, dummy gates are selected, and the default width is 16nm (W_{eff} more than 6 times larger than W)

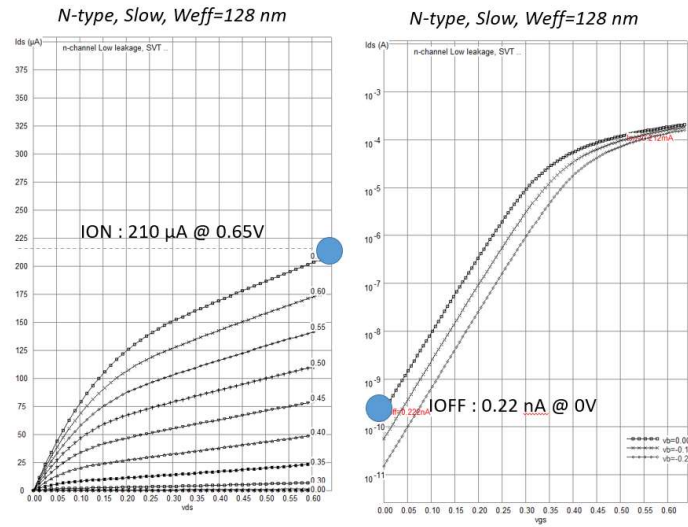


Figure 14: I_{ON}/I_{OFF} for the slow nsFET, n-type

The I_{ON} current for the slow device is around 210 μA (Figure 14) and corresponds to the maximum available current. Several authors prefer the I_{EFF} current defined by equation 2. In a first-order approximation, I_{EFF} is around $I_{ON}/2$ (86 μm for the slow nsFET).

$$I_{EFF} = \frac{I_{High} + I_{Low}}{2} \quad (\text{Eq. 2})$$

$$I_{High} = ID(V_g = \frac{V_{dd}}{2}, V_s = 0, V_d = V_{dd})$$

$$I_{Low} = ID(V_g = V_{dd}, V_s = 0, V_d = \frac{V_{dd}}{2})$$

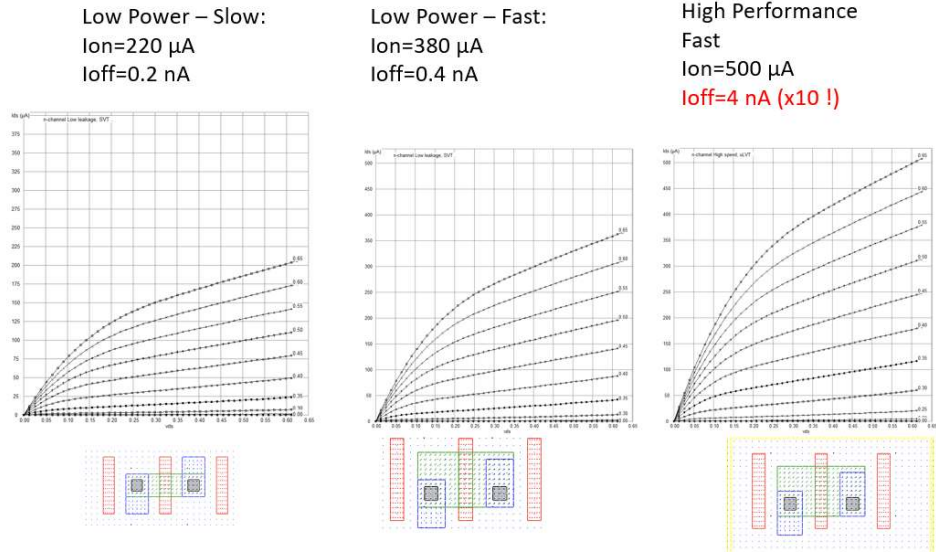


Figure 15: Comparing ID/VD curves for slow, fast and high-performance fast devices (nsFET.MSK)

The ID/VD curves of the slow and fast devices show an Ion current nearly double. Using the option layer, we may turn the device to high-performance mode for a supplementary boost of nearly 30% ION current, but at the cost of IOFF multiplied by 10 (Figure 15). The use of such device should be restricted to situations where the speed is critical (clock tree, critical logic path, needs for highest performances) and power saving is no more the priority.

In Nanosheet (NS) device architecture, it is much more challenging than FinFET or MosFET to provide multiple threshold voltage (multi-Vt) options for designer. Typically, low Vt devices are used for high performance, while high Vt devices are preferred for low power. Industrial processes usually propose up-to 4 different types of Vt to satisfy designer needs for optimized trade-off between speed and power consumption. For example [Cho 2016] from Samsung discussed the introduction of, sLVT, LVt, RVT, HVt variants of the same FinFET device in 10-nm technology, with Vt varying 200mV between the super-low and high-vt devices, thanks to adjustments in the thickness of metal layers used in the gate stack. Regarding NSFet, the metal gate boundary control is discussed by [Bao 2019] as a solution to enable multi-Vt devices.

In our 3-nm implementation of the NSFet, we may use either the High-Vt default device (Vt=0.30V), or the high-performance/low-Vt device (Vt=0.25V).

Modelling the NsFET

The reference model for simulating the Nano-Sheet FET is Berkeley BSIM-CMG, which stands for Common-Multi-Gate [BSIM-CMG 2021]. At the time of the writing of this application, BSIM-CMG 111.1 was not open source but BSIM-CMG 111.0 was available for download. Some details about the model may be found in [Dasgupta 2020]. It can be seen from Figure 16 that previous BSIM-CMG approaches were overestimating the drain current, whereas the updated model is able to capture the trend with high accuracy, matching measurements almost perfectly.

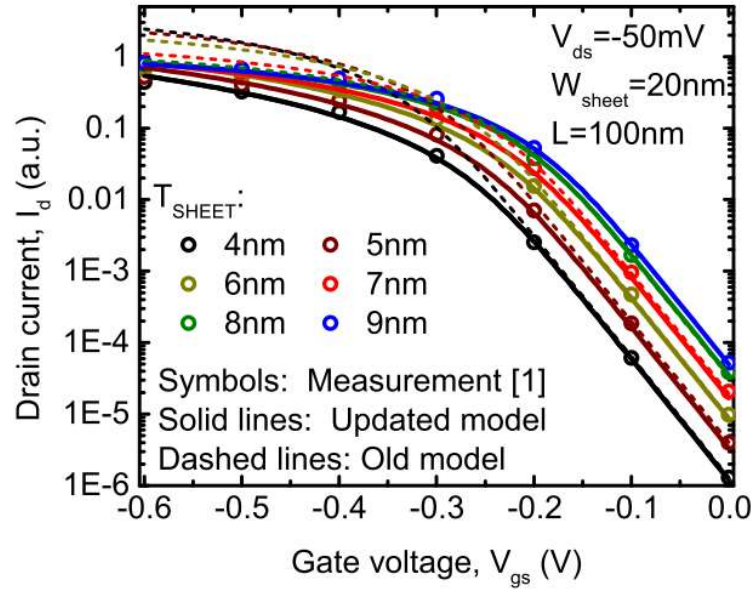


Figure 16: Measured drain current as a function of the gate voltage for nanosheet FETs with NS thickness varying from 9nm to 4nm. The updated model is able to capture the trend with high accuracy [Dasgupta 2020]

Microwind uses a simplified version of the BSIM4 model for simulating the Nanosheet FET, for the sake of simplicity (Figure 17). The simplified version of BSIM4 follows the main equations detailed in the book [Liu 2001]. The BSIM4 model was not initially targeted to FinFET nor double-gate/nano-sheet devices. However, it may fit in first order the I/V characteristics of advanced devices. Using BSIM4 model instead of BSIM-CMG may lead to significant mismatch between simulations and measurements, specifically for analog & radio-frequency designs, as BSIM4 suffers from some non-symmetrical equations, do not handle self-heating corrected in late versions such as BSIM6 [Agarwal 2013] & BSIM-CMG. Quantum effects are also ignored in BSIM4 models.

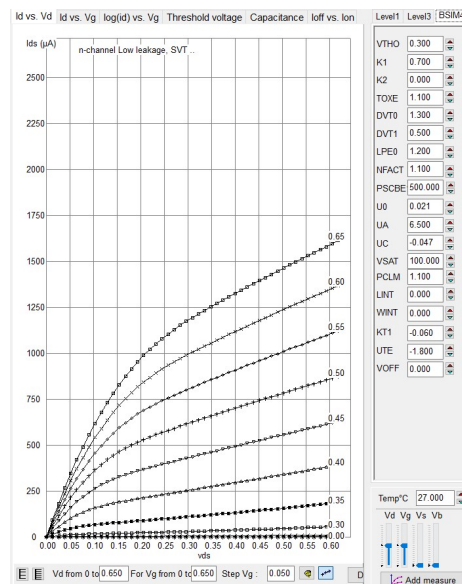



Figure 17: Simplified BSIM4 model implementation in Microwind used to simulate the 3-nm nanosheet devices

Getting Started with Nano-Sheet

Hand-made design of an inverter

1. Select the "NsFET Gate" layer in the palette window (Red).
2. Fix the first corner of the box with the mouse. While keeping the mouse button pressed, move the mouse to the opposite corner of the box. Release the button. This creates a narrow gate as shown in Figure 18. The box width should not be inferior to 2λ , which is the minimum and optimal thickness of the gate.
3. Select "N+ diffusion" by a click on the palette of the N+ Diffusion (Green).
4. Draw a n-diffusion box at the bottom of the drawing as in Figure 18. The N+ diffusion should have a minimum of 4λ height and extension both sides of the polysilicon gate. The intersection between N+ diffusion and gate is the channel of the N-device.
5. Select "P+ diffusion" by a click on the palette of the N+ Diffusion (Brown).
6. Draw a P+ diffusion box as shown in Figure 18. The intersection between diffusion and gate creates the channel of the P-device.
7. Select "Metal 1" and draw a box over the N+ & P+ area. Minimum width is 3λ
8. Select the icon "Connect layers" , click in the intersection N+/metal, and again in the intersection P+/metal.
9. Add VDD, VSS properties
10. Add a clock on the input gate
11. Add a "visible" property to the output (eye "Visible node")
12. Click "Simulate". Click "More" until you reach 1ns.

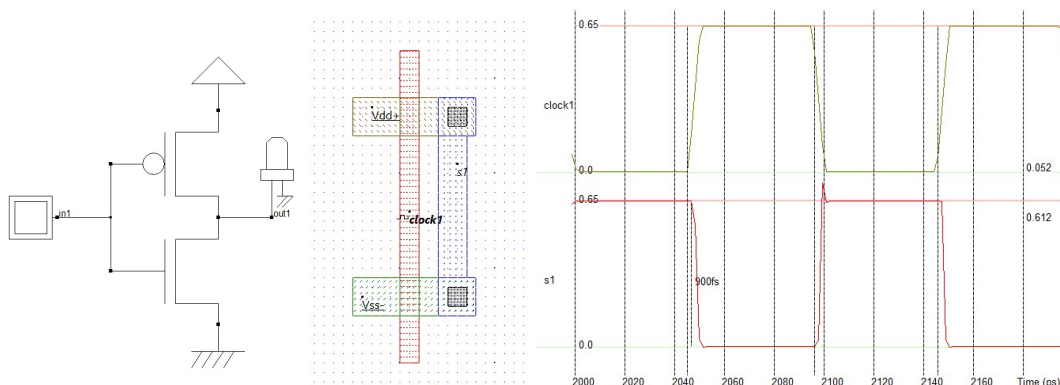


Figure 18: Steps to draw a simple inverter (mySimpleInverter.MSK)

Another approach to avoid design rule errors is to instantiate the n & p devices directly using the layout generator. Just click the device icon in the palette, the "Generate Device", place the component on the layout, and click again the same icon, but this time select "p-type", and place the component on top of the n-type device. Dummy gates are added by default for manufacturability purpose. The devices should be aligned. The minimum distance between N+ and P+ diffusions is 6λ . All gates should touch together in order to merge vertical layers in a regular way, as illustrated in Fig. 19.

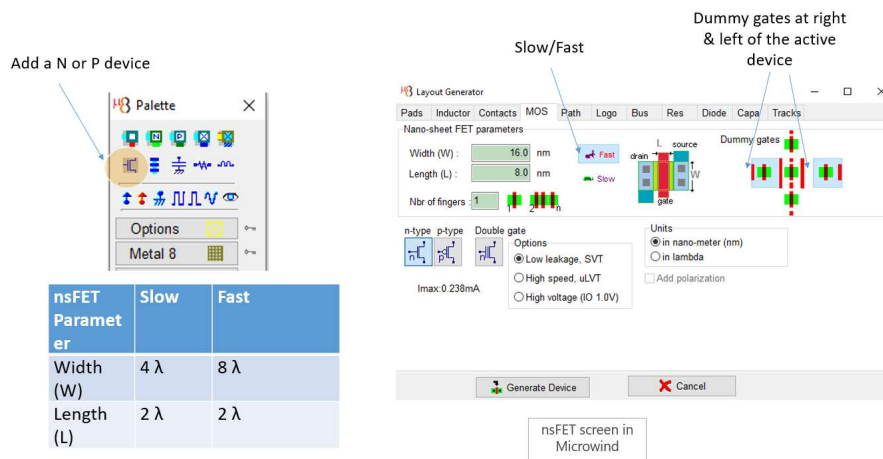


Figure 19: Select a n-channel or p-channel NsFET

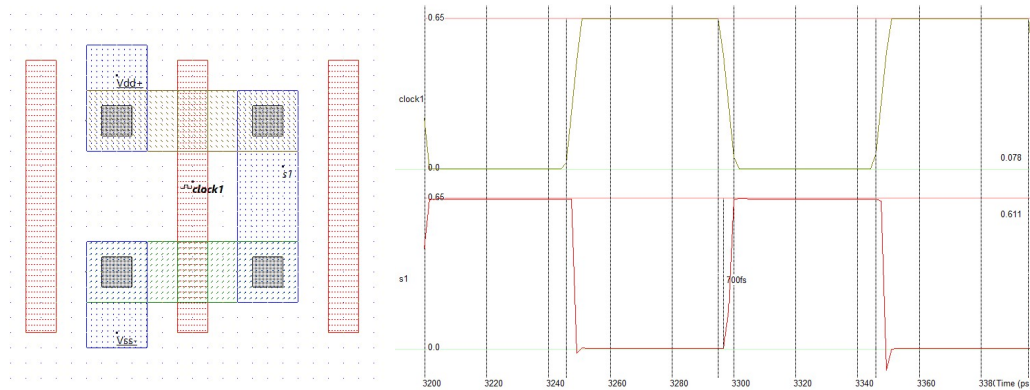



Figure 20: Creating an inverter with n-channel or p-channel NsFet generated by Microwind.

The N & P devices use a 4 λ channel footprint, which corresponds to the “slow” design style. The nano-sheet cross section can be displayed using the icon  with a vertical selection corresponding to the active gate (A-A’). The 3 stacked nano-sheets appear (Figure 21), each with a thickness of 5 nm and spacing of 10 nm.

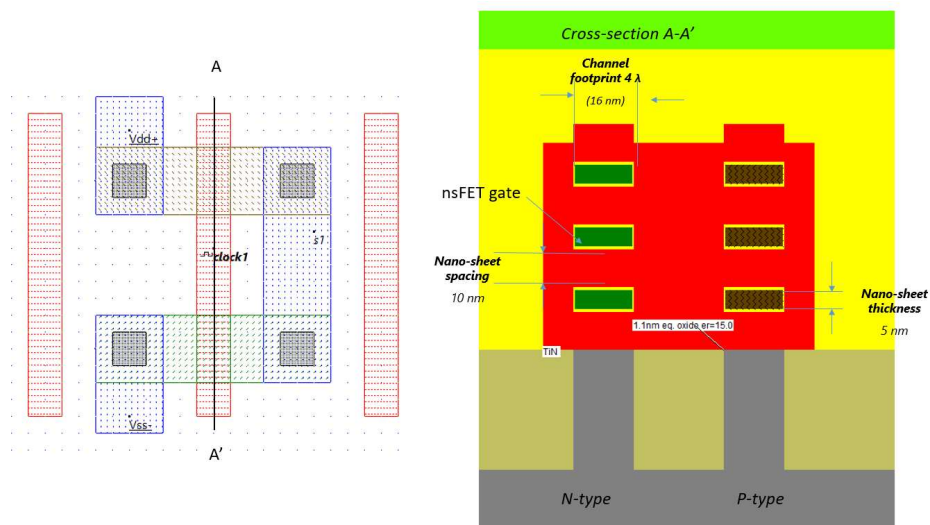


Figure 21: Cross-section of the n-channel or p-channel NsFET generated by Microwind.

The equivalent channel width W_{eff} is

$$W_{eff} = ns \times (2W + 2TNS) = 3 \times (2 \times 16 + 2 \times 5) = 126 \text{ nm}$$

where ns is the number of nano-sheets, W is the channel footprint and TNS the nano-sheet thickness.

Designing using 5T approach

Most publications related to 3-nm design refer to so-called 5T design where “T” stands for “horizontal metal tracks” [Mokuta 2018][Kim 2021]. The higher the number of “T”, the taller the cell. The value of T is equal for the metal pitch Metal Pitch (MP) which is around 24 nm in 3-nm technology (3 λ minimum metal width, 3 λ minimum spacing). The “T” concept is illustrated by [Kim 2021] with a cell height reduced from 168 nm (6T with 5-nm design rules) to 120 nm (5T with 3-nm design rules), as shown in Figure 22.

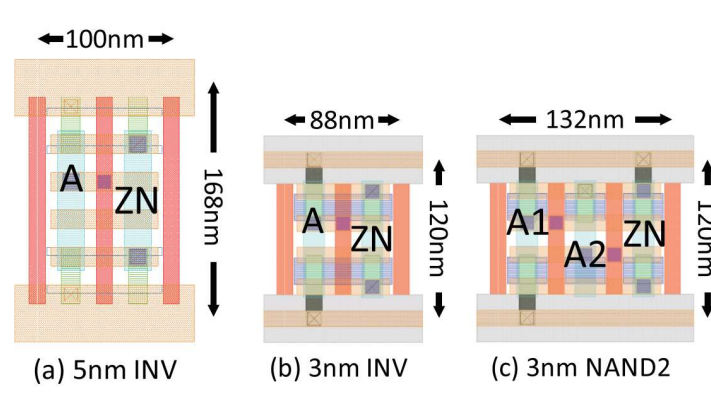


Figure 22: comparing the design of a 5-nm Inverter with 50nm contacted gate pitch (CPP), 6T and the 3-nm INV with 44nm CPP with 5T approach [Kim 2021]

When adding an upper metal track for VDD supply, and a the lower track for VSS supply, we must ensure there is enough room for 4 intermediate metal tracks for horizontal routing. The VDD and VSS tracks are shared with upper and lower cells, so supply tracks account for half track each. In sum, this design style is called “5T design”. In Microwind, it corresponds to 124 nm cell height (31 λ) and 80 nm cell width for an inverter. There is enough space to enlarge the device width for a faster switching (so-called fast design, with twice more device surface), as shown in Figure 23-right.

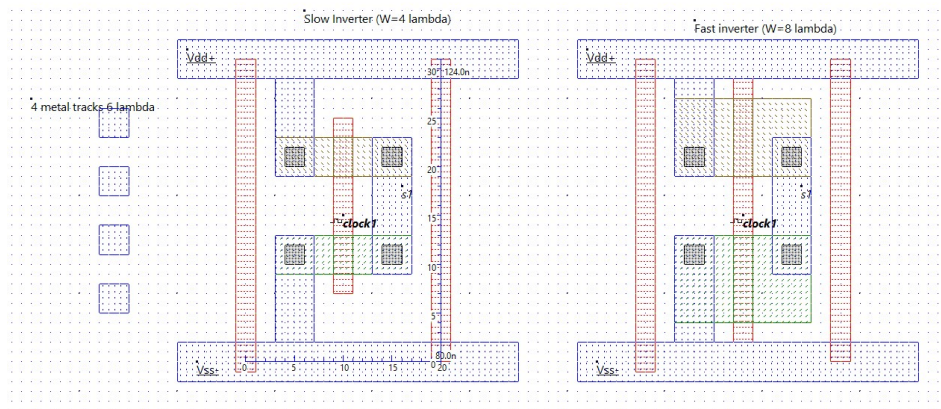


Figure 23: Adding the VDD & VSS power rails in a 5T strategy, leading to a cell height of 120 nm, slow & fast inverters

Compile one inverter, 5T

Microwind includes a specific tool to handle the generation of a complete inverter. Other simple logic cells such as NAND, NOR, AND, OR can also be generated using this tool. The cell height corresponds to the “5T” approach. The device width can be either “Slow” (4λ footprint) or “Fast” (8λ). An example of three compiled inverters is reported in Figure 24. Each new cell is added at the right side of the existing layout.

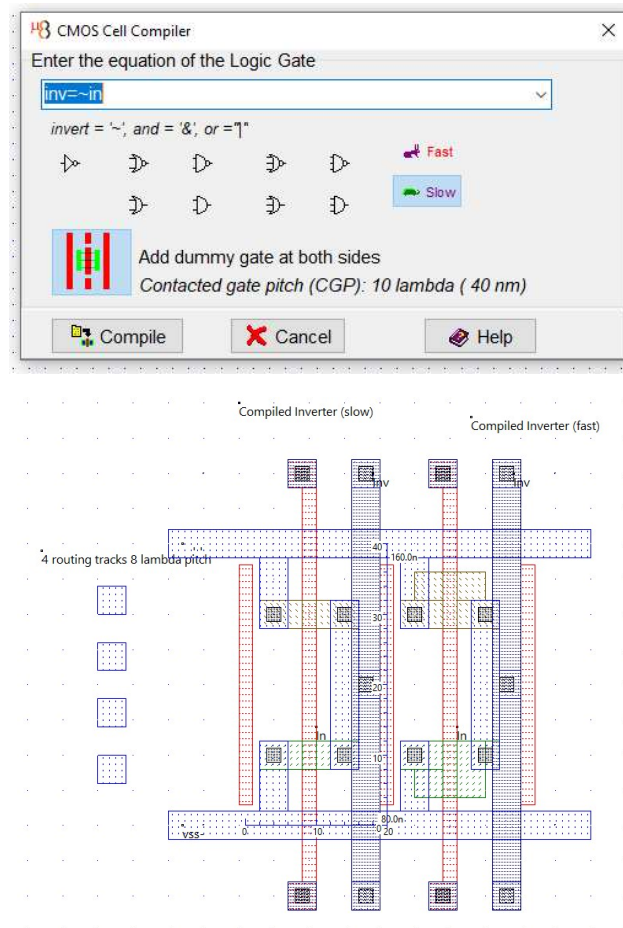


Figure 24: Two versions of the compiled inverter: slow at left, fast at right (invCompiled-Slow-Fast.MSK)

A closer look at the compiled layout reveals that the cell height is a little taller than expected. This is due to the internal routing strategy that does not rely on minimum width, minimum pitch (6λ) but uses instead relaxed metal pitch of 8λ , that simplifies the addition of contacts, but is not optimal. The cell height is 160 nm instead of 124 nm that is found in optimized 5T design (Figure 24).

Logic Design with Nano-Sheet

Ring Oscillator

Compiling 3 successive inverters enables to build a ring oscillator, that oscillates freely, without any external stimulation. The only work to do is to build the interconnections according to the schematic diagram shown below and to add the VSS and VDD supplies. The loading condition corresponds to the shortest possible wire and one single gate (the next input stage).

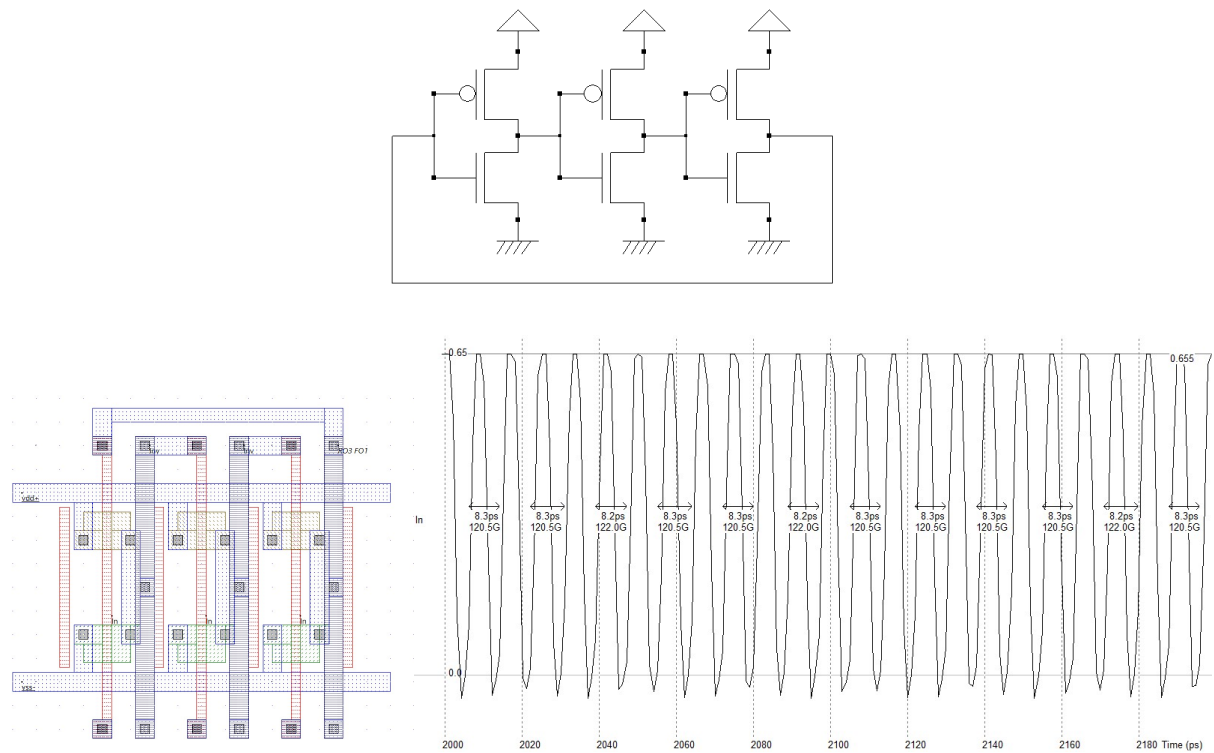


Figure 25: A simple 3-stage ring oscillator based on compiled inverters “Fast” mode (RO3-FO1-Fast.MSK)

The design corresponds to minimum parasitic resistance & capacitance, which corresponds to maximum performances. The observed frequency is approaching 120 GHz (Figure 25). Further boost may be obtained by enlarging the device width furthermore, or using the “high-speed” option, which is accessible using the option layer. Instead of the default “low leakage” option, we surround all 6 devices by as option layer and change the device option to “high speed”. The resulting simulation shows an oscillating frequency of 160 GHz.

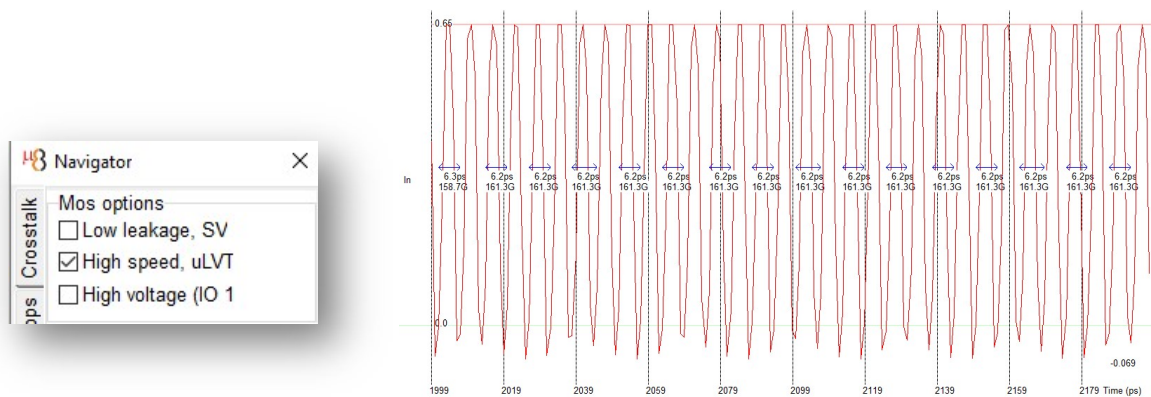


Figure 26: Turning the device option to “High-speed” increases the oscillating frequency to 160 GHz (RO3-FO1-Fast.MSK)

Ring Oscillator with Fan-Out

Many scientific publications include simulations of ring oscillators, such as [Wang 2020], [Ahmed 2020] or [Na 2021]. As the number of stages and operating conditions significantly vary among publications, direct comparison of the published results is not always possible. For example, [Na 201] uses 19 stages, each stage connected to M1, M2..M6 and then back to M1. In [Wang 2020], a 3-stage ring oscillator is used, each stage loaded by a metal track with a length corresponding to $25 \times (CGP + MP)$, where CGP is the contacted gate pitch (48 nm) and MP is the metal pitch (28 nm), which intends to represent typical loading conditions. Comparison are possible only if similar operating conditions are used (VDD, loading, options, device size) and if power & frequency per stage is evaluated, instead of the ring oscillator itself.

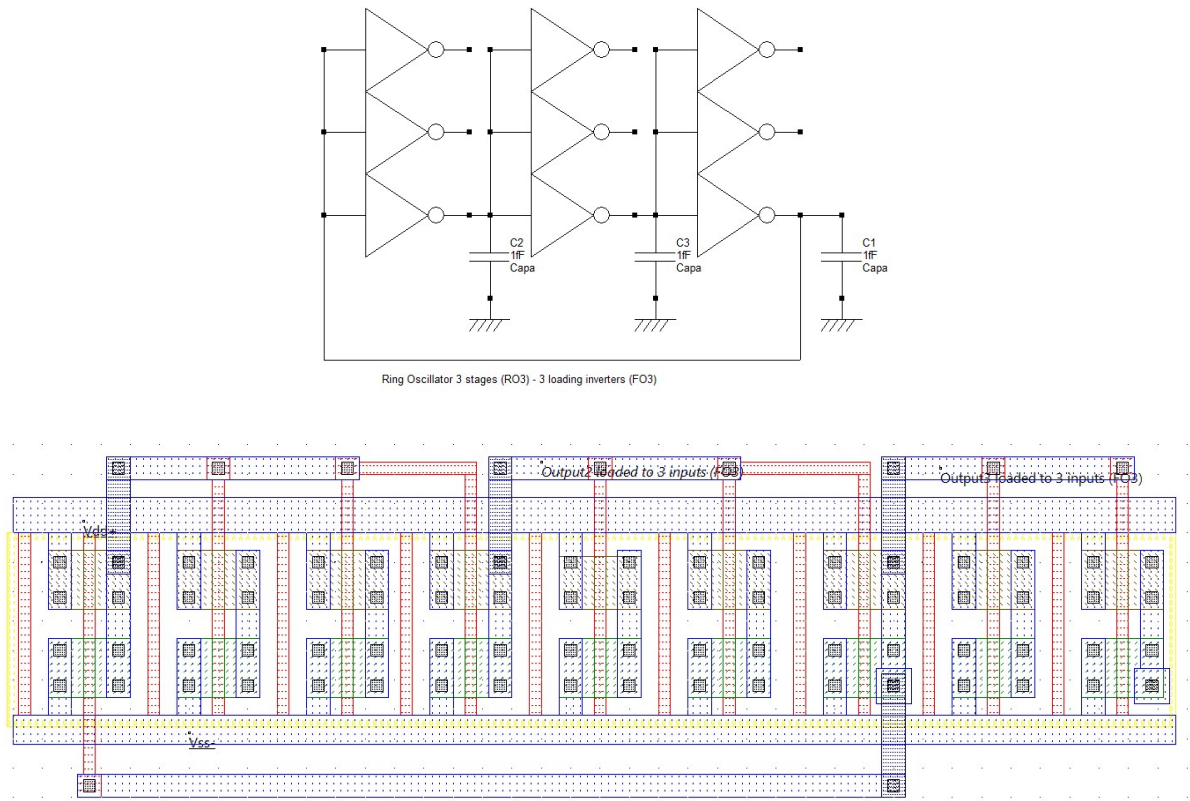
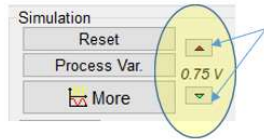
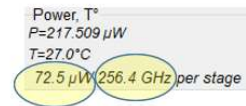


Figure 27: Each inverter output is connected to 3 inputs to emulate a significant load (RO3-FO3-Fast.MSK)

We use the following strategy for simulation: we consider a 3-stage RO with a 3-input load. This corresponds to a capacitance load around 1 fF (Figure 27). We extract the frequency per stage by multiplying the RO frequency by 3. We also extract the power per stage by dividing the total power consumption. In the following simulation, we use “fast” design approach and consider high-performance devices, instead of the default low power, to maximize the oscillating speed. Then, we iterate the simulation for VDD ranging from 0.5 to 0.8V, step 50 mV.



Modify VDD by step 50 mV



The power & frequency per stage

Figure 28: VDD may be increased/decreased 50 mV directly from the simulation menu. For ring oscillators, the power & frequency per stage appear below the evaluation of the total power

Figure 29 compares the performances of the Low-Power & High-Performance FinFET devices as published in [Sicard 2021] for VDD varying from 0.5 to 0.8 V. The circuit is a RO3-FO3 (3 stage, 3 connected inputs for each output). The same simulation performed in HP 3-nm NsFET shows improved speed at constant power consumption or reduced power consumption at constant speed, which demonstrates the benefits of the 3-nm technology. Further gains are expected for next generation 2-nm and 15A nodes.

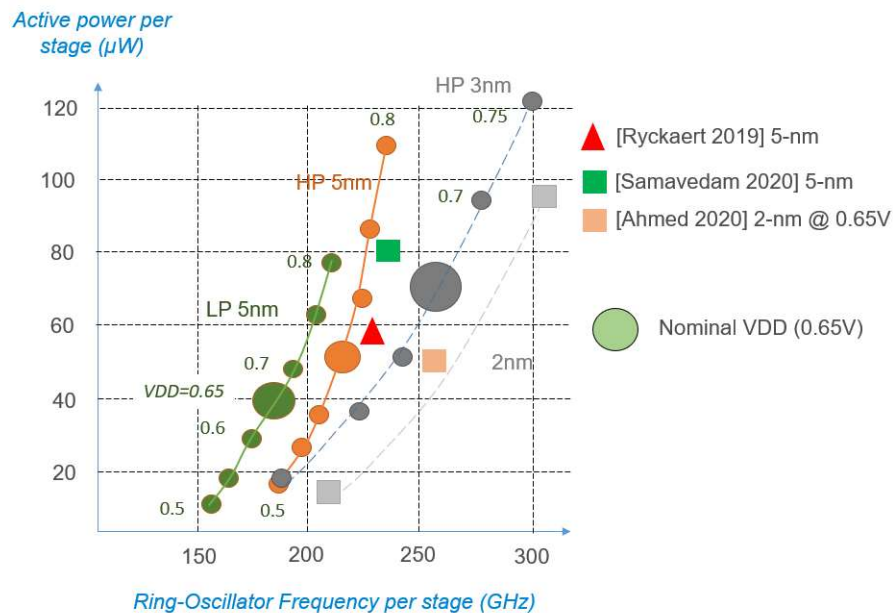


Figure 29: Comparing the power & frequency per stage of 3-stage RO with Fanout 3 in 5-nm FinFET & 3-nm NsFET ring oscillators

Basic cells

We use again the cell compiler to generate basic cells, namely the NAND, NOR, NAND3, OR3 and AND3 gates. The cells are placed horizontally with a regular CGP, and share the same VDD (top of the cells) and VSS (bottom of the cells, Figure 30). The A, B and C inputs have been merged to simulate the gate inputs simultaneously, thanks to M1/M2 routing and appropriate vias on the bottom. The simulation shows a delay ranging from 1 to 2 ps for unloaded Nand & Nor gates, and increased to 3-4 ps for unloaded AND & Or gates, due to the supplementary inverter stage (Figure 31).

Interconnect delay

All these delays are optimistic as no charge has been connected to the outputs, which are just floating. The connection of the outputs input gates through interconnects will be equivalent to a significant RC delay, which slows down the propagation. This is illustrated in figure 32: although the intrinsic delay is dominant for short & medium interconnects, the interconnect delay has a strong impact on the total switching delay for long interconnects. The metal resistance ranges between 500-1K $\Omega/\mu\text{m}$ [Wang 2020] [Seon 2021] according to authors and the metal capacitance is around 300aF/ μm . Although no significant gain is observed between fast and slow inverter designs for short & medium interconnects, fast inverters limit the overall delay as compared to slow inverters when long metal wires (4 μm and above) are used.

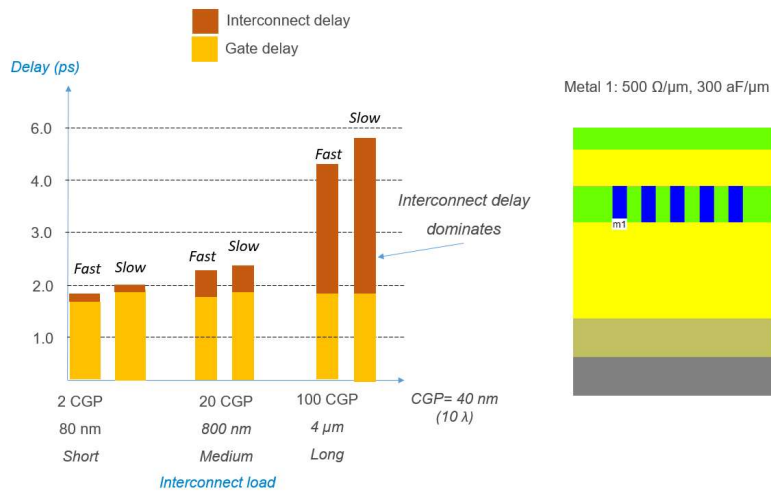


Figure 32: The interconnect delay has a strong impact on the total switching delay for medium to long interconnects

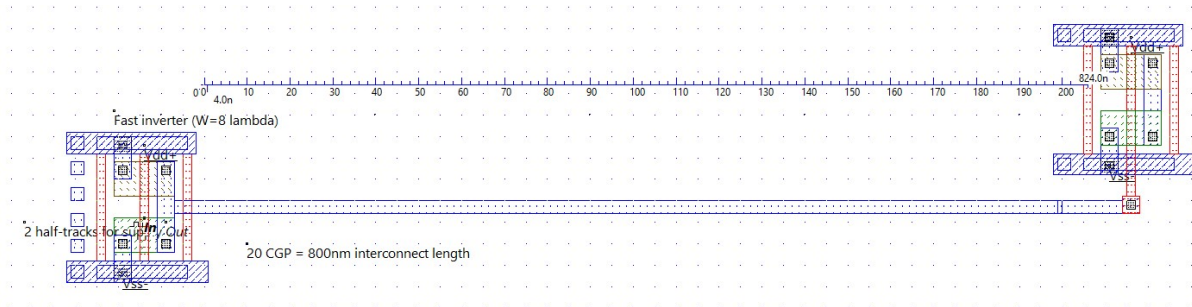


Figure 33: A fast inverter loading a 20-CGP metal interconnect and connecting to another inverter (inv5T-Fast-20CGP.MSK)

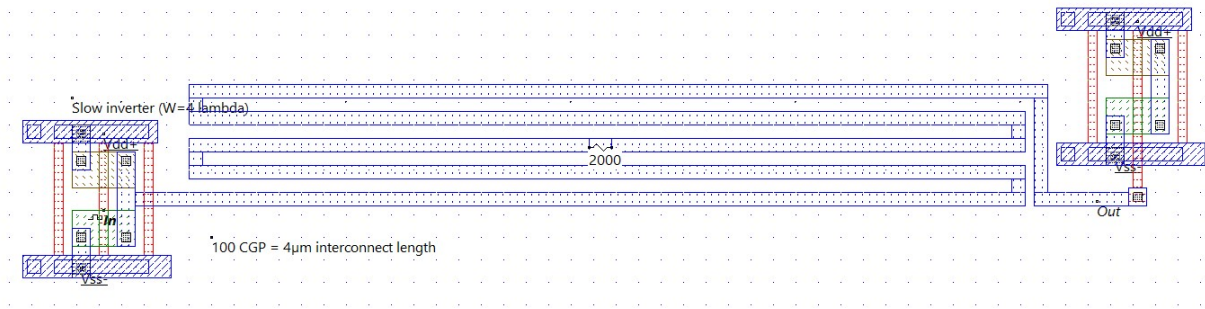


Figure 34: A fast inverter loading a 100-CGP metal interconnect and connecting to another inverter, with around $2K\Omega$ serial resistance (inv5T-Fast-100CGP.MSK)

Figure 33 shows the simulation setup for evaluating the near-end delay of a 20-CGP metal interconnect. For the 100-CGP interconnect, we fold the wire into 5 parts (Figure 34). A $2K\Omega$ virtual symbol has also been added to force the simulator to handle the RC delay, which is limited to capacitance C by default.

XOR Gate

Several options exist for building the XOR gate, such as the 6-Transistor & 10-Transistor implementations reported in Figure 34. The main problem of the 6T implementation (Figure 35 – top) is the VT losses as the n & p-devices are used as pass transistors, leading to inappropriate delays and non-ideal logic levels. The 10T implementation is safer but consumes more silicon area. Its corresponding layout consists of 3 inverters and 2 transmission gates, as reported in Figure 36. The worst-case delay in the simulation is around 4.8 ps.

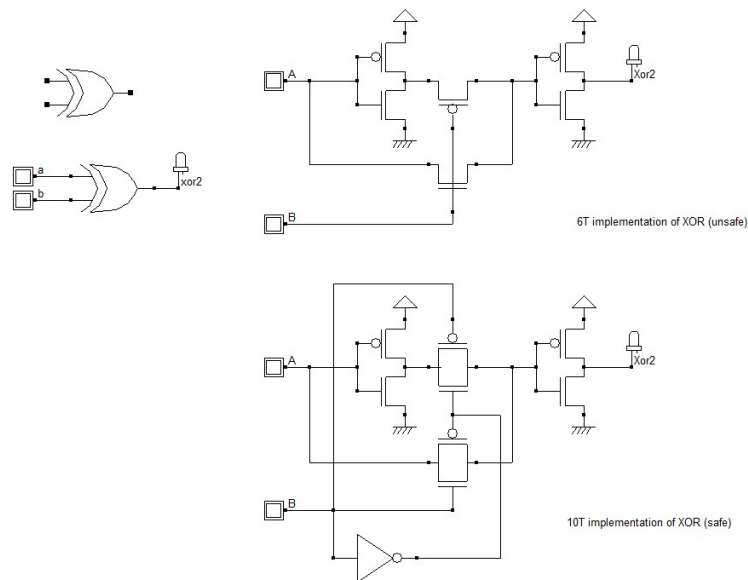


Figure 35: 6T and 10T schematic diagrams for the adder (XOR2_6T_10T.SCH)

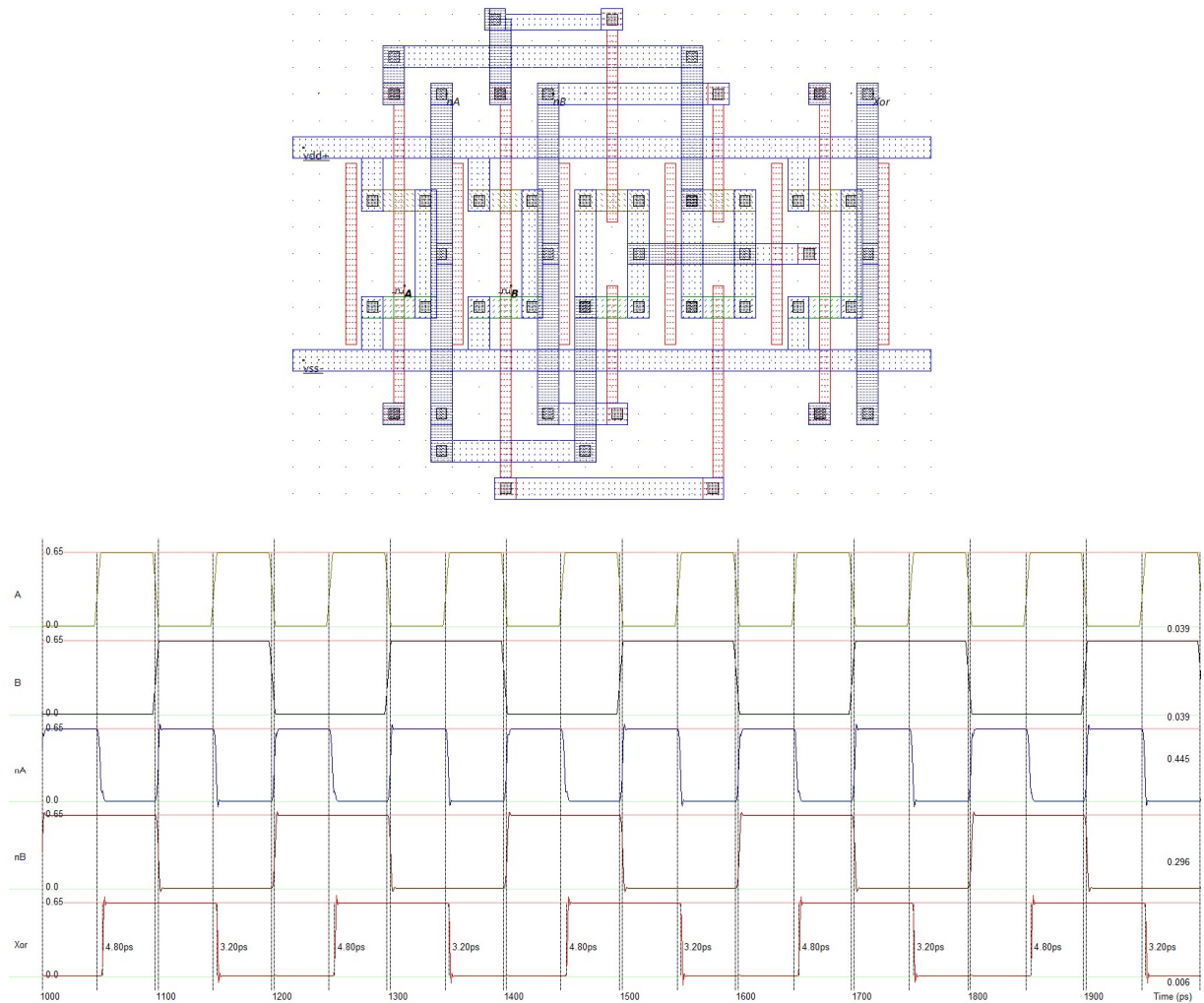
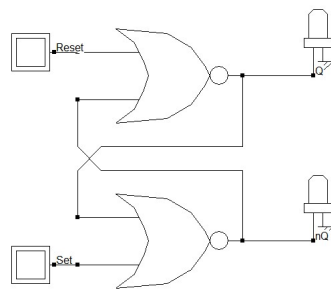


Figure 36: 10T implementation and simulation of the XOR gate (XOR2_10T.MSK)

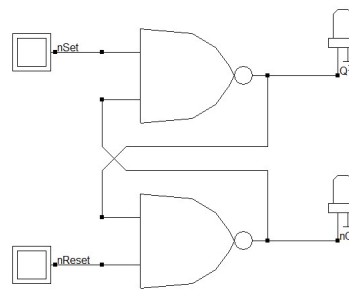
Sequential Design with Nano-Sheet

RS-Latch

The RS Latch is one of the simplest sequential circuits that may be built, but not the most useful. Two implementations of the RS-Latch are feasible, one based on NOR gates, the other one based on NAND gates (Figure 37-top). In the case of RS-NOR, the cell is sensitive to high levels of either Set or Reset, while for the RS-NAND, the cell is sensitive to low levels of either Set or Reset. We compile 2 NOR2 gates and add the necessary properties, as shown in Figure 37.



RS-NOR sensitive on high level of Set or Reset



RS-NAND sensitive on low level of Set or Reset

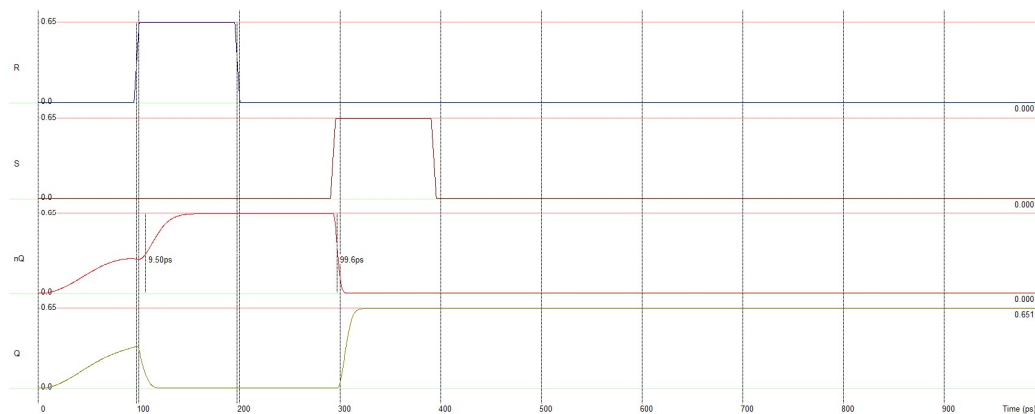
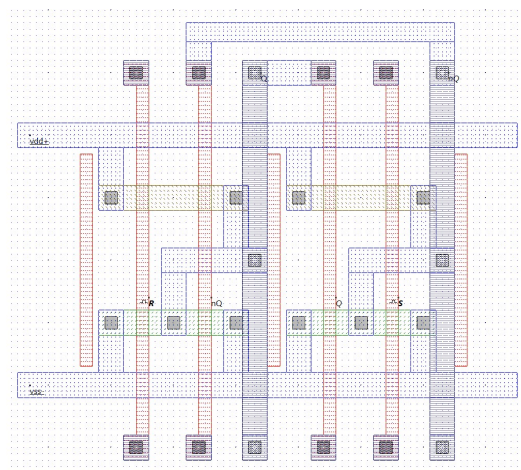


Figure 37: Compiled NOR gates to construct the RS-Latch (RSNor.MSK)

Memory

The 6-transistor static memory (also called SRAM 6T) consists of a 2-inverter stable loop that stores the data and 2 access transistors to either import or export the logic data through so-called bit lines. When the data is imported from outside to the cell (the data through BL, its opposite through \sim BL), we refer to the write cycle, while when the data is exported, it is called the read cycle. The cell structure is optimized for multiplication in X, Y in order to create a matrix of cells, typically 1000 x 1000 that leads to 1 Mega-bit memory plane.

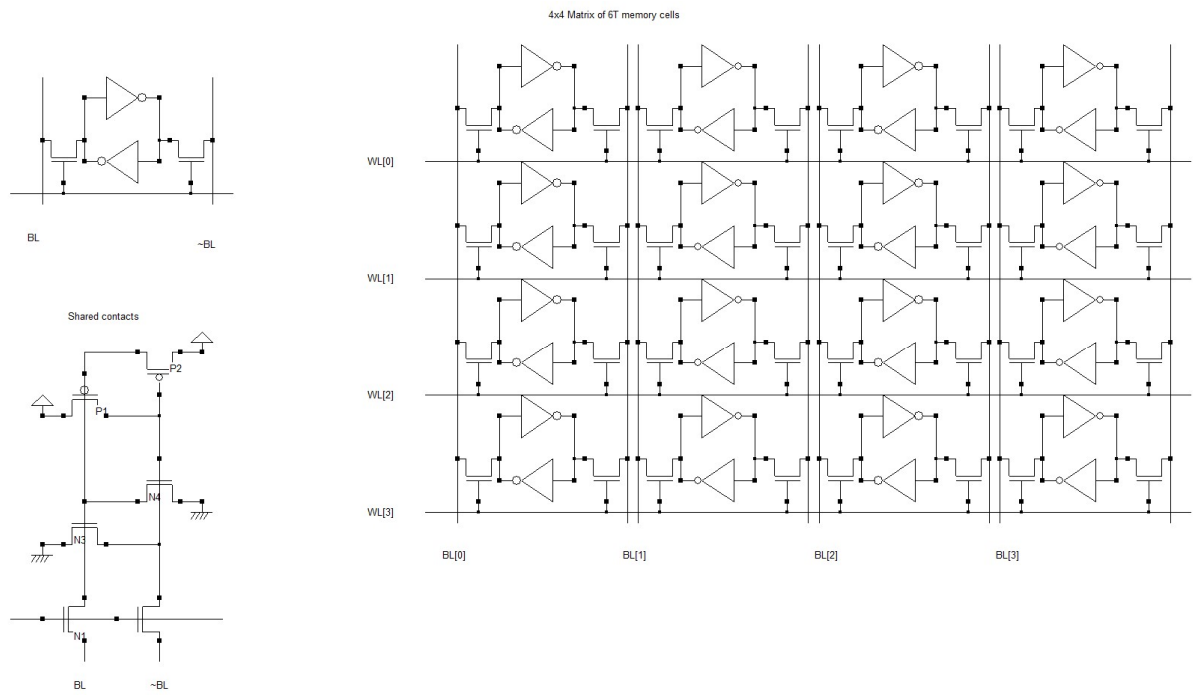


Figure 38: Principles of the SRAM topology (Ram6T-array.SCH)

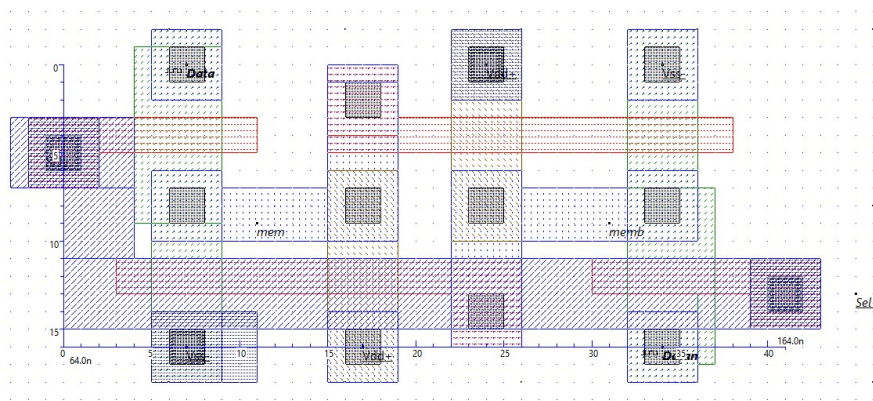


Figure 39: Layout of the 6T memory optimized to save space, share VDD & VSS contacts (Ram6T-3nm.MSK)

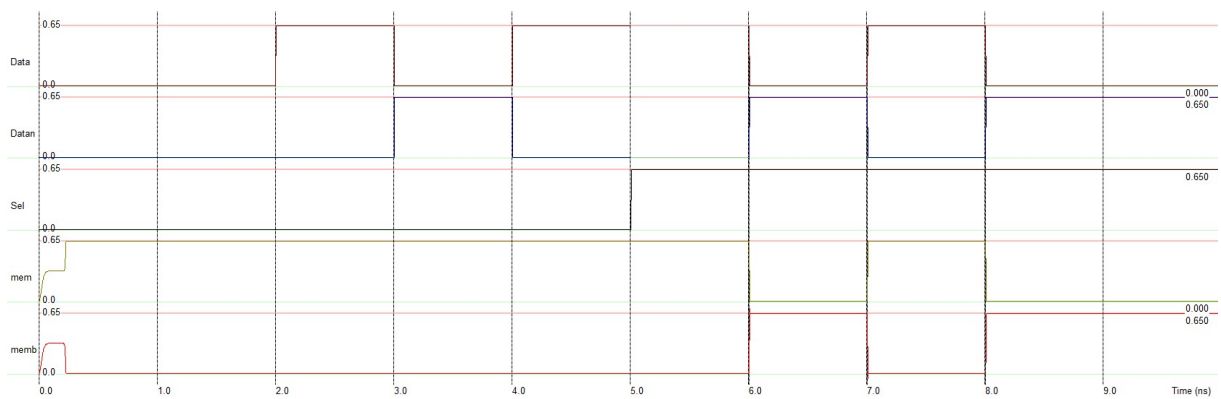


Figure 40: Write cycle of the SRAM memory (Ram6T-3nm.MSK)

The inverters are folded and the supply contacts are placed at the boundaries of the cell to enable to share VDD & VSS contacts with adjacent cells. The selection wire (Also called Word Line) is going through the cell using Metal3. The simulation reported figure 40 shows a memory state while the Selection is not active. At time 5, *Sel* is active but *Data* and $\sim Data$ are in 3-state mode. At time 6 ns, the memory is set to 0, and at time 7 ns, it is set to 1.

Future steps

Intel has unveiled in 2020 [Huang 2020] a 3D stacked CMOS architecture to enable smaller standard cell and SRAM cell size, while providing better performance per Watt for future computing systems. The combination of nanoribbon, stacked N-FET and P-FET devices (as illustrated by [Huang 2020], Figure 41) and further improvements in pitch scaling would divide by 10 the silicon surface in 20A node (2-nm) as compared to existing 10-nm FinFET technology.

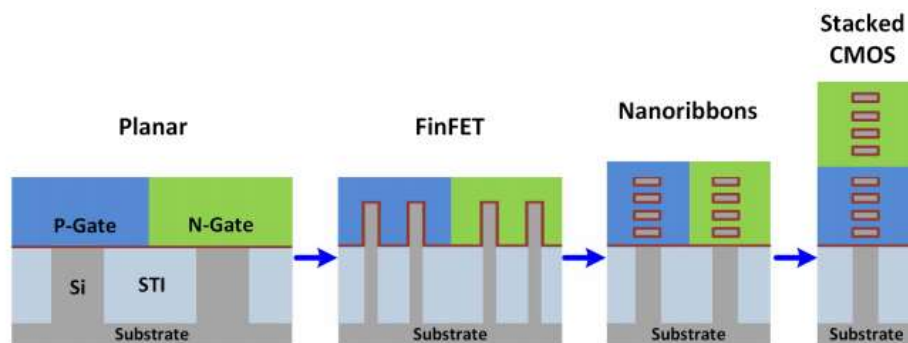


Figure 41 : From FinFET to NanoRibbons and stacked CMOS devices [Huang 2020]

Further 2x boost in transistor would be achieved by die stacking, buried power layers and improved packaging. An illustration of the combined benefits of all these innovations is given by [Intel 2021], with an expected multiplication of the number of transistors per chip by nearly a factor of 50 as compared to 10-nm. PowerVia is Intel's industry-first implementation of backside power delivery, an approach proposed by IMEC as Buried Power Layer [Gupta 2020]. The Microwind implementation of the buried power layer appears in Figure 42 and should be proposed for the 2-nm/20-Å node, associated with an application note to appear early 2022. The stacked N&P should be introduced for the 1.5-nm/15-Å node, to appear late 2022.

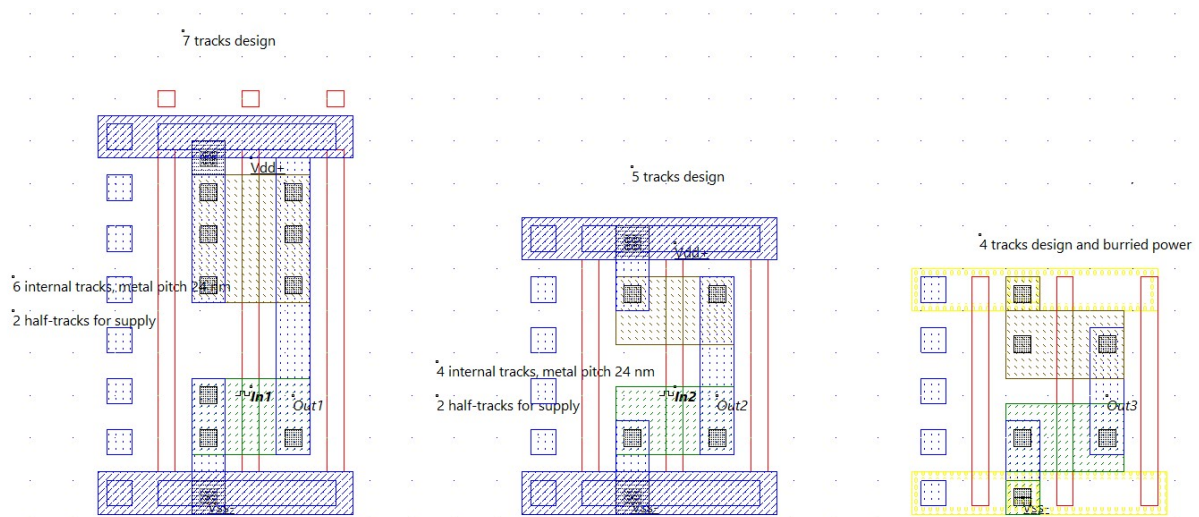


Figure 42 : Introducing buried power rails will enable further reduction of the cell height while keeping similar routing capabilities (inv-7-5-4T.MSK)

Conclusion

This application note has described the implementation of the 3-nm technology in the educational tool Microwind, which is a major breakthrough as compared to previous nodes due to the introduction of the nano-sheet FET. We discussed in this paper about the NsFET characteristics, the performance tradeoff, the interconnect parasitic effects and the performances of basic cells such as logic gates, ring oscillators and memory cells.

Although limited gains are observed in terms of geometrical scale down, the NsFET efficiency has enabled considerable gains in terms of device surface, enabling a shrink of the logic cell height and the suppression of the n-well. The 3-nm node enables 20% speed improvement or 25% power saving as compared to the 5-nm FinFET-based node. Further improvements are forecast by introducing buried power layers (2-nm/20-Å node) and stacked P-FET & N-FET (1.5nm/15-Å).

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We gratefully acknowledge the numerous students, researchers and engineers who have used our applications notes related to 90.5-nm technologies, and published more than 600 scientific papers using Microwind. This motivates us to release new application notes dedicated to the nano-cmos technologies of the future.

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