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Joris Jourdon, Sandrine Lhostis, Stéphane Moreau, Patrick Lamontagne, Hélène Frémont. Search for copper diffusion at hybrid bonding interface through chemical and electrical characterizations. *Microelectronics Reliability*, 2021, pp.114217. 10.1016/j.microrel.2021.114217 . hal-03375909

HAL Id: hal-03375909

<https://hal.science/hal-03375909>

Submitted on 5 Jan 2024

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Search for copper diffusion at hybrid bonding interface through chemical and electrical characterisations

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Abstract— Cu/SiO₂ diffusion at hybrid bonding interface without diffusion barrier was investigated in order to validate the electrical insulation of interconnects. The Cu thermal diffusion was studied by ToF-SIMS analysis of the dielectrics stack facing bonding pads after a bonding annealing (400 °C, 2 h) and a diffusion annealing (400 °C, 14 h). No trace of copper was found above the limit of detection 10¹⁷ at.cm⁻³. Cu ions drift was followed by I-V measurements on specially designed comb-serpentine that maximize the electrical field at bonding interface. Their efficiency was confirmed since physical failure analysis located the dielectric breakdown damage between bonding pads. Breakdown voltages coupled to wafer-to-wafer misalignments enabled the extraction of the SiO₂ breakdown strength: 3.4 MV.cm⁻¹. This study proves that at room temperature, hybrid bonding interconnects remain electrically insulated despite thermal budgets involved by the bonding process.

Keywords—3D integration, hybrid bonding, copper diffusion, ToF-SIMS, voltage breakdown

1. INTRODUCTION

3D integration enables the increase in performance and diversification of integrated circuits while limiting their form factor by stacking vertically interconnected dies. Among interconnection technologies, hybrid bonding offers the most aggressive pitch (< 1 μm) [1] and scalability. The connection between top and bottom tiers is ensured by copper bonding pads located at bonding interface, surrounded by insulating SiO₂ and connected to the BEOL with vias. Despite the improvement of bonding accuracy [2], the wafer-to-wafer misalignment remains, leading to the creation of a Cu/SiO₂ interface. Without diffusion barrier, Cu can diffuse through SiO₂ to assist dielectric conduction and reduce TDDB lifetime [3].

Wafer bonding is followed by an annealing in order to strengthen bonding interface and enable electrical connection. This step activates thermal diffusion of metal atoms since the diffusivity follows Arrhenius' law [4]. Moreover, the electrical field established between two interconnects triggers ionic copper drift. Both thermal and field-assisted diffusions were evidenced for metal/dielectric interfaces created by Cu deposition on SiO₂ [5] but not by direct bonding.

Some integration uses SiCN barrier at bonding interface to enhance the bonding strength but also prevent diffusion phenomena [6] even if copper thermal diffusion at Cu/SiO₂ bonding interface was not evidenced yet. It is believed that the native cuprous oxide formed on bonding pads prior to bonding acts as a diffusion barrier [7]. However, the Cu₂O layer can become a source of ionic copper when an electrical field is applied. When the metal-oxygen bond has the same

direction as the electrical field it stretches then breaks, releasing a positively charged copper ions free to drift in SiO₂ [8].

This article aims at evaluating thermal and field-assisted diffusion of copper at Cu/SiO₂ bonding interface using chemical and electrical analysis on dedicated test vehicles.

2. THERMAL DIFFUSION

2.1. Chemical analysis

2.1.1. Compatibility of hybrid bonding with ToF-SIMS

Thermal diffusion refers here to atomic diffusion of copper through SiO₂ when subjected to a thermal budget as opposition to ionic drift of charged copper ions when exposed to an electrical field. A simple sample with a large Cu/SiO₂ contact area would be the bonding of fullsheet Cu and SiO₂ wafers. However, such sample is unsuitable for two reasons. Firstly, the Cu/SiO₂ interface is not robust enough to support mandatory steps for sample preparation. Grinding and sawing generate a mechanical stress that could lead to delamination. The bonding energy is weak, about 100 mJ.m⁻², because the adhesion of oxidized copper and SiO₂ surfaces is ensured by hydrogen bonds. Secondly, patterned copper favors the contact between Cu and SiO₂. Indeed, Cu and SiO₂ are initially separated by a native Cu₂O layer. During bonding annealing, the CTE mismatch of Cu and SiO₂ leads to the strain of bonding pads. The resulting thermomechanical stress forces the fracture and the segregation of Cu₂O layer into nodules [9]. Therefore, SiO₂/SiO₂ interface is required in order to strengthen bonding interface and triggers the contact of Cu with SiO₂.

Hybrid bonding integration is robust thanks to SiO₂/SiO₂ (covalent bonds) and Cu/Cu (metallic bonds) interfaces. The choice of chemical analysis method relies on the integration. For the integration previously reported [10], bonding pads are 3.6 μm wide and the maximum of misalignment between top and bottom wafers is 2 μm (3σ). Thus, the chemical analysis must be very local. EDX fulfills this criterion but it is not sensitive enough to detect Cu dispersed in a SiO₂ matrix. For a SiO₂ analysis, monocrystalline Si is taken as a reference (10²² at.cm⁻³). EDX sensitivity is around 0.1-1 mol% so the limit detectable concentration is 10¹⁹-10²⁰ at.cm⁻³. The maximum of solubility of copper is 10¹⁸ at.cm⁻³ which is lower than EDX detection threshold. ToF-SIMS can address lower concentrations (10¹⁷ at.cm⁻³), therefore it is appropriate to investigate copper diffusion.

ToF-SIMS requires the abrasion of a 300 μm × 300 μm surface, so the preparation of dedicated sample is necessary to characterize the dielectric at bonding interface.

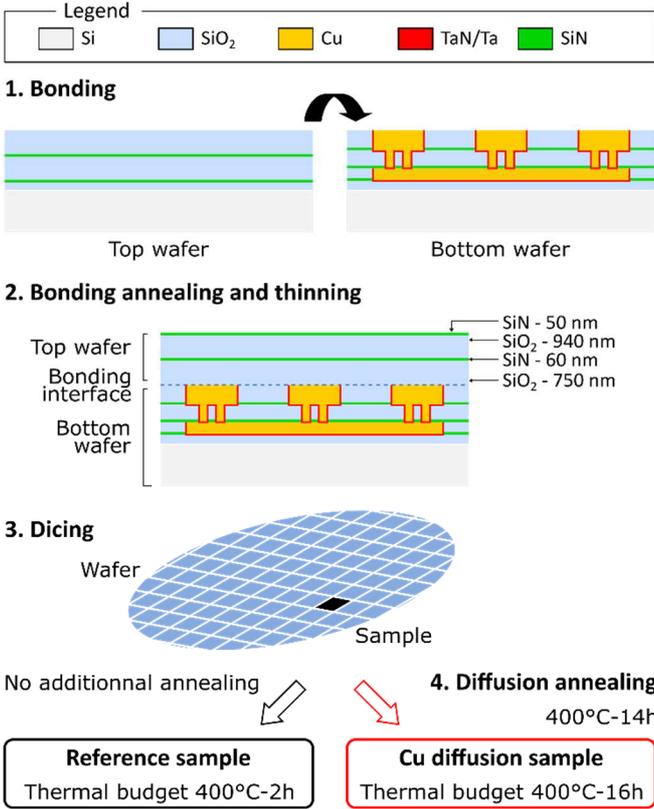


Figure 1 Process flow of reference and Cu diffusion samples.

2.1.2. Experimental

The manufacturing process of samples consists in bonding two 300 mm wafers: fullsheet SiO₂ and Cu patterning. The top tier is the stacking SiO₂/SiN/SiO₂/SiN/SiO₂ obtained by successive depositions of dielectrics on a silicon substrate (Figure 1). The bottom tier contains two metal levels: metal lines (single damascene) and via + bonding pads (dual damascene). Copper is separated from SiO₂ thanks to a TaN/Ta diffusion barrier. After a dedicated surface preparation, wafer are bonded at room temperature, followed by a 400 °C bonding annealing during 2 h. Thanks to the strong SiO₂/SiO₂ interface, the silicon substrate of the top wafer can be removed by mechanical and chemical thinning until the first SiN barrier is exposed. Then, the stack is diced into 10 mm x 10 mm samples. At this point, reference samples are created, so called because they were exposed to a minimal thermal budget due to the bonding annealing. A part of reference samples undergoes an additional annealing called “diffusion annealing” in order to activate thermal diffusion of copper through SiO₂. The temperature of annealing is 400 °C, which is the maximal temperature acceptable for Cu-based integration. The duration of annealing is determined by modeling the thermal diffusion for different coefficients of diffusion, D, found in literature. The surface concentration of Cu at a position x, after a time of annealing t, is given by [11]:

$$\rho(x, t) = \rho_0 \left(1 - \operatorname{erf} \left(\frac{x}{2\sqrt{Dt}} \right) \right) \quad (1)$$

with ρ_0 the surface concentration of Cu at Cu/SiO₂ interface. A 14 h diffusion annealing enables to observe a change in Cu concentration higher than ToF-SIMS resolution (7 nm per

decade) whatever the coefficient of diffusion (Figure 2). The diffusion annealing is achieved by placing some reference samples in an oven under N₂ atmosphere at 400 °C for 14 h.

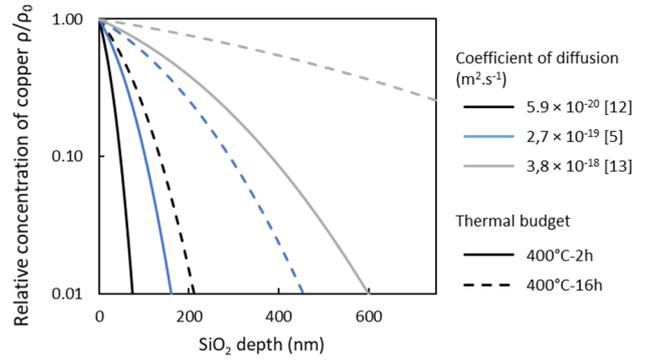


Figure 2 Theoretical concentration profiles of Cu in SiO₂ for reference (400°C-2h) and diffusion annealing (400°C-16h) samples and various coefficients of diffusion found in the literature [5,12,13].

2.1.3. Results

ToF-SIMS analysis is performed on two samples: reference sample and sample after diffusion annealing. The dielectric multilayer allows a homogeneous abrasion to avoid loss of resolution. Also, it contains no bulk copper that could mask diffused Cu. The area of interest is located between the first SiN barrier (layer #1 in Figure 3a) and SiO₂/Cu interface. The nitrogen and copper concentration profiles for both samples are plotted in Figure 3b. The two SiN barriers are located thanks to the peaks of nitrogen. Concentration profiles of samples with or without diffusion annealing are superimposed which indicates no detectable effect of the diffusion annealing. Moreover, as SiN acts as a diffusion barrier, an accumulation of copper should be visible in the second SiN barrier (layer #3). The concentrations of copper in the first SiN barrier on the surface of samples with or without diffusion annealing, are respectively 1.82×10^{20} and 1.17×10^{21} at.cm⁻³. However, no peak of Cu was found at SiO₂/SiN interface nor in the second SiN barrier. The copper on surface is probably a contamination during the handling of samples. Thus, there is no copper thermal diffusion or the concentration does not exceed 10¹⁷ at.cm⁻³. Our Electron Energy Loss Spectroscopy (EELS) analysis revealed the presence of a thin layer (~3 nm) of cuprous oxide Cu₂O at the copper/dielectric interface that most probably acts as a diffusion barrier to copper [14]. In the next section, an electrical field is applied to generate Cu ions and force diffusion through SiO₂.

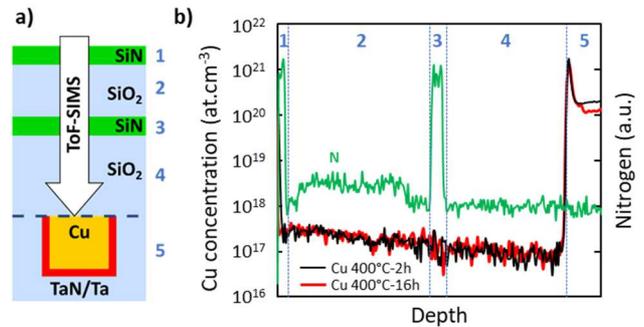


Figure 3 (a) Schematic cross section of samples. (b) Superimposition of Cu concentration profiles obtained by ToF-SIMS

analysis of reference (400°C-2h) and diffusion annealing (400°C-16h) samples.

2.2. Electrical characterisation

2.2.1. Experimental

Electrical measurements are performed on comb-serpentines. The test structures are made compatible with 3D hybrid bonding integration by splitting them into bonding pads connected together by a metal line (Figure 4a). The serpentine and combs are respectively located in top and bottom tiers. Bonding pads are 1.71 μm wide and are voluntarily misaligned from a distance d at the comb-serpentine border (Figure 4b). This particular disposition maximizes the Cu/SiO₂ contact area and the electrical field at bonding interface. During the bonding step, misalignment occurs because of the translation, the rotation and the scaling of wafers [15]. The bonding alignment accuracy is 200 nm (3σ) and the rotation can be considered as null. The distance between combs and serpentine bonding pads is:

$$d = d_0 - \Delta x, d_0 = 252 \text{ nm} \quad (2)$$

where Δx is the misalignment along x axis. The bonding is followed by a 400 °C bonding annealing for 2 h.

I-V measurement are performed at wafer level by a semi-automatic prober at 25 °C. A 0-120 V voltage ramp is applied to the serpentine; combs can be either in floating mode or connected to the ground. The currents measured through serpentine and comb are respectively noted I_{serp} and I_{comb} . The current compliance is 10⁻⁴ A.

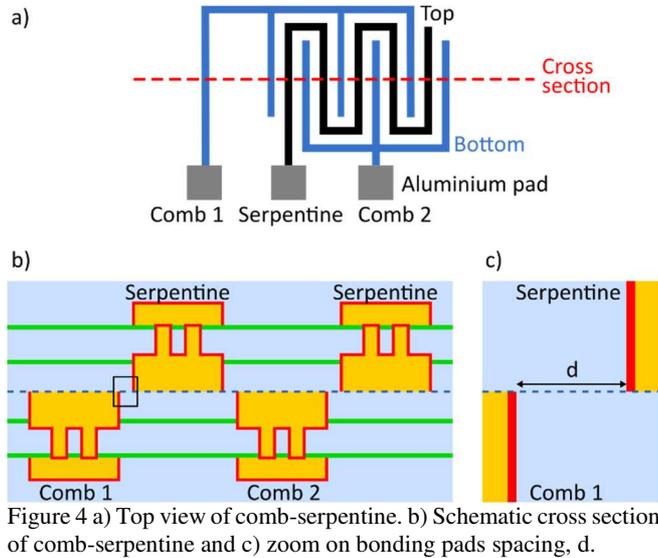


Figure 4 a) Top view of comb-serpentine. b) Schematic cross section of comb-serpentine and c) zoom on bonding pads spacing, d .

2.2.2. Result

35 dies were sequentially tested on the same wafer. The current compliance (10⁻⁴ A) was reached for 27 dies. The prober is equipped with a microscope for wafer level visual inspection. Signs of degradation between aluminum pads were evidenced for the 27 dies that reached the compliance. Therefore, the population is split into two parts: dies with or without visible damage.

2.2.2.1. Breakdown between aluminium pads

I-V curves of dies that exhibit damages are gathered in Figure 5a. Breakdown voltages range from 107 to 119 V and the

comb-serpentine spacing varies between 147 and 245 nm. Voltage breakdown V_{BD} plotted as a function of d appears to be constant (Figure 6). This independence of V_{BD} to misalignment suggests that failure does not occur at the bonding interface. Such hypothesis can be confirmed by performing a physical failure analysis.

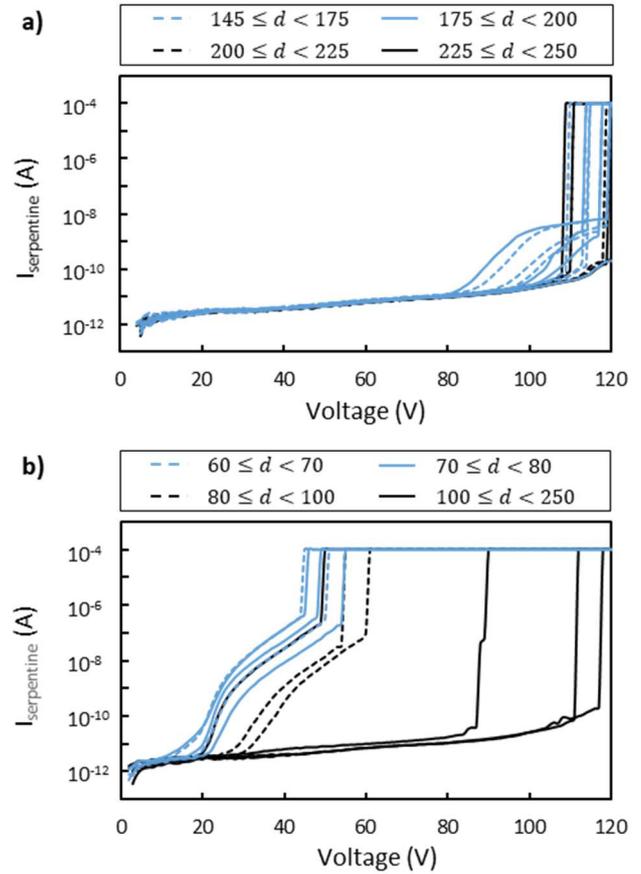


Figure 5 Comb-serpentine I-V measurements for various spacing values leading to a) visible or b) invisible damages.

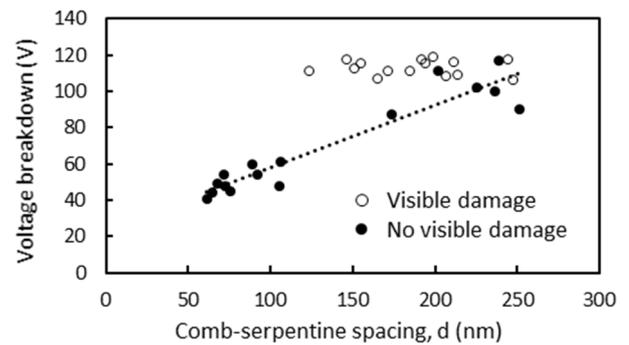


Figure 6 Comb-serpentine breakdown voltage as a function of their spacing.

Figure 7a is a top view of the aluminum pads after a sample preparation which consists in thinning the frontside silicon to remove melted residues. The failure located between pads has a filament shape with extremities positioned in pads' corners. Due to the square geometry of pads, the electrical field is prone to be the highest in corners. The test structure is neither observable by visible nor infrared light because it is covered by a stack of dielectrics and metal layers. OBIRCH analysis

is performed on two test structures in order to reveal potential shorts under the surface (Figure 7b-c). The defect exclusively forms near aluminum pads. Hence, no breakdown occurs in the test structures. However, OBIRCH does not provide any information regarding the position of the failure in the stack. SEM images are used as complementary analysis. Cross sections are performed by focused ion beam (FIB) in one filament (Figure 7d) and in the area revealed by OBIRCH (Figure 7e). The filament corresponds to the melting of the thinned silicon across the entire layer thickness. Closer to the aluminum pad, the melting extends to the top metal line M1. However, hybrid bonding pads are always intact. Morphological analyses confirm that failure occurred on the surface of the top wafer where the spacing between aluminium pads and metal lines is set by a photomask. Therefore, the failure is visible by top view inspection and the voltage breakdown is insensitive to the misalignment. At higher misalignment values, when the distance between bonding pads is smaller than 150 nm, a different type of failure occurs.

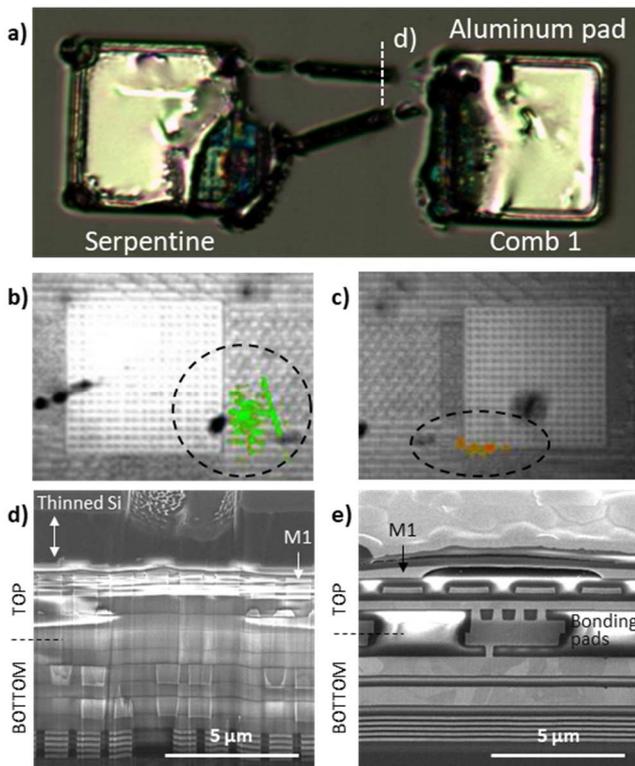


Figure 7 a) Top view photography of sample 1 aluminum pads after voltage breakdown. OBIRCH analysis on samples b) 1 and c) 2 shows defects encircled by a black dashed line. FIB-SEM cross section of d) sample 1 filament and e) sample 2 defect area revealed by OBIRCH.

2.2.2.2. Breakdown at bonding interface

I-V curves of dies that do not show degradation of aluminium pads are plotted in Figure 5b. Breakdown voltages range from 41 to 117 V and the comb-serpentine spacing varies between 61 and 250 nm. The general trend is that the closer the comb and serpentine, the lower the breakdown voltage. The misalignment reduces the dielectric thickness between the comb and the serpentine. Therefore, dielectric breakdown occurs at lower voltage for the most misaligned test

structures. This suggests that the failure occurs at bonding interface, between bonding pads.

When $d > 150$ nm, I-V characteristics exhibit the same behavior as breakdown between aluminum pads. The leakage current slowly increases from 10^{-13} to 10^{-10} A, then immediately reaches compliance. When $d < 150$ nm, and starting at 20 V, the compliance is preceded by a quick increase in leakage current from 10^{-12} to 10^{-6} A. The two types of electrical signature can be explained by the difference in the conduction mechanism related to the electrical field. At constant voltage, highest electrical fields will be found in the most misaligned test structures. It has been demonstrated that electrical conduction is driven by Schottky emission and Poole-Frenkel for low and high electrical fields respectively [16]. For $d > 150$ nm, the failure can be indifferently located either at comb-serpentine or at aluminum pad. The first cause is the random behavior of SiO_2 linked to its disordered structure. The second one is the misalignment along the Y axis that changes the test structure geometry, therefore the critical path.

Electrical measurements are followed by failure analysis in order to locate the dielectric breakdown. As seen in Figure 8a, visual inspection shows no evidence of damage. An OBIRCH analysis conducted on the same sample revealed a hot spot which position matches the test structure footprint (Figure 8b). An electrical short could trigger such a signal. FIB-SEM analysis of the spot is performed to identify the nature of the defect and the metal level stressed. Bonding pads are recognizable at their staggered disposition (Figure 8c). The cross section plane is between vias so they are not visible. The comb-serpentine spacing measured on the SEM image is about 30 nm, and 60 nm according to overlay measurements. This deviation can be explained by the angled edge of bonding pads. The etching of bonding pads shapes them as trapezoid so the distances obtained by top view observation differs from the actual distance at bonding interface.

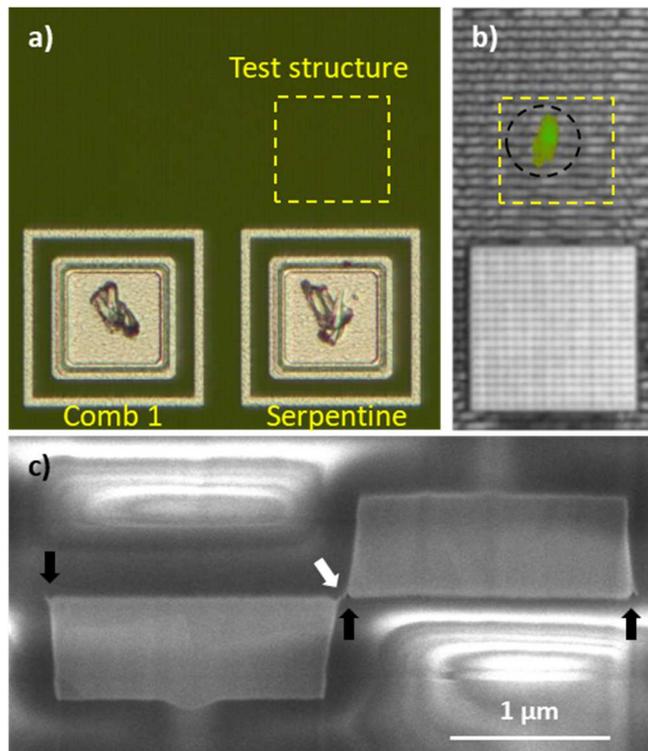


Figure 8 a) Top view photography of a test structure after voltage breakdown. b) OBIRCH analysis locates the defect (dashed circle) within the test structure footprint. c) FIB-SEM cross section of comb-serpentine in defect area revealed by OBIRCH. Black and white arrows respectively indicate lack of copper and short.

The cross section also reveals a metallic filament that links TaN barrier of two bonding pads at the bonding interface, creating a short between the comb and the serpentine. The short happens where the electrical field is maximum. In this area, the two metallic species are Cu and Ta. Cu is prompter than Ta to diffuse in SiO₂, especially along interfaces known to be preferential diffusion paths. A lack of copper is visible both sides of bonding pads, at the intersection of Ta/Cu and Cu/SiO₂ interfaces but it is not the result of Cu migration. This well-known defect called “fang” is generated during CMP because of stress concentration. Chen *et al.* proposed a failure mechanism in which diffused Cu⁺ ions move toward the cathode then combine with electrons to become neutral atoms. The atoms agglomerate and form a direct metallic shorting bridge. TEM-EDX would be an effective complementary analysis to verify this hypothesis. Thanks to the formation of Cu clusters, the EDX limit of detection is no longer an issue.

The breakdown strength extracted by plotting V_{BD} as a function of d , is 3.4 MV.cm⁻¹ (Figure 6). This value is depreciated due to misalignment measurement but remains in agreement with previous studies. Literature reports SiO₂ breakdown strength between 2 and 10 MV.cm⁻¹ [17,18]. Comb-serpentine structures allow the characterization of the dielectric at the bonding interface. The tests prove that it conserves its insulating properties despite the thermal budget involved in the bonding process. Even if there is copper diffusion at the bonding interface, it is so limited that it does not degrade the dielectric.

CONCLUSION

This paper aimed to evaluate the diffusion of copper through SiO₂ at hybrid bonding interface under thermal and electrical stress. ToF-SIMS did not detect any trace of copper above 10¹⁷ at.cm⁻³ after a 400°C-16h thermal budget. It is believed that a native copper oxide layer acts as a diffusion barrier. Copper ions can be generated and drift by applying an electrical field. A comb-serpentine test structure was specially designed in order to be compatible with this specific 3D integration, to maximize Cu/SiO₂ interface and the electrical field between bonding pads. I-V measurements evidenced that the voltage breakdown is misalignment dependent. The defect location at bonding interface was confirmed by failure analysis. The characterized dielectric is the one between bonding pads and its breakdown strength is 3.4 MV.cm⁻¹. Thus, the SiO₂ at the bonding interface remains insulating despite the bonding annealing and the lack of diffusion barrier. The experimental protocol employed did not allow us to conclude regarding copper diffusion and its negative impact on the dielectric integrity. However, the results question the necessity of a diffusion barrier at the bonding interface. A further study will focus on the native copper oxide layer and triangular voltage sweep to track copper ions drift since this technique allows to lower the detection of metallic contaminants down to 10⁻⁹ ions.cm⁻³. **In addition, time dependent dielectric breakdown (TTDB) tests are on progress which does not reveal any unexpected effect.**

ACKNOWLEDGMENTS

This work was funded thanks to the French national program “Programme d’Investissement d’Avenir IRT Nanoelec” ANR-10-AIRT-05.

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