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Towards a safe failure mode under short-circuit operation of power SiC MOSFET using optimal gate source voltage depolarization

Wadia Jouha^a, Frédéric Richardeau^a, Stephane Azzopardi^b

^a LAPLACE, University of Toulouse, CNRS, INPT, UPS, France

^b Safran Tech, SAFRAN TECH, Paris Saclay, France

Abstract –This paper focuses on the enhancement of the robustness level of SiC MOSFET during short-circuit conditions. In this study, two approaches allowing to ensure safe “Fail-To-Open” (FTO) mode in planar power SiC MOSFET devices under short-circuit operation are presented. These approaches are based on direct depolarization of the gate source voltage and its estimation from the calculation of the critical dissipated power (W/mm²) between FTO and classical unsafe thermal runaway. They allow to determine the maximum value of the gate source voltage to preserve a FTO mode under a drain source voltage close to the nominal value i.e $V_{BRmin} / 2$. The boundary of the power density between FTO and “Fail-To-Short” (FTS) is introduced. A complete experimentation of the two failure modes in competition that may appear during short-circuit (SC) test of 1.2 kV SiC MOSFETs is presented. Finally, the penalty of the gate source voltage depolarization on the on-state resistance ($R_{ds(on)}$) is investigated in order to evaluate the techniques efficiency.

1. Introduction

Wide bandgap semiconductor materials like Silicon Carbide (SiC) stands in the centre of attention for designing new power semiconductor devices thanks to their better intrinsic properties than Silicon (Si) [1]. SiC has interesting physical properties such as high electric field and high thermal conductivity that makes ability to ensure superior performances in high power applications (temperature, switching frequency, efficiency) [2]. SiC MOSFET are an effective technology solution to design high performance electrical-power switches that provides lower switching losses and high power density [3,4]. Beside the switching performance, SiC MOSFETs robustness in the industrial field is a major feature that must be considered for power conversion systems [5]. Indeed, SiC MOSFET capability in withstanding stressful conditions, such as short-circuit (SC) operation, is the main obstacle of the expansion of these devices to industrial applications.

Literature highlights several studies investigating the SC capability of SiC MOSFETs [6-9]. According to the literature, SiC MOSFETs may present, under short circuit operation, a competition between two failure modes. The first one is called drain-source Fail-To-Short (FTS) failure characterized by a drain-source short and leads to a permanent damage of the device. The second one is named drain-source Fail-To-Open (FTO) failure caused by a hard gate –source short-circuit path which $V_{gs} < V_{gsth}$ (threshold voltage) is applied.

The FTS mode is issued from a thermal runaway and/or the parasitic BJT latch-up inducing the local destruction of the die and the creation of a metallic path between drain and source. In the FTO mode, fusion and diffusion of the Al top metal through gate-cracks are observed [10]. This failure is related to the extreme heat in short-circuit between the poly silicon gate and the Al source. This metallic path can be located either on top of

the chip between the gate fingers and the source pad below the passivation layer, and/or through the ILD (Inter-Layer Dielectric) across metallized cracks [11]. This is due to a very low coefficient of thermal expansion of the oxide compared to those of Al and SiO₂. In the latter case, the short-circuit between the gate and source electrodes can lead to a permanent FTO mode if $V_{gs} < V_{gsth}$ or a partial FTO mode if $V_{gs} > V_{gsth}$. In any case, FTO is clearly a more secure failure mode and is suitable for safety applications. In the literature [12], to preserve the FTO mode, a drain source voltage (V_{ds}) depolarization method was used to reduce the power density crossing the chip in order to avoid thermal runaway. Obviously, this approach directly reduces the switching power capability to the same power semiconductor device.

This paper focuses on the faculty to obtain a FTO failure mode using the two above approaches based on direct depolarization of the gate source voltage (V_{gs}) by reducing the buffer voltage (V_{buffer}). These approaches aim to determine the maximum value of V_{gs} allowing a FTO mode to be maintained at a voltage V_{ds} close to the nominal value i.e $V_{BRmin}/2$ (eg.600 V for 1.2 kV rating). The short circuit characterizations are performed on commercially available power SiC MOSFETs. The device performance and robustness are investigated under single pulse short circuit, for various V_{buffer} bias conditions and at room temperature $T = 25$ °C. This paper is organized as follow: first, the device under test and test protocol are presented. Then, the experimental results of V_{gs} depolarization approach, the V_{gs} estimation method and the penalty of these approaches on $R_{ds(on)}$ are discussed.

2. Device under test and test protocol

2.1 Device under test

Table 1. Electrical characteristics of power device under test

Device	C2M0080120D
Total chip Surface (mm ²)	10.4
V _{dss} (V)	1200
I _D @ 25 °C (A)	36
V _{gsnom} (on/off) (V)	-5/20
R _{ds(on)} (mΩ) @ V _{gsnom} @ T _{case} =25°C	80

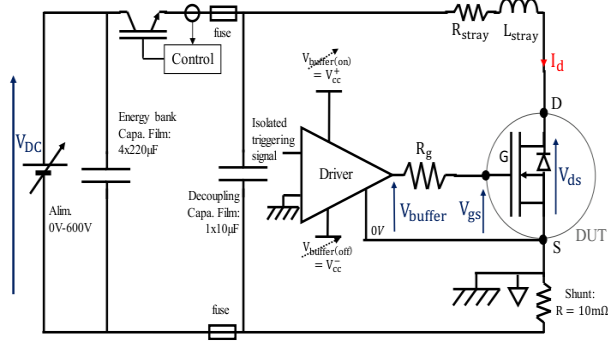


Fig. 1. Schematic of Type 1 short-circuit test [11].

In this work, short circuit tests are carried out on 1200 V planar SiC MOSFETs manufactured by Cree (C2M0080120D) [13]. Main electrical characteristics are presented in Table 1.

2.1 Protocol of short circuit test

Commercially power SiC MOSFET are examined under type 1 short circuit test. The test setup is presented in Fig.1. The characterization of the Device Under Test (DUT) under type 1 short-circuit test is performed by placing the DUT in the Low Side (LS) position and the High Side (HS) device is replaced by a strap bar. A circuit breaker based on Si IGBT mounted in series is used to protect the DUT from any damage after short-circuit failure. An adjustable gate drive was developed in order to drive the various DUT. The turn-on voltage ($V_{\text{buffer(on)}}$) can be adjusted from 9 V to 21.5 V and the turn-off voltage ($V_{\text{buffer(off)}}$) can be adjusted from 0 V to -6 V. The control signal for the driver is provided by an FPGA allowing to adjust the desired short-circuit duration through a touch screen. The FTO and / or FTS failure mode occurs by applying successive short circuit tests with increasing short circuit duration (T_{sc}) by 1μs at each test. The DC bus voltage (V_{DC}) or V_{ds} is provided by a DC voltage supply (0 V-600 V). V_{ds} is gradually applied until the desired value is reached. A gate resistance (R_{G}) fixed to 47 Ω was used for this study for local measurement of gate leakage and permits a slow turn-off to avoid overvoltage without the use of a Soft Shut Down (SSD).

3. Experimental results and discussion

3.1. Failure mode and Gate voltage depolarization

Both FTS and FTO modes are controlled by the temperature

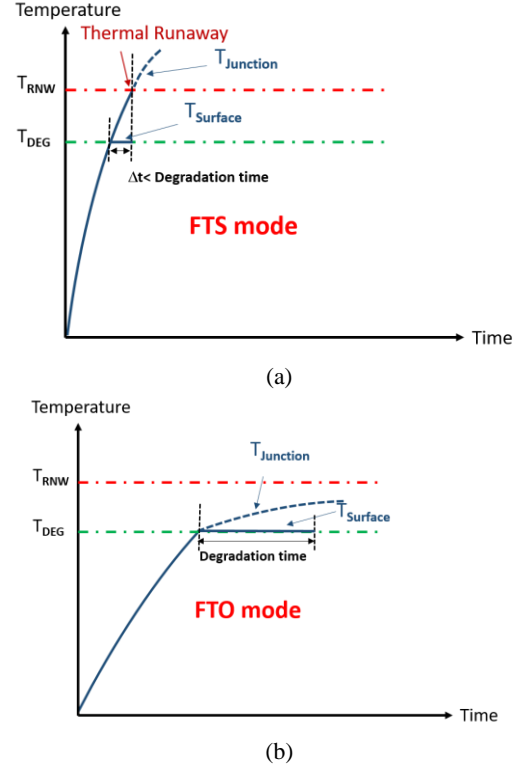


Fig. 2. Interpretation of two failure type [14]

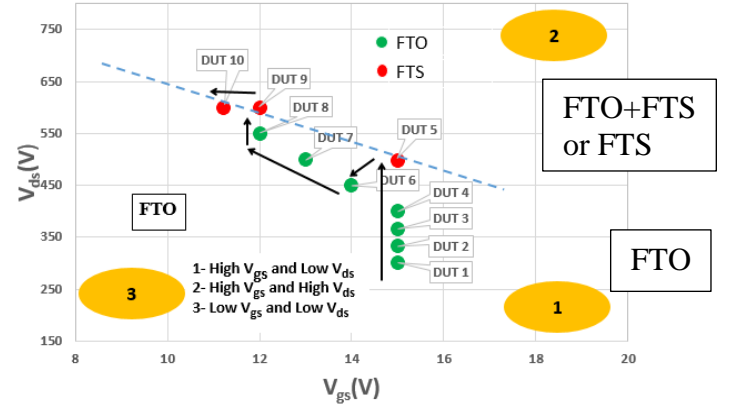


Fig. 3. Results of short circuit tests carried out on the C2M0080120D devices using a direct depolarization of V_{gs} . (FTO: fail-to-open, FTS : fail-to-short).

increase inside the device, and more precisely by its growth rate. In [14], the authors explain the appearance of these failure modes and its dependence on device temperature. This approach presented in Fig. 2.

From Fig. 2a, the FTS mode occurs when the junction temperature rises quickly and reaches a thermal runaway temperature (T_{RNW}) in a time that does not allow the gate degradation delay time to be reached. If the device temperature remains between the degradation temperature (T_{DEG}) and the runaway temperature for sufficient time, the device should reached in an FTO type defect (Fig. 3b). This implies that in

Table 2. Summary of short circuit tests performed on C2M0080120D 80mΩ / 1200V devices using a direct depolarization of V_{gs}

DUT	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
V_{ds} (V)	300	333	363	400	500	450	500	550	600	600
V_{gs} (V)	15	15	15	15	15	14	13	12	12	11.2
Failure mode	FTO	FTO	FTO	FTO	FTS	FTO	FTO	FTO	FTS	FTS
T_{sc} (μs)	40	28	25	21	16	20	21	18	13	19
E_{sc} (J)	0.80	0.97	0.93	0.90	0.81	0.82	0.82	0.64	0.63	0.79
P (W/mm ²)	1918	3316	3589	4102	4936	3948	3757	3418	4640	4014

order to obtain the FTO failure, the temperature within the chip should not rise too quickly. According to equation (1) [15], there are two ways to decrease junction temperature in a short-circuited chip: decrease V_{ds} or decrease the density of saturation current by V_{gs} depolarization.

$$\Delta T_{jmax}(t) = \frac{2 \cdot V_{ds} \cdot J_{sat}}{\rho c \sqrt{\pi \alpha}} \sqrt{t} \quad (1)$$

where ρ is the density of SiC, c is the specific heat of SiC, α is the thermal diffusivity of SiC and t is the SC time.

In our study, to preserve a FTO under a V_{ds} value close to the nominal voltage, an approach based on the direct depolarization of V_{gs} is investigated. Short circuit tests are carried out by setting the gate source polarization value at 15 V and starting with a voltage V_{ds} of 300 V. Many commercial SiC MOSFET components have a FTO mode at a reduced V_{ds} . This voltage is the starting point of the study. If the test induces a secure failure mode FTO at this value of V_{gs} , then the V_{ds} voltage is gradually increased by one step (between 33V and 100V). On the other hand, if the test induces a FTS, then V_{gs} is reduced with a step of 1V. Fig.3 summarizes the results of short circuit tests carried out on the C2M0080120D devices under various polarization conditions of V_{ds} using a direct depolarization of V_{gs} . Table 2 presents for each DUT:

- the failure mode (FTO or FTS)
- the maximum short circuit duration T_{sc} ,
- the maximum energy $E_{sc} = I_{dsmoy} \cdot V_{ds} \cdot T_{sc}$,
- the dissipated power per unit area $P = I_{dsmoy} \cdot V_{ds} / (\text{surface of the chip})$.

It can be observed that direct polarization of V_{gs} method shows a promising results in terms of T_{sc} that exceeds 10μs (standard for IGBT device), and the appearance of FTO mode under a V_{ds} close to the nominal value. From Fig. 3, three critical regions must be defined in order to choose an optimum short circuit bias conditions. The first region (1) appears for very low drain voltages where the device is in strong derating in V_{ds} . In this region, the device robustness is more assured by FTO mode, however its performance is penalized in terms of the converter efficiency and its cost. In the second zone (2), the device is placed under high V_{ds} and V_{gs} which reduce its robustness and leads to its degradation (appearance of a strong drain leakage and gate leakage currents) or to its failure with a FTO mode

followed by a FTS or directly an FTS mode. For the third region (3), the device is placed under a small gate polarization (strong depolarization in V_{gs}), which generates an increase in $R_{ds(on)}$ and consequently losses in higher conduction. On the other hand, with a V_{gs} too close to V_{gsth} makes the device more sensitive to electron trapping effect at SiC/SiO₂ interface and V_{gsth} drift [16-17]. Also, due to the variability of local V_{gsth} from one local MOSFET cell to another, a too low V_{gs} can lead to a high current density inhomogeneity of the chip surface in the channel regions. Fig. 4 depicts the waveforms of the various voltages and currents obtained for the short circuit test performed on DUT#8 under $V_{buffer} = 12$ V and $V_{ds} = 550$ V. From the Fig. 4, a delayed FTO with 5μs from the short circuit duration applied ($T_{sc} = 18$ μs) is observed. Before the appearance of the FTO mode, a gate leakage current (I_{gs}) of 12 mA is measured, although the polarization is reduced to 12 V, to around 2/3 of the T_{sc} . During the short-circuit event, I_{ds} slope variation can be noticed which results in the appearance of the drain leakage current very clear at turn-off. This drain leakage is always clearly visible from 500 V.

Using the direct depolarization method of V_{gs} is not always promising for keeping FTO a value of V_{ds} closer to the nominal value. In Fig. 5, the short circuit characterization of DUT#10 under $V_{buffer} = 11.2$ V and $V_{ds} = 600$ V, shows the appearance of the FTS failure mode which leads to catastrophic damage of the device. This failure mode appears after 4 μs from the applied short circuit duration ($T_{sc} = 19$ μs). Fig. 5 illustrates the waveforms of the various resulting voltages and currents. The appearance of FTS failure mode is linked to the increase of the drain leakage current compared to the results obtained under the $V_{ds} = 550$ V. On the other hand, the gate leakage current ($I_{gsmax} = 10$ mA) is less pronounced compared to the previous test ($I_{gsmax} = 12$ mA at $V_{buffer} = 12$ V) due to the lower applied value of V_{buffer} .

3.2. Gate source voltage estimation methodology

To complete the direct depolarization method of V_{gs} , a second approach is developed to estimate the V_{gs} value permitting to keep the appearance of FTO failure. This approach allows to investigate the critical dissipated power (W/mm²) boundary between FTO and FTS modes, responsible for the the

device failure. The method is based on the results of two single pulse short circuit events. The first one leads to a FTO mode, and the second one induces a FTS mode. The results of SC tests on DUT#8 and DUT#10 are analyzed for

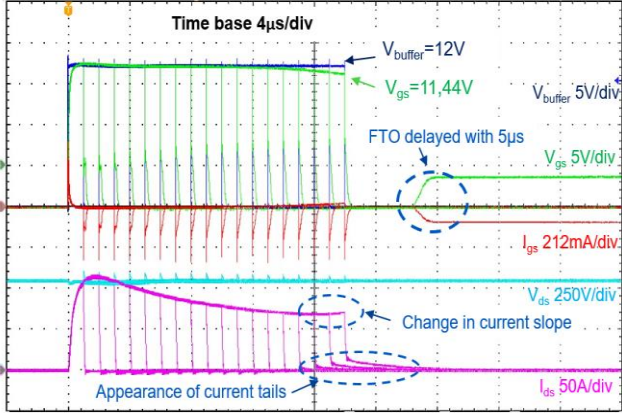


Fig. 4. Experimental waveforms during short circuit of the DUT#8 ($V_{ds}=550$ V; $V_{buffer(on/off)}=+12$ V/ -5 V; $T_{case}=25$ °C; $R_G=47$ Ω).

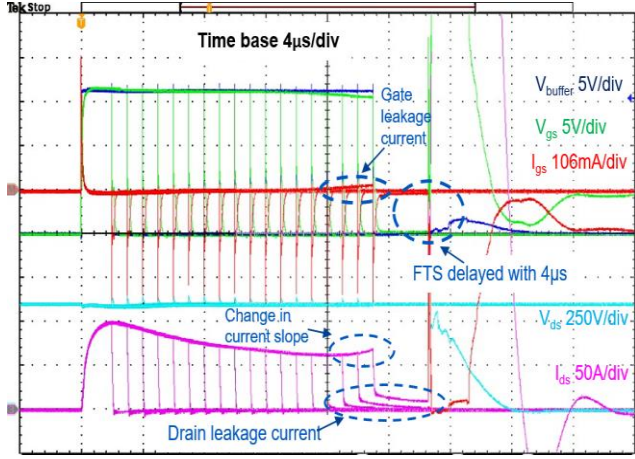


Fig. 5. Experimental waveforms during short circuit of the DUT#10 ($V_{ds}=600$ V; $V_{buffer(on/off)}=+11,2$ V/ -5 V; $T_{case}=25$ °C; $R_G=47$ Ω).

such purpose. The first short circuit event performed on DUT#8, under $V_{ds}=550$ V and $V_{gs}=12$ V, shows a dissipated power of $P_{FTO}=3418$ W/mm² leading to appearance of FTO failure. While the second event carried out on DUT#10, under $V_{ds}=600$ V and $V_{gs}=11.2$ V, presents a dissipated power of $P_{FTS}=4014$ W/mm² leading to appearance of FTS failure. The dissipated power is expressed by equation (2).

$$P = V_{ds} \cdot I_{dsmoy} \quad (2)$$

In small signal of V_{gs} variation, the I_{dsmoy} current can be presented by equation (3).

$$I_{dsmoy} = K_{LV} \cdot (V_{gs} - V_{gsth})^2 \quad (3)$$

where K_{LV} (A/V²) is a constant that represents transconductance

parameter in Low Voltage (LV) of V_{gs} .

For V_{gs} values higher than the threshold voltage V_{gsth} ($V_{gs} \gg V_{gsth}$), the operating device can be placed in the large signal of saturation zone (i.e proportionality relation). Therefore, equation (3) can be expressed by equation (4).

Table 3. Short circuit test results using a V_{gs} estimation method

DUT	#11	#12
V_{ds} (V)	600	600
V_{gs} (V)	10	10
T_{sc} (µs)	24	23
P_{mes} (W/mm ²)	3440	3549
P_{est} (W/mm ²)	3418	3418

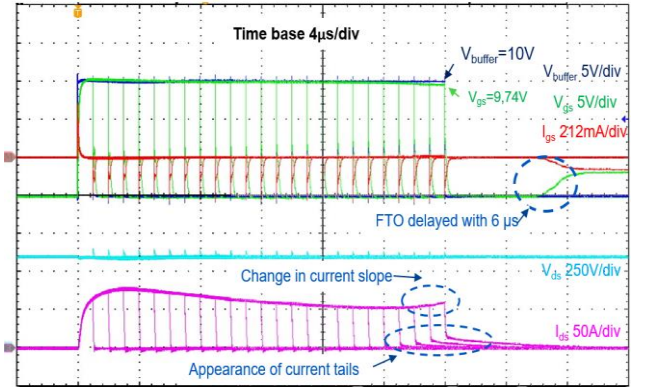


Fig. 6. Experimental waveforms during short circuit of the DUT#11 ($V_{ds}=600$ V; $V_{buffer(on/off)}=+10$ V/ -5 V; $T_{case}=25$ °C; $R_G=47$ Ω).

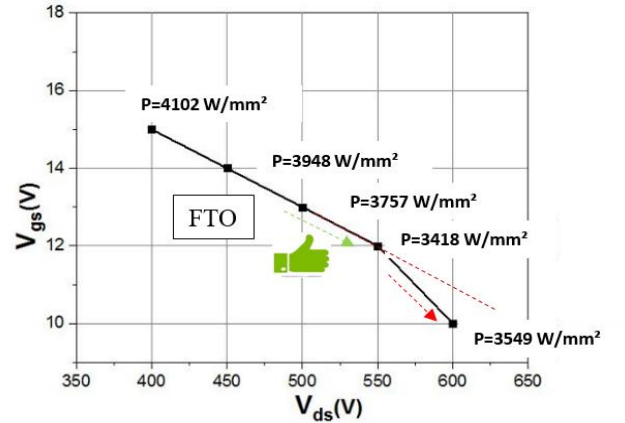


Fig. 7. Evolution of V_{gs} as a function of V_{ds} according to iso-power (P) criterion and FTO failure mode.

$$I_{dsmoy} = K_{HV} \cdot (V_{gs} - V_{gsth}) \quad (4)$$

where K_{HV} is a constant that represents transconductance parameter in High Voltage (HV) of V_{gs} .

Consequently, the dissipated power P is related to V_{gs} voltage through equation (5).

$$P = V_{ds} \cdot K_{HV} \cdot (V_{gs} - V_{gsth}) \quad (5)$$

For DUT#8 that presents a FTO mode under $V_{ds}=550V$, $V_{gs}=12V$, $V_{gsth}=2.61V$ and $P_{FTO}=3418W/mm^2$, the transconductance K_{HV} is calculated as:

$$K_{HV} = K_{FTO} = \frac{P_{FTO}}{V_{ds} \cdot (V_{gs} - V_{gsth})} = 0.661 A/V \cdot mm^2 \quad (6)$$

From this result, we found that the V_{gs} estimated (V_{gs_es}) estimated at $V_{ds}=600V$, using the same P_{FTO} value and is equal to 11.22 V. However, it has been demonstrated that this value of V_{gs_es} induces a FTS mode on DUT#10. The K_{HV} is a posteriori calculated for ($P_{FTS} = 4014 W/mm^2$) and $V_{ds}=600V$.

$$K_{HV} = K_{FTS} = \frac{4014}{600 \cdot (11.22 - 2.61)} = 0.779 A/V \cdot mm^2 \quad (7)$$

Then, V_{gs_es} is estimated more precisely for a test under $V_{ds}=600V$ with a dissipated power leading to a FTO (P_{FTO}) and the calculated K_{FTS} coefficient:

$$V_{gs_es} = \frac{P_{FTO}}{V_{ds} \cdot K_{FTS}} + V_{gsth} \approx 10V \quad (8)$$

This method allows to find the V_{gs} interval which ensures a FTO mode at $V_{ds}=600V$:

$$10V \leq V_{gs_es} < 11.22V \quad (9)$$

To validate this method of V_{gs} estimation from the dissipated power density, the short-circuit test is performed under the voltage $V_{buffer} = 10V$ and $V_{ds} = 600V$ on two DUTs in order to evaluate the repetitiveness of the proposed approach. Table 3 presents the short circuit test duration (T_{sc}), the measured dissipated power (P_{mes}) compared to the estimated dissipated power (P_{est}) that confirm the validity of the new approach for the two DUTs. Fig. 6 illustrates the waveforms results of short circuit test performed on DUT#11. It can be observed that the secure failure mode FTO appears after 6 μs from the applied short-circuit duration ($T_{sc} = 24 \mu s$). The gate leakage current ($I_{gsmax} = 2.5 mA$) is less pronounced compared to the previous test ($I_{gsmax} = 12 mA$ at $V_{buffer} = 12V$ and $I_{gsmax} = 10 mA$ at $V_{buffer} = 11.2V$) given the low value of the applied voltage ($V_{buffer}=10V$). The drain leakage is high because V_{ds} has a high value of 600 V. However, this leakage current remains the same magnitude as for the test for 550V preserving the FTO failure. This observation proves that the applied power density over the duration T_{sc} is preserved to give the same failure mode.

By associating the two approach results presented previously, it can be identified that the damaged devices in FTO mode follows a quasi linear $V_{gs} - V_{ds}$ characteristics (Fig. 7) which becomes improvable at high voltage close to 600 V due to the appearance of a drain leakage causing a delayed FTO/FTS sequence. This trend allows the prediction of V_{gs} that leads to

the appearance of a FTO.

4. Penalty of the V_{gs} depolarization on the $R_{ds(on)}$ resistance

The impact of V_{gs} depolarization approaches on $R_{ds(on)}$ resistance must be investigated. Fig. 8 presents the $R_{ds(on)}$ resistance evolution as a function of the V_{gs} voltage at two

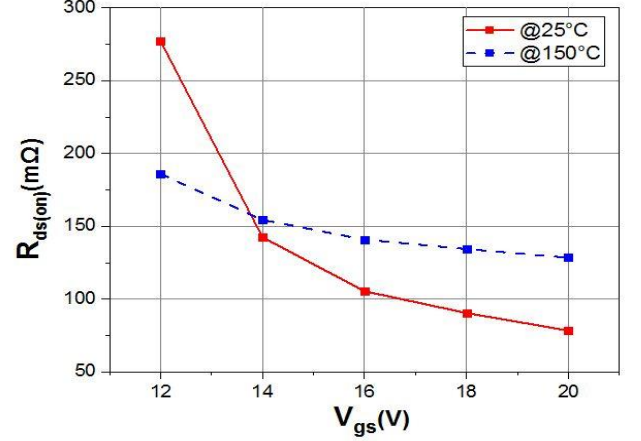


Fig. 8. $R_{ds(on)}$ as a function of V_{gs} at two temperatures 25 °C and 150°C for C2M0080120D device.

temperatures 25 °C and 150 °C. These results were obtained from the datasheet. It can be observed that relative variation of $R_{ds(on)}$ against V_{gs} voltage is +247% at 25 °C and only +44% at 150 °C. Moreover, if we consider that the conduction losses only account 50% of the total losses, thus the V_{gs} depolarization will represent an acceptable impact on $R_{ds(on)}$ @ 150 °C with a 22% ratio. The reduction of the $R_{ds(on)}$ penalty at $T_j = 150 °C$ is physically related to the mobility behavior affected by Coulomb scattering [18]. Indeed, the mobility in the channel is governed at low polarization by Coulomb scattering mechanism which becomes dominant compared to the others mechanisms in particular surface acoustic scattering for the JFET and drift regions. The Coulomb mobility has a positive thermal sensitivity coefficient for a T_{case} range between 25 °C and 200 °C. Therefore, the channel resistance decreases when the case temperature of the chip in operation increases.

However, the other resistances of JFET and drifts regions increase with the temperature rise. Consequently, a compensation effect appears and becomes more effective as V_{gs} is reduced. At a given V_{gs} , there is an optimum case temperature which gives the lowest total value of $R_{ds(on)}$ corresponding to a state of thermal effects compensation between the resistive terms.

5. Conclusion

In this paper, planar gate structure SiC MOSFETs robustness has been experimentally evaluated under short circuit operation. The obtained results confirm the existence of two failure modes (FTO and FTS) for thirteen devices (80mΩ/1.2kV, 2nd Gen).

Two approaches based on direct depolarization of V_{gs} are developed to ensure a secure failure mode FTO at V_{ds} close to the nominal value i.e $V_{BRmin}/2$. The direct depolarization approach shows promising results in terms of short circuit duration (T_{sc}) that exceeds 10 μs , and the appearance of FTO mode taking into account a maximum power density around 3.5 kW.mm⁻². This critical value is identified as the power density boundary between FTO and FTS modes. For these devices, the V_{gs} estimated from the dissipated power calculations leads to a FTO appearance at V_{ds} =600 V. The study of $R_{ds(on)}$ resistance evolution as a function of V_{gs} , shows that V_{gs} depolarization impacts $R_{ds(on)}$ in acceptable way at 150 °C. This approaches have been validated on other current rating devices (25m Ω /1.2kV) and for voltage rating devices (45m Ω /1.7kV) from the same manufacturer. However, the trench gate-structure evaluated did not show satisfying results for V_{gs} depolarization approach. The results may provide useful indicators for converter design and fault protection conditions of SiC power MOSFETs with planar structure.

6. References

- [1] K. Shenai, "The figure of merit of a semiconductor power electronics switch", IEEE Transactions on Electron Devices, vol. 65, no. 10, pp. 4216–4224, Oct 2018.
- [2] X. She, A.Q. Huang, Ó. Lucía, B. Ozpineci, "Review of silicon carbide power devices and their application", IEEE Trans. Ind. Electron. 64 (10) (Oct. 2017) 8193–8205.
- [3] T. Wu, J. Chen, S. Mao, M.J. Schutten, "1200 V SiC MOSFETs for high voltage power conversion", Proc. IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, 2012, pp. 2921–2926.
- [4] D. Othman, S. Lefebvre, M. Berkani, Z. Khatir, A. Ibrahim, A. Bouzourene, "Robustness of 1.2 kV SiC MOSFET devices", Microelectronics Reliability, vol. 53, no. 9-11, pp. pp 1735–1738, Sept.-Nov. 2013.
- [5] M. Riccio, a. Castellazzi, G. De Falco, A. Irace, "Experimental analysis of electro-thermal instability in SiC Power MOSFETs", Microelectron. Reliab. 53 (9–11) (2013) pp.1739–1744.
- [6] A. Castellazzi, A. Fayyaz, L. Yang, M. Riccio and A. Irace, "Short-circuit robustness of SiC Power MOSFETs: Experimental analysis", 2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD), Waikoloa, HI, 2014, pp. 71-74.
- [7] Z. Wang, et al., "Temperature-dependent short-circuit capability of silicon carbide power MOSFETs", IEEE Trans. Power Electron. 31 (2) (Feb. 2016) 1555–1566.
- [8] C. Chen, D. Labrousse, S. Lefebvre, M. Petit, C. Buttay, H. Morel, "Study of short-circuit robustness of SiC MOSFETs, analysis of the failure modes and comparison with BJTs", Microelectronics Reliability. 55 (9–10) (Aug.2015) pp. 1708–1713.
- [9] D. Pappis, P. Zacharias, "Failure modes of planar and trench SiC MOSFETs under single and multiple short circuits conditions", 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Warsaw, 2017 pp. P.1-P.11.
- [10] J. Liu, G. Zhang, B. Wang, W. Li and J. Wang, "Gate Failure Physics of SiC MOSFETs Under Short-Circuit Stress", in IEEE Electron Device Letters, vol. 41, no. 1, pp. 103-106, Jan. 2020.
- [11] F. Boige, F. Richardeau, S. Lefebvre, J.-M. Blaqui re, G. Guibaud, A. Bourennane, "Ensure an original and safe "fail-to-open" mode in planar and trench power SiC MOSFET devices in extreme short-circuit operation", Microelectron. Reliability., vol. 88–90, pp. 598–603, Sep. 2018.
- [12] F. Boige, F. Richardeau, D. Tr mouilles, S. Lefebvre, G. Guibaud. "Investigation on damaged planar-oxide of 1200 V SiC power MOSFETs in non-destructive short-circuit operation", Microelectronics Reliability, Elsevier, 2017, 76-77, pp.500 - 506.
- [13] Cree, C2M0080120D-SiC MOSFET Datasheet, (2015).
- [14] G. Romano, A. Fayyaz, M. Riccio, L. Maresca, G. Breglio, A. Castellazzi, and A. Irace, "A Comprehensive Study of Short-Circuit Ruggedness of Silicon Carbide Power MOSFETs", IEEE J. Emerg. Sel. Top. Power Electron., vol. 4, no. 3, pp. 978–987, Sep. 2016.
- [15] S. Clemente, "Transient thermal response of power semiconductors to short power pulses" in IEEE Transactions on Power Electronics, vol. 8, no. 4, pp. 337-341, Oct. 1993.
- [16] P.D. Reigosa, F. Iannuzzo, L. Ceccarelli, "Effect of short-circuit stress on the degradation of the SiO2 dielectric in SiC power MOSFETs", Microelectron Reliability 88–90 (2018) 577–583
- [17] A. J. Lelis, D. Habersat, R. Green, A. Ogunniyi, M. Gurfinkel, J. Suehle, N. Goldsman, "Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements" in IEEE Transactions on Electron Devices, vol. 55, no. 8, pp. 1835-1840, Aug. 2008.
- [18] S L Rummyantsev, M S Shur, M E Levinshtein, P A Ivanov, J W Palmour, A K Agarwal, B A Hull and Sei-Hyung Ryu, "Channel mobility and on-resistance of vertical double implanted 4H-SiC MOSFETs at elevated temperatures", Semiconductor Science and Technology. vol24.no 4.075011, 2009.