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# Analysis and mitigation of timing inaccuracies in high-frequency on-chip sinusoidal signal generators based on harmonic cancellation

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**Abstract**—On-chip sinusoidal signal generators are a key element for enabling a wide variety of DfT and BIST applications for AMS-RF integrated circuits. Harmonic cancellation techniques have been recently proposed for the efficient implementation of high-quality embedded sinusoidal signal generators. However, harmonic cancellation techniques, based on phase-shifting and combining a set of periodic signals, rely on precise and accurate phase-shift control which makes them very sensitive to timing issues due to mismatch, noise, etc. Timing issues can severely limit the performance of these generators especially in high-frequency applications where precise timing becomes challenging. In this paper, we analyze the effects of timing inaccuracies on high-speed harmonic cancellation generators and we propose circuit techniques for mitigating them. Electrical simulation results on a 1.45 GHz sinusoidal signal generator implemented in ST 28 nm FDSOI technology are provided to validate our proposals.

## I. INTRODUCTION

Current nanometric CMOS technologies enable the integration of complex mixed-signal systems onto a single chip. However, these advanced CMOS manufacturing processes are prone to imperfections which can lead to a degradation of the system performance or even to malfunctions. Extensive production testing is needed in order to guarantee the functionality of the fabricated ICs. However, the wide circuit variety in current SoCs including analog, mixed-signal, RF and digital building blocks makes test a challenging task. Moreover, accessing these building blocks from the outside for testing purposes may be challenging or even impossible due to the high integration level in current SoCs.

Built-In Self-Test (BIST) techniques may be a solution to the aforementioned issues. BIST techniques take into account the test of each building block of a complex SoC at the design stage by integrating some tester capabilities together with each block. Thus, the external access problem can be solved and each building block becomes self-testable. Moreover, a built-in test can help in diagnosing the source of the failure and thereby can help in enhancing the production yield through appropriate actions. It also enables an on-field test of the ICs to monitor their health in safety-critical and mission-critical applications.

A wide variety of test techniques for AMS-RF circuits are based on the application of high-quality sinusoidal test stimuli. Indeed, moving sinusoidal stimulus generators on-chip has

been repeatedly identified as one of the main blocking points for moving many AMS-RF tests to a practical BIST scheme. In this sense, recently proposed on-chip sinusoidal signal generators make use of harmonic cancellation techniques in order to reduce circuit complexity—in some cases relying mostly on digital circuitry—while providing a highly-linear output signal [1]–[9]. Harmonic cancellation techniques are based on combining a set of delayed and weighted versions of a given periodic signal in order to cancel out the most significant undesired harmonic components in the original periodic signal [10]. The technique can be successfully applied using digital square waves as the original periodic signal [3]–[9]. This makes this technique very suitable for a digital-friendly integration of AMS-RF test techniques.

However, the effectiveness of the harmonic cancellation relies on the accuracy of the introduced delays and weights. As the operating frequency increases, inherent timing inaccuracies may severely limit the performance of these integrated generators. That would be the case for high-speed AMS-RF circuits such as high-speed ADCs, RF front-ends, etc. that operate at the GHz frequency range. In this paper, we analyze in detail the effects of timing inaccuracies in high-speed harmonic cancellation-based generators and propose two circuit-level techniques for mitigating the effect of these timing inaccuracies on the harmonic cancellation effectiveness.

The rest of the paper is organized as follows. In Section II we present relevant previous work on sinusoidal signal generation based on harmonic cancellation. In Section III we explain the principle of the harmonic cancellation technique. In Section IV we analyze the effect of timing inaccuracies in harmonic cancellation techniques and discuss its impact as a function of the operating frequency. In Section V, we present a practical implementation at transistor level for the generation of precise square-wave phases including circuit-level techniques for mitigating timing inaccuracies. The feasibility of the proposed circuitry is validated with electrical simulations. Finally, Section VI summarizes our main contributions.

## II. PREVIOUS WORK

Harmonic cancellation techniques have been widely employed in the last few years for the implementation of on-chip sinusoidal signal generators due to the reduced complexity and enhanced performance that can be achieved compared

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to other architectures [1]–[7], [9]. Although each particular implementation may vary, these signal generators share the same operating principle. The output sinusoidal signal is built by combining time-delayed and scaled versions of a periodic signal in such a way that low-order harmonic components are canceled, while a lowpass output filter is employed to attenuate higher-order harmonics. Thus, the works in [1], [2] employ analog circuitry to delay and combine scaled versions of an analog sine-wave signal. The generated output sinusoid shows a very good linearity with THD figures below  $-75$  dB at an output frequency around 1 MHz for the integrated solution in [2] and below  $-90$  dB THD at 3 kHz for the discrete-component implementation in [1].

The works in [3]–[7], [9], on the other hand, rely on digital circuitry and employ time-shifted versions of a digital square wave as the base signal for the harmonic cancellation. The generation of these time-shifted square-waves can be easily performed in the digital domain, while the scaling and combination of the different signals is carried out using some Digital-to-Analog architecture. Thus, [3], [4] proposes a simple digital counter for generating the time-shifted signals. These signals are then scaled and added using a complete current-steering DAC circuit. The limitation of this architecture comes from the mismatch in the DAC weights which can reduce the linearity of the output signal. To mitigate the mismatch issues in the DAC, a partial dynamic element matching is proposed in [4]. Reported results show a THD below  $-40$  dB for a generated signal at 20 MHz.

The works in [5], [7], [9] target higher generated frequencies in the range of hundreds of MHz. Thus, [5] employs a ring oscillator for generating time-shifted square-wave signals while a weighted resistor summing network is used to scale and combine these time-shifted signals in the analog domain. However, due to the mismatch and process variations, the ring oscillator is prone to timing errors in the duty cycle and the relative phase-shift of the generated signals. To mitigate this issue, authors propose a calibration circuit that corrects timing inaccuracies with the help of external feedback. The THD of the output signal reported in this work is  $-57$  dB at 650 MHz and  $-62$  dB at 750 MHz after calibration. On the other hand, the work in [7], [9] proposed an efficient sinusoidal signal generator that employs a simple circular shift-register for generating a set of time-shifted digital square-waves, while a simplified current steering DAC with conversion weight calibration was employed to scale and combine these signals. Experimental results on an integrated prototype demonstrate a THD of  $-46$  dB at 330 MHz, being fundamentally limited by timing inaccuracies.

In this work, we explore the application of harmonic cancellation techniques for the implementation of sinusoidal signal generators in the GHz frequency range. Increasing the output frequency of this family of generators to these frequencies could open the door to novel high-frequency BIST for a wide variety of applications. However, enabling this frequency increase requires a careful analysis of timing inaccuracies and dedicated compensation circuitry to avoid a significant

degradation of the generated signal spectral performance.

### III. THEORETICAL BASIS

#### A. Harmonic cancellation

As already mentioned in previous sections, the fundamental principle of the harmonic cancellation technique is that it is possible to cancel a set of harmonic components in a periodic signal by adding time-shifted and scaled versions of this signal. In the following, we restrict our analysis to square-wave signals due to the inherent simplicity of generating these signals in the digital domain.

Let us consider that signal  $q(t)$  is a periodic square-wave signal with unit amplitude, an ideal 50% duty cycle and period  $T$ . Ignoring the DC level component, this signal can be represented as a Fourier series as,

$$q(t) = \sum_{n=1,3,5,\dots}^{\infty} \frac{2}{n\pi} (-1)^{\frac{n-1}{2}} \cos(n\omega_0 t), \quad (1)$$

where  $\omega_0 = 2\pi/T$  is the frequency of the square wave. Let us define signal  $y(t)$  as the linear combination of signal  $q(t)$  and  $p$  pairs of versions of signal  $q(t)$  time-shifted in opposite directions  $t_i$  and  $-t_i$  and scaled by a factor  $\alpha_i$ , that is

$$y(t) = q(t) + \sum_{i=1}^p \alpha_i [q(t + t_i) + q(t - t_i)]. \quad (2)$$

From equations (1) and (2), signal  $y(t)$  can be written as,

$$y(t) = \sum_{n=1,3,5,\dots}^{\infty} \frac{2}{n\pi} (-1)^{\frac{n-1}{2}} \left[ 1 + 2 \sum_{i=1}^p \alpha_i \cos(2n\pi \frac{t_i}{T}) \right] \times \cos(n\omega_0 t) \quad (3)$$

From equation (3) we can observe that the spectrum of signal  $y(t)$  is similar to the spectrum of signal  $q(t)$  but with an amplitude for the  $n$ -th harmonic that is a function of the scale factors  $\alpha_i$  and the time-shifts  $t_i$ . Thus, by selecting an appropriate set of time shifts  $t_i$  and scale weights  $\alpha_i$  it should be possible to make

$$\left[ 1 + 2 \sum_{i=1}^p \alpha_i \cos(2n\pi \frac{t_i}{T}) \right] = 0, \quad (4)$$

for a given value (or set of values) of  $n$ , effectively canceling the  $n$ -th harmonic (or harmonics) in signal  $y(t)$ .

#### B. Conceptual implementation

The described harmonic cancellation technique can be easily extended to the generation of high-linearity sinusoidal signals. Indeed, starting from a digital square-wave, we can cancel low-order harmonics using the harmonic cancellation while higher-order harmonics can be attenuated using a low-pass filter. Assuming  $p$  pairs of the scaled and delayed square-wave signal  $q(t)$  we can easily derive from (4) the required  $\alpha_i$  and

$\phi_i = 2\pi t_i/T$  to cancel all odd harmonics below the  $2(2p+1)$ -th harmonic as

$$\begin{cases} \phi_i = i \frac{2\pi}{4(p+1)} & 1 \leq i \leq p \\ \alpha_i = \cos(i \frac{2\pi}{4(p+1)}) & 1 \leq i \leq p. \end{cases} \quad (5)$$

Equation (5) shows that there is a trade-off between the number of required time-shifted pairs of signals  $p$  and the number of harmonics that can be canceled, and consequently with the selectivity of the output filter that should cancel the higher-order harmonics not affected by the harmonic cancellation. The reader is referred to [8] for a study of different solution families to the harmonic cancellation equation. A particular solution that offers a good trade-off between complexity and cancellation performance is the use of  $p = 2$  pairs of time-delayed square-waves (i.e., 5 signals) with opposite phase-shifts  $\phi_1 = \pm \frac{\pi}{6}$  and  $\phi_2 = \pm \frac{\pi}{3}$  and scale weights  $\alpha_1 = \frac{\sqrt{3}}{2}$  and  $\alpha_2 = \frac{1}{2}$ . As a case study, this particular solution will be employed in the rest of the paper for the cancellation of all odd components below the  $10^{\text{th}}$  harmonic.

#### IV. EFFECT OF TIMING INACCURACIES IN HARMONIC CANCELLATION

The performance of a practical implementation of the harmonic cancellation technique using current integrated technologies is unavoidably limited by a number of fabrication non-idealities. Thus, mismatch and process variations can affect the effectiveness of the harmonic cancellation by deviating critical parameters like the square-wave duty cycle, phase difference, or scalar weights from the ideal values defined by (5). This section analyzes the effect of the main non-idealities that may degrade the harmonic cancellation performance. Some of these non-idealities have been considered previously in the low-frequency scenario [1]–[4] resulting in a predominance of the weight-mismatch as the main cause of linearity degradation. In the present paper, we analyze for the first time high-frequency applications and we show how this previous result no longer holds. This is because timing inaccuracies become the main limiting factor.

##### A. Static Phase Error (SPE)

Due to fabrication inaccuracies, the relative phase-shift between the square-waves that is required for the harmonic cancellation may deviate from the ideal values defined by (5). In our analysis we define the Static Phase Error (SPE) as the variation in the relative phase between the square-waves in the harmonic cancellation scheme. Let us consider that  $\phi_i$  and  $\alpha_i$ ,  $i = 1, \dots, p$  are the phase-shifts and scale-weight factors required for canceling the  $n$ -th harmonic component. If the relative phase-shifts are affected by an error  $\delta_{\phi_i}$ , the magnitude of the  $n$ -th harmonic component (normalized to the amplitude of the original square-wave),  $A_n$ , of signal  $y(t)$  will not be canceled,

$$A_n \simeq \frac{4}{\pi} \sum_{i=1,3,5,\dots}^p \alpha_i \delta_{\phi_i} \sin(n \phi_i) \quad \text{for } n = \text{odd} \quad (6)$$

It is interesting to note that the magnitude of the resulting harmonic component is a linear combination of the phase error terms  $\delta_{\phi_i}$  and that static phase error does not introduce even harmonic components, as the symmetry of the signals is not affected.

##### B. Duty Cycle Variation (DCV)

Fabrication inaccuracies can also affect the duty-cycle of the square-waves in the harmonic cancellation scheme, usually due to an imbalance between the rise and fall times. In this case, even harmonic components also appear at the spectrum of signal  $y(t)$  as

$$A_n = \frac{2}{n\pi} |\sin(n\pi d)| \left[ 1 + 2 \sum_{i=1}^p \alpha_i \cos(n \phi_i) \right], \quad n = 1, 2, \dots \quad (7)$$

where  $d$  is the duty cycle of the square-wave defined as the ratio between the time in the ‘‘high’’ state and the square-wave period. It is interesting to notice that DCV does not have any effect on the harmonic cancellation, but degrades the spectral quality by introducing even order harmonics.

##### C. Mismatch Variation (MV)

Mismatch can cause the scaling-weights  $\alpha_i$  to deviate from their ideal values. This deviation has a direct impact on the harmonic cancellation condition (4). If we consider that each scaling weight factor is affected by a deviation of  $\delta_{\alpha_i}$ , then the magnitude of the  $n$ -th harmonic component in the generated signal  $y(t)$  can be expressed as

$$A_n = \frac{4}{n\pi} \sum_{i=1,3,5,\dots}^p \delta_{\alpha_i} \cos(n \phi_i) \quad \text{for } n = \text{odd} \quad (8)$$

Interestingly, scale-weight mismatch does not have an impact on the even harmonic components, and the magnitude of the resulting harmonic components is a linear combination of the mismatch error terms  $\delta_{\alpha_i}$ .

##### D. Jitter

In any practical implementation, each of the square-wave signals in the harmonic cancellation scheme will be affected by jitter. That is, the actual position of the rise and fall edges will be noisy. This noise can be random or deterministic in nature, and it will increase the noise floor of the generated signal  $y(t)$ . However, it has no effect on the effectiveness of the harmonic cancellation. For previously reported low-frequency generators jitter had no significant impact since it does not degrade the THD of the output. However, as we move higher in frequency the increase in the noise floor can dramatically reduce the SINAD of the generated output.

##### E. Finite rise and fall times

Practical square-wave signals will have non-ideal (i.e., finite) rise and fall times  $t_r$  and  $t_f$ , respectively. In the particular case in which  $t_r = t_f$ , this is actually beneficial for the proposed application. A finite transition time has a

filtering effect in the high-frequency harmonic components of the original square-wave signal in (1) with a roll-off of  $-40$  dB/dec from frequency  $f = 1/(\pi t_r)$ . If  $t_r \neq t_f$ , then the duty-cycle will deviate from 50% and this roll-off effect is superimposed on the appearance of even-order harmonics.

#### F. Case Study

In order to quantify the role of these effects in a practical harmonic cancellation case study, we implemented a behavioral model in Matlab for a 5-phase sinusoidal signal generator. As mentioned before, for this case study we will employ a reference square-wave and  $p = 2$  pairs of phase-shifted versions with  $\phi_1 = \pm \frac{\pi}{6}$  and  $\phi_2 = \pm \frac{\pi}{3}$  and scale weights  $\alpha_1 = \frac{\sqrt{3}}{2}$  and  $\alpha_2 = \frac{1}{2}$ , using the notation in the previous Section. This solution allows the cancellation of all odd components below the 10<sup>th</sup> harmonic. A first-order lowpass filter whose pole has been located at the output fundamental frequency is included to filter higher-order harmonics.

In a first set of experiments, we have carried out a worst-case corner analysis using the presented behavioral model in order to analyze and compare the effect of the static phase error, duty-cycle variation and scale-weight mismatch. Figure 1 shows the obtained worst-case THD for the generated output sine-wave as a function of the maximum percentage of variation for each effect. The percentage variation of SPE is the variation of the relative phase with respect to the period of the original square-wave, duty-cycle is naturally expressed as a ratio to the signal period and mismatch variations are referred to the ideal  $\alpha_i$  factors. In absolute terms, it is clear to observe that timing errors (i.e., phase and duty cycle variations) drastically degrade the linearity of the generated sine-wave, while the effect of scale-weight mismatch remains more limited. However, these results should be interpreted relative to the operating frequency of the generator. Thus, if we consider a low-frequency scenario, SPE and DCV percentage variations become negligible as the signal period becomes larger, and the linearity of the output signal becomes effectively limited by the mismatch errors. This is the case for previously reported low-frequency generators such as [1], [2] which report THD figures below  $-75$  dB in the frequency range from 3 kHz to 1 MHz. As we move to higher operation frequencies, timing errors become dominant: the signal period decreases while the achievable timing resolution and component mismatch keep approximately constant for a given technology. If we refer to Fig. 1, increasing the operating frequency has the effect of moving the design point to the right along the X-axis for the SPE and DCV curves, which dramatically decreases the linearity of the output signal.

In a second set of experiments, we evaluated the effect of random and deterministic jitter in the square-wave signals employed in the harmonic cancellation scheme. Thus, Fig. 2 shows the degradation of the generated sine-wave SINAD as a function of the RMS value of the injected random jitter. Similarly, Fig. 3 shows the SINAD degradation when deterministic sinusoidal jitter is injected in the square-wave signal. As it can be seen, a practical implementation should

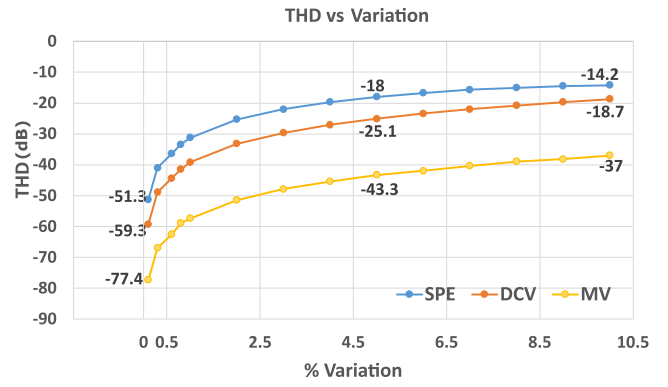


Fig. 1. Generated output THD as function of timing and mismatch errors.

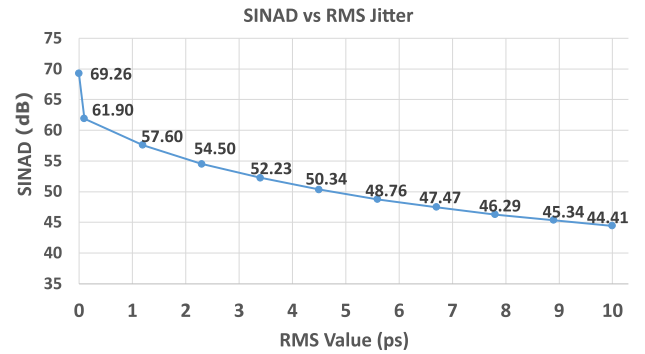


Fig. 2. Generated output SINAD in the presence of random jitter, as a function of the jitter RMS value.

consider this degradation mechanism to avoid increasing the noise floor of the generated signal, even if the THD is not affected.

#### V. PRACTICAL IMPLEMENTATION INCLUDING MITIGATION OF TIMING INACCURACIES

In the view of the results obtained in the previous section, it is clear that a practical implementation of a harmonic

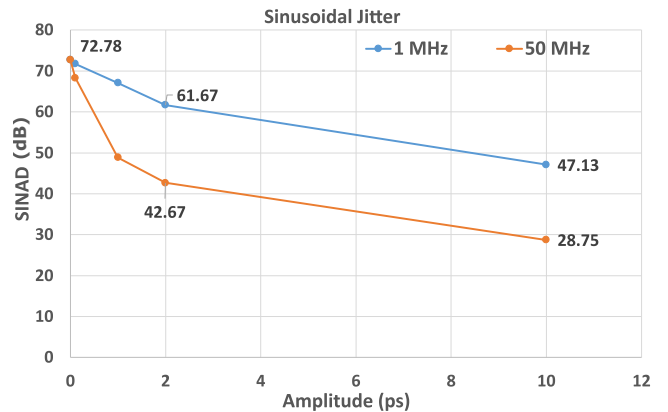


Fig. 3. Generated output SINAD in the presence of sinusoidal jitter, as a function of the sinusoidal jitter amplitude and frequency, for a generated signal at 1.4 GHz.

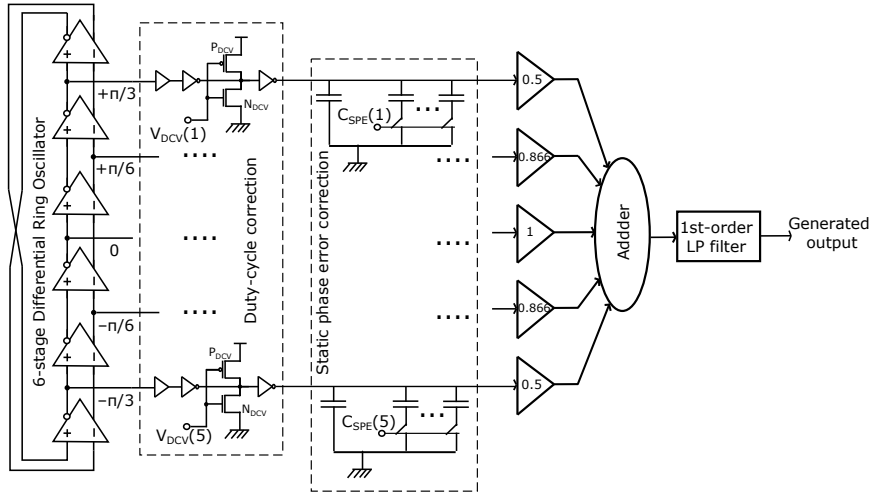


Fig. 4. Block diagram of the proposed harmonic canceling sinusoidal signal generator including duty-cycle and static phase error correction.

canceling generator targeting high-frequency operation has to carefully consider any timing issues that would otherwise limit the linearity of the generated signal. This explains the limited performance of previously reported generators at higher frequencies such as [4], [9] that rely only on a calibration of the scaling weights, while the performance is actually limited by timing inaccuracies. Better results are obtained in [5] due to the introduction of timing calibration. However, the proposed tuning knob cannot decouple duty-cycle and phase errors which in the end may have hindered the output linearity.

In the present work, we propose a practical transistor-level implementation of a square-wave phase generator for harmonic cancellation applications that includes separate circuit solutions for the mitigation of phase errors and duty-cycle variations. This case study implementation will target the 5-phase harmonic cancellation generator already presented in the previous sections. Fig. 4 shows a block diagram of the proposed generator. A 6-stage differential ring oscillator is employed for generating the required 5 phases ( $\phi_0 = 0$ ,  $\phi_1 = \pm \frac{\pi}{6}$  and  $\phi_2 = \pm \frac{\pi}{3}$ ) shown in Fig. 4. Subsequently, dedicated duty-cycle and phase error mitigation circuits are employed to calibrate timing inaccuracies in the generated square-waves. Finally, the calibrated phases are scaled, combined and filtered by a low-pass output filter in order to generate an analog sinusoidal signal at the output. The pole of the output filter has been placed at the fundamental frequency. Since the main focus of this paper is the mitigation of timing inaccuracies, in order to offer a realistic validation, the ring oscillator and the mitigation circuitry have been implemented at transistor level in ST 28 nm FDSOI technology. The implementation of the rest of the generation circuitry (weighted sum of the generated phases and filtering) is out of the scope of this paper and has been modeled at behavioral level using VerilogA.

The ring oscillator has been sized and biased for an oscillation frequency around 1.4 GHz. To our knowledge, this is the first time that this generation strategy is pushed to the GHz frequency band. As mentioned before, targeting such a high operating frequency requires the use of mitigation strategies

for timing inaccuracies. In this regard, we present two circuit-level mitigation solutions for compensating static phase errors and duty cycle variations.

#### A. Mitigation of duty-cycle variation

The proposed duty-cycle correction circuit is based on a pulse-width modification circuit adapted from the work in [11]. The proposed circuit consists of a chain of inverters as depicted in Fig. 4. Firstly, each of the phases generated by the ring oscillator is buffered and fed to the correction circuit. The buffers are required since the correction in the duty cycle and the phase should not affect the internal nodes of the oscillator. Otherwise, the phase and frequency of the oscillator can be affected. The duty-cycle of each of the generated phases is then controlled by the input analog voltage  $V_{DCV}(i)$  applied to an inverter in parallel to the buffers. When the  $V_{DCV}(i)$  voltage is increased, the NMOS transistor  $N_{DCV}$  compensates the current of the NMOS transistor in the previous inverter and similarly, when the  $V_{DCV}(i)$  voltage is decreased, the PMOS transistor  $P_{DCV}$  compensates the current of the PMOS transistor of the previous inverter. The circuit has been sized to achieve a tunability range around  $\pm 5\%$  duty cycle variation across the technology corners.

#### B. Mitigation of static phase error

The mitigation of the static phase error is achieved by loading the output of the duty-cycle correction circuit by a variable capacitor array as depicted in Fig. 4. This way, the digital control word  $C_{SPE}(i)$  can effectively advance or delay the generated square-waves. The capacitor array has been sized in order to correct phase errors up to  $\pm 5\%$ . It is important to notice that the output buffers in the duty-cycle calibration circuit actually decouple the two calibration knobs so there is no degradation of the duty-cycle due to phase error corrections. Moreover, the capacitive loading has also the added effect of slowing the rise and fall times of the square-wave, which further reduces the magnitude of high-frequency harmonic components as described in the previous section.



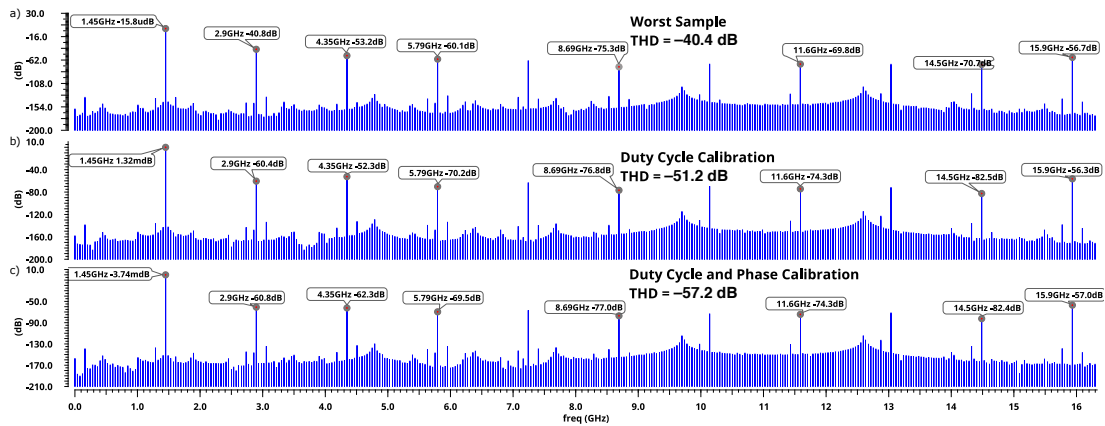


Fig. 5. Frequency Spectrum of the generated sinusoidal signal: a) Uncalibrated; b) Duty-cycle correction; c) Duty-cycle and static phase error corrections

### C. Results

In order to show the feasibility and performance of the proposed phase-generation circuitry, we run a set of 200 Monte Carlo simulations of the complete sinusoidal signal generator in Fig. 4 using the Monte Carlo process and mismatch models in the PDK of the selected ST 28 nm FDSOI technology. The obtained linearity is expressed in terms of the THD of the generated sinusoidal signal. The THD has been computed up to the 10<sup>th</sup> harmonic component since the proposed harmonic cancellation technique is targeted at the cancellation of the odd harmonics up to the 9<sup>th</sup> component. The nominal run results in a 1.45 GHz sinusoidal signal with a THD of  $-61$  dB. However, due to process and mismatch variations, the timing inaccuracies severely degrade this nominal performance. The worst-case uncalibrated THD in our Monte Carlo simulations was  $-40$  dB. The output spectrum of the uncalibrated worst-case generated signal is shown in Fig. 5a up to the 11<sup>th</sup> harmonic component. In order to show the viability of the proposed correction circuit, Fig. 5b and c show the spectral improvement of the output signal when the duty-cycle and both the duty cycle and the phase errors are corrected, respectively. As it can be seen, the correction of the duty cycle improves the THD to  $-51$  dB, which represents an 11 dB improvement. It is clear to see the improvement of the second and fourth harmonic components which are reduced by  $-20$  dB and  $-10$  dB, respectively. Correcting both duty cycle and phase errors further improves the THD of the generated output to  $-57$  dB, which represents an improvement of 17 dB with respect to the uncalibrated generator. It is interesting to notice that even order harmonics are not affected by the phase error tuning and only odd order harmonics are improved. The orthogonality of the tuning knobs is a property that can simplify a future on-chip calibration scheme for this family of generators.

## VI. CONCLUSIONS

In this work we have analyzed in detail the effect of timing inaccuracies in the linearity of harmonic canceling sinusoidal signal generators. The presented analysis has shown that the effectiveness of harmonic cancellation techniques in

high-frequency applications is dramatically affected by timing errors. In this context, we have presented two circuit solutions for the mitigation of these timing inaccuracies. The feasibility and performance of these correction circuits are demonstrated at transistor level in a case study application considering a 5-phase harmonic cancellation scheme.

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