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Integrated Wideband Millimeter-Wave Bias-Tee – Application to Distributed Amplifier Biasing

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Abstract— A wideband fully-integrated bias-tee well suited for millimeter waves is presented. Compared to conventional bias-tees, where RF-choke is optimized on the basis of its inductance value, here, the proposed RF-choke takes advantage of its low parasitic capacitance as one of the design parameters. While enabling wideband operation, in particular towards lower frequencies, this bias-tee enables ease-of-implementation, robustness against resonance, efficient power delivery to the intended wideband circuit and contributes to circuit area reduction on integrated circuit (IC) implementation. As a proof-of-concept, a wideband CMOS distributed amplifier (DA) with a lower-corner frequency (F_{lower}) of 5 GHz and an upper-corner frequency (F_{upper}) close to 100 GHz is implemented in STMicroelectronics' 55-nm technology with the proposed bias-tee connected to its artificial drain line. The implemented bias-tee enabled a bandwidth close to 100 GHz and its RF-choke required a surface area of $82 \mu\text{m} \times 82 \mu\text{m}$. When integrated along with the DA, the overall chip area remained the same (0.89 mm^2). Post-layout simulations showed a DC power overhead (due to inclusion of the on-chip bias-tee) limited to 17% of the DA-only consumption.

Keywords— Wideband, on-chip, high capacitive-reactance, RF-choke, fully integrated, bias-tee, CMOS, broadband, distributed amplifier.

I. INTRODUCTION

Millimeter-waves frequency bands are of major interest for various applications such as high-speed optical links [1], imaging systems [2] and even medical applications [3]. In the context of wideband circuits, the demand for fully integrated, low-cost and power efficient system is increasing with the surge of wireline and optical high data links. For instance, throughout the years, publications showed the effort dedicated to designing wideband distributed amplifiers in low-cost silicon technologies. Such systems are proven to provide bandwidths exceeding 50 GHz [4] or even 100 GHz [5]-[6] starting from DC [7] or very low frequencies. They are compact (fully integrated), offer wideband matching and gains as large as 30 dB [6]. Wideband circuits are followed, however, by challenges when it comes to designing their DC supply network, especially in the context of power efficient fully integrated devices, in which high Q passives are not available.

A compact way of obtaining a wideband biasing network is by using integrated resistive elements as RF-chokes [7].

With this approach, a series resistance is used to inhibit RF signals from leaking towards bias circuitry. This approach benefits from allowing the lower-corner frequency to be extended down to 0 Hz. However, it is power consuming because the supply voltage V_{DD} needs to be increased as to compensate for the voltage drop across this series resistance and preserve the same operating point of the biased circuit. External bias-tees with large inductance are commonly used, such as in [4], [5] and [8], to mitigate this issue owing to their attractive low DC-resistance while providing high reactance that chokes RF signal. This technique, however, requires the use of a bulky and expensive off-chip inductor not suited for fully integrated systems. Embedding a large spiral inductor as part of the design to avoid cost penalty, such as in [9], is suited for relatively small operational bandwidths where they can be positioned below SRF (self-resonant frequency) [10], but this integrated solution may become problematic when dealing with several tens of gigahertz bandwidth where having the SRF inside passband could alter the circuit's behavior. Shifting this SRF outside such wide passband is considered challenging, especially when the intended circuit to be biased operates up to 100 GHz, for example.

In this paper, a compact fully-integrated wideband bias-tee suited for wideband millimeter-waves circuits is proposed and demonstrated by means of a DA design example implemented in CMOS technology and reaching frequencies up to 100 GHz. Compared to conventional approaches where intended circuits to be biased are designed independently as a first step and then bias-tees are implemented to provide high impedance RF-chokes across full bandwidth, here the proposed bias-tee is designed as part of the main circuit and inhibits the RF signal from leaking to bias circuitry by originally taking advantage of the parasitic capacitance of the reactive RF-choke itself. In addition, the paper intends to demonstrate the concept and proposes design equations which could be straightforwardly transposed to other wideband circuits. The paper is organized as follows. The proposed bias-tee's design concept and analytical methodology are presented in Section II, followed in Section III by a design implementation example with a 100-GHz CMOS DA using STMicroelectronics's eight-metal 55-nm process. Here the post-layout simulations are shown, and a comparison with other DAs' employing different biasing approaches is done. Finally, a conclusion is provided in Section IV.

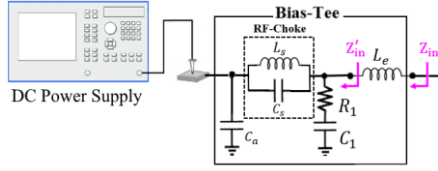


Fig. 1. Proposed bias-tee topology.

II. DESIGN CONCEPT AND METHODOLOGY

Fig. 1 illustrates the lumped-element equivalent network representation of the bias-tee under study. In this paper, this biasing circuit is intended to be matched to a resistor R_1 , typically of $50\text{-}\Omega$ impedance that is required in almost all wideband circuits as a reference impedance, but the concept could be extended to any other impedance magnitude. For the sake of simplicity in illustrating the proposed bias-tee's concept and design methodology, analytical expressions are first presented, and then, in a second step, practical implementation is discussed.

A. Analytical expressions

Typically speaking, the bias-tee's RF-choke is designed such that its SRF is pushed above the biased circuit's upper-corner frequency (F_{upper}) while providing sufficiently high inductive reactance across its passband. This is usually achieved by optimizing the structure on the basis of L_s while trying to diminish RF-choke's parasitic C_s . Our proposed way, however, takes advantage of the SRF instead of suffering from it. This is done by making use of RF-choke's parasitic capacitance C_s and considering it now as a design parameter while pushing bias-tee's overall resonance below the biased circuit's lower-corner frequency (F_{lower}). For this reason, the bias-tee of the proposed approach could be viewed as having a 'capacitive-reactance RF-choke', i.e. mostly operating in the capacitive region established by low C_s . In the proposed bias-tee, shunt capacitor C_a is added as a filtering capacitor to protect the integrated system against any impedance perturbation that comes from DC power supply and its wiring. Capacitors C_a and C_1 own parasitic is not considered herein, being negligible as compared to L_s - C_s tank elements. Finally, the purpose of adding L_e , a small value inductor, will be explained further in (8) and is first ignored in the following derivations.

In a first approach, L_s and C_s are being considered as independent parallel components. As a matter of fact, the relationship between both will be discussed in the next section when dealing with practical implementation, helping to choose adequately the RF-choke's parameters. The tank's reactance is found to be equal to (2).

$$Z_{tank} = \frac{-j}{\omega C_s (1 - (\frac{\omega_{tank}}{\omega})^2)}, \quad (2)$$

$$\text{where } \omega_{tank} = 1/\sqrt{L_s C_s}$$

By ignoring L_e , and if C_a is chosen large enough to be safely assumed as an AC-connection to ground for the whole passband, the bias-tee's equivalent input impedance is derived first from Z'_{in} in (3). Emphasis was put intentionally here on the parasitic capacitance C_s as a design parameter, instead of L_s .

$$\begin{aligned} \text{Re}\{Z'_{in}\} &= R'_{in} = R_1 \frac{C_1^2}{\Delta} \\ \text{Im}\{Z'_{in}\} &= X'_{in} = -\frac{1}{\omega} \cdot \frac{C_1 + \beta C_s + \omega^2 \beta C_s C_1^2 R_1^2}{\Delta} \end{aligned} \quad (3)$$

$$\text{where } \beta = 1 - (\omega_{tank}/\omega)^2,$$

$$\Delta = (C_1 + \beta C_s)^2 + (\omega \beta C_1 C_s R_1)^2$$

Z'_{in} is in the form of $R'_{in} \pm j|X'_{in}|$. For matching purpose, $|X'_{in}|$ should be almost equal to 0 while R'_{in} should not vary far from R_1 , across the considered bandwidth. Up to this point, an additional relationship between C_s and β is necessary to pursue the proposed bias-tee design; it can be obtained through practical implementation considerations.

B. Practical implementation

As an illustration, the targeted bandwidth will range from $F_{lower} = 5$ GHz up to $F_{upper} = 100$ GHz, with $R_1 = 50 \Omega$. The RF-choke is a homemade microstrip spiral inductor using the eighth metal layer of STMicroelectronics' 55-nm technology, with a fixed coil width of $2 \mu\text{m}$, coil area of $82 \mu\text{m} \times 82 \mu\text{m}$, and $0.55 \mu\text{m}$ spacing between metallic windings, with varying number of turns. Fig. 2 gives the self-resonance frequency, SRF , of the simulated spirals on ANSYS' HFSS as well as their DC resistance. By curve fitting the collected SRF to L_s , an empirical expression is formulated in (4).

$$SRF = \frac{\omega_{tank}}{2\pi} = 3.778 * 10^4 L_{s(H)}^{-0.6479} + 4.355 * 10^9 \quad (4)$$

Equation (4) is optional, but simplifies the design task by relating C_s and β to any implemented spiral design through its SRF . Another possible way could be to iterate through multiple 3-D electromagnetic (EM) simulations and extract C_s and β for each spiral inductor winding turns. Both C_s and β are given by (5) and (6), respectively:

$$C_s = 1/((2\pi SRF)^2 L_s) \quad (5)$$

$$\beta = 1 - (SRF/f)^2 \quad (6)$$

The RF-choke's SRF has been plotted in Fig. 2 by using (4). For various spiral inductors turns, referred to by their value in nano-Henry (nH) in TABLE I, both C_s and β are calculated through (5) and (6), respectively. Then, on the basis that F_{lower} is 5 GHz, both C_a and C_1 are chosen 2 pF to insure enough AC-shunt while not reserving too much area when implemented. Finally, using (3), the variations of R'_{in}

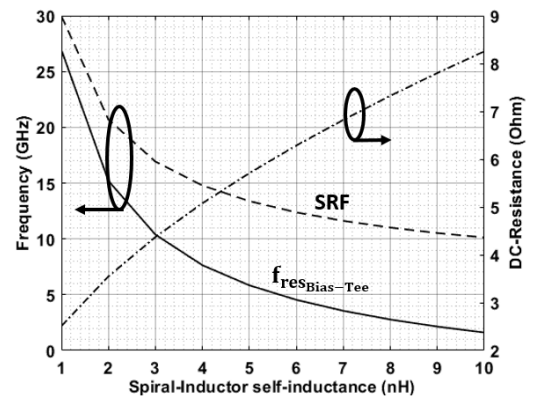


Fig. 2. Bias-tee's overall resonance frequency, and homemade spiral inductor's SRF and DC resistance against different values of self-inductance (L_s). For C_a and C_1 equal to 2 pF, and $R_1 = 50 \Omega$.

TABLE I
ELECTRICAL PARAMETERS OF IMPLEMENTED BIAS-TEE

Spiral	C_a (pF)	R_1 (Ω)	C_s (fF)	$f_{res}^{Bias-Tee}$ (GHz)	C_1 (pF)
3-nH	2	50	29.5	10.3	2
4-nH	2	50	29	7.6	2
5-nH	2	50	28.3	5.7	2
6-nH	2	50	27.6	4.5	2

and X'_{in} against frequency can be calculated. Thus, the overall resonance frequency of the bias-tee, corresponding to $X'_{in} = 0 \Omega$, can be easily determined. It is plotted on Fig. 2 and provided as an empirical expression with SRF in (7).

$$f_{res}^{Bias-Tee} = 1.273 * SRF - 11.25 * 10^9 \quad (7)$$

Fig. 3(a) shows the input reactance of the bias-tee as negative reactance changing against frequency for various spiral coils values, proving an equivalent linear capacitive behavior above the resonant frequency. In order to obtain wideband low input reactance up to the intended F_{upper} , for better port matching purposes, and since the negative part of the reactance is quite small, it can be compensated at higher frequencies by simply adding a low-value inductor, L_e . By doing so, one arrives at the complete bias-tee of Fig. 1, providing an input impedance Z_{in} . Both Z_{in} and L_e are described by (8).

$$Z_{in} = Z'_{in} + j\omega L_e \approx R'_{in} \quad (8)$$

For the practical implementation example considered, referring to Fig. 2 and considering $F_{lower} = 5$ GHz, any inductance above about 5.6 nH would place the resonance of the bias-tee below F_{lower} . However, the higher the inductance, the higher the DC resistance of the inductor is and thus the higher the DC power overhead due to the voltage drop along it. In this paper, in order to be cautious against process variation, 6-nH is chosen which results in $C_s = 27.6$ fF and a bias-tee resonance frequency below

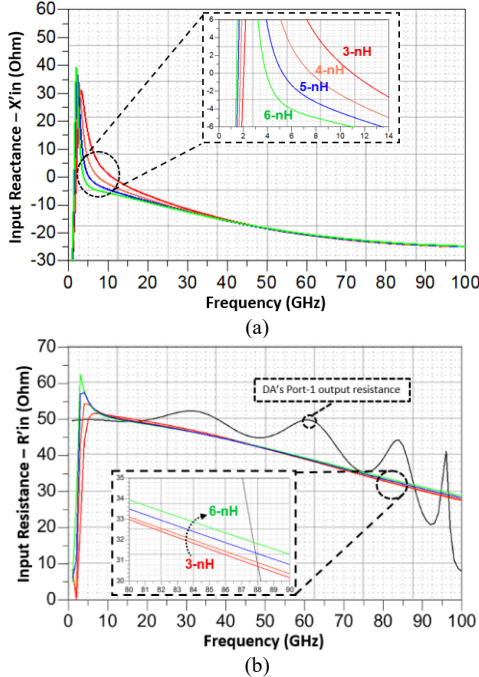


Fig. 3 Bias-tee's (a) equivalent input reactance (X'_{in}) and (b) input resistance (R'_{in}), versus frequency for different sizes of spiral inductors.

5 GHz. Examining Fig. 3 (b), it can be observed that bias-tee input resistance is decreasing against frequency. To anticipate with the distributed amplifier as an applicative circuit, it is interesting to note that the DA's resistance seen at the concerned biasing port is also decreasing in a similar manner. Thus, the proposed bias-tee can also benefit through C_s an adequate matching terminal resistance. Fig. 4 illustrates the bias-tee's choke bandwidth referred to 50Ω . Here, a maximum input reflection coefficient of -10 dB is defined for the bias-tee as a determinant for such a bandwidth. Thereby to compensate for the negative input reactance at the intended F_{upper} , inductor L_e is set to 30 pH. This resulted in a bias-tee bandwidth reaching 100 GHz.

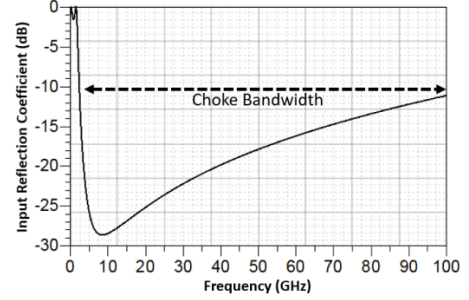


Fig. 4 Bias-tee's input reflection coefficient against frequency with respect to a $50\text{-}\Omega$ input impedance.

III. APPLICATION TO DISTRIBUTED AMPLIFIERS

As a proof-of-concept of the proposed wideband bias-tee, a CMOS DA, with 1-dB bandwidth target close to 100 GHz and F_{lower} of 5 GHz is implemented using the eight-metal version of STMicroelectronics' 55-nm process, as illustrated in Fig. 5, where Fig. 5 (a) presents the DA biasing approach at R_1 termination.

The required DA is designed at a reference impedance of 50Ω . It consists of five unit cells, and each unit cell is made from a cascode Gm-cell of two stacked transistors, N-MOS common-source (CS) and common-gate (CG) FETs. The wideband amplifier is designed at V_{DD} of 1.2 V with total current consumption $I_{DD} = 25$ mA corresponding to a current density of 0.16 mA per CS transistor width (in μm). The CS and CG FETs' widths were set to 31 μm and 62 μm . The unit-cells' inductive segments ($L/2$ on Fig. 5(a)) are

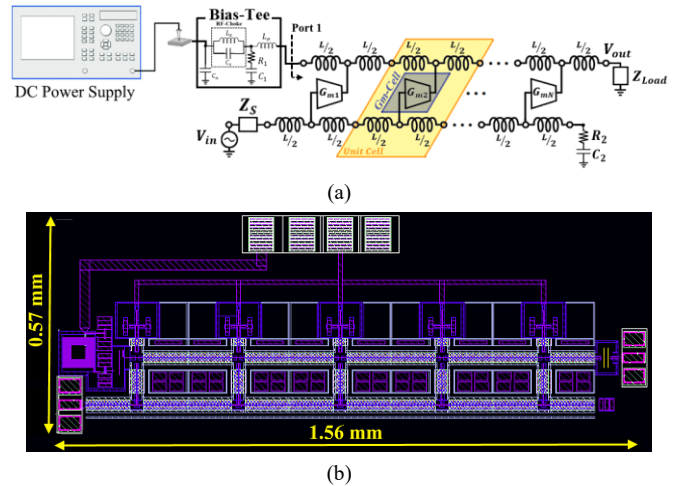


Fig. 5 (a) Distributed amplifier principle with bias-tee connected to the left side of its artificial output line. (b) Chip layout of the five unit-cells distributed amplifier with bias-tee connected to its artificial drain line.

TABLE II
COMPARISON TO OTHER CMOS DISTRIBUTED AMPLIFIERS BIASING APPROACHES

Ref.	Process Techno.	Gain (dB)	BW (GHz)	GBP (GHz)	Supply (V)	P_{DC} (mW)	GBP/P_{DC} (GHz/mW)	Surface Area (mm ²)
[4]	90-nm SOI CMOS	9.7	49	149.7	2**	132	1.1	0.3
[5]	120-nm SOI CMOS	7.8	82	201.3	2.6**	130	1.55	1
[11]	180-nm CMOS	6	27	53.9	3.3**	68.1	0.8	1.62
[9]	180-nm CMOS	25 [‡]	34	604.6	2.8*	176	3.4	0.86
[7]	100-nm HEMT	10	90	284.6	N/A	860 [#]	0.3	2
This Work	55-nm CMOS	6	92	183.7	1.4*	35	5.2	0.89

N/A = not available.

[‡]Cascaded distributed amplifier

*Through integrated on-chip RF-choke. **Through external bias-tee. [#]Through integrated on-chip resistor.

implemented using the process design kit (PDK) microstrip TL (μ -TL) with a width of 1 μ m and length of 135 μ m. The 50- Ω resistor R_1 is implemented using silicide N+ polysilicon type resistors, similarly for R_2 . C_a is designed at 2 pF by using parallel plate capacitor available from design kit. Capacitor C_1 , also set to 2 pF, uses the same component, similarly for C_2 . The 6-nH homemade microstrip spiral inductor, previously described, covers a surface area of 82 μ m x 82 μ m. Referring to Fig. 2, the price of such an inductance is a DC resistance of about 6.3 Ω . The 30-pH inductor L_e is implemented using PDK μ -TL of 1- μ m/50- μ m in width/length. For the gate line, biasing is provided through RF input pad (to be connected to the bias-tee internal to a vector network analyzer).

Fig. 6 shows the post-layout simulated S-parameters versus frequency. 6-dB amplification with P_{DC} of 35 mW is observed from 3 GHz up to 97 GHz with the same input matching bandwidth (BW). The output matching BW is slightly restricted from 5 GHz up to 97 GHz leading to a DA BW of 92 GHz. To compensate for the DC-resistance resulting from bias-tee's spiral inductor, the supply voltage V_{DD} must be increased from 1.2 V to 1.4 V while maintaining same current consumption of 25 mA, i.e. 17% of DC power overhead. The resulting GBP is 184 GHz. Table II summarizes the comparison between the designed DA with proposed on-chip bias-tee connected to the left side of its drain line and the reported DAs in the literature with their respective biasing approaches. Compared with other DAs, the proposed one exhibits the lowest voltage supply (V_{DD}) through bias-tee, and hence it contributed to a lower DA's P_{DC} , while also being applied for wideband amplification. This led us to attaining a DA with a highest gain-bandwidth product (GBP) over P_{DC} of 5.2 GHz/mW. Even with a 6-nH spiral inductor, the designed bias-tee resulted in a compact profile that could be accommodated inside the DA layout, as illustrated in Fig. 5(b), and hence the total surface area remained unchanged, as shown in Table II.

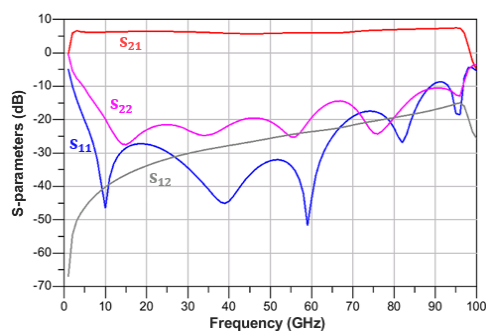


Fig. 6 DA's post-layout simulated S-parameters versus frequency (the proposed bias-tee is included).

IV. CONCLUSION

A wideband millimeter-wave bias-tee was proposed, taking advantage of the parasitic capacitance of the RF-choke. Through proper choice of proposed bias-tee's design parameters, its overall resonance can be established at a frequency below the lower corner of the biased circuit's passband. The bias-tee design methodology has been described and applied for biasing a broadband CMOS DA in a 55-nm process. The bias-tee provided wide input matching bandwidth, reaching frequencies up to 100 GHz. It is compact and avoids the use of off-chip bulky bias-tees, while causing low voltage drop. The proposed way of implementing the bias-tee could open the door for future on-chip bias-tees for integrated measurement tools at probe-level, for example.

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