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# Low temperature behavior of FD-SOI MOSFETs from micro- to nano-meter channel lengths

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**Abstract**—In this paper we present an analytical experimental study regarding the extraction and analysis of 28 nm FD-SOI MOSFET parameters, from room temperature down to 25 K, and from micro- to nanometer gate lengths. It is shown that the FD-SOI device behavior with temperature can reliably be described by the already established theory of physics for deep cryogenic conditions: Boltzmann statistics and phonon scattering mechanisms are the two main factors that define the device electrical behavior. Moreover, we also demonstrate the advantage of the Y-function as a parameter extraction method, across different channel lengths, and a wide temperature range. We demonstrate the dependence of threshold voltage, subthreshold swing, low-field mobility and source-drain series resistance on temperature, and how this may be affected by the gate length decrease.

**Keywords** — MOSFET, Y function, nanoelectronics, cryogenic, FD-SOI

## I. INTRODUCTION (HEADING 1)

As the potential of quantum computing and the interest in related research are growing, so does the demand for a deep understanding of the behavior of modern electronic devices at low temperatures. Furthermore, the study of CMOS technologies at cryogenic temperatures has to be regarded not only in focus of readout electronics for quantum technologies (around few degrees above 0 K), but also for what concerns space applications of electronics and cryobiology [1-2]. It has been well established in earlier research works that, as predicted by theory [3], low temperatures can in fact enhance a MOSFET's performance, through the decrease of the subthreshold swing and the increase of the carrier mobility.

The recent literature is rich in experimental studies of advanced microelectronic devices such as FinFETs [4] and Fully Depleted SOI MOSFETs [5, 6] operating at very low temperatures. Nevertheless, to the best of our knowledge, there has been no systematic study of the FDSOI parameter evolution with temperature, as a function of the gate length. In this work, a thorough experimental study is presented, regarding the low temperature behavior of device electrical parameters (i.e. threshold voltage,  $V_t$ , low-field mobility,  $\mu_0$  and subthreshold swing, SW) in Si channel Fully Depleted

Silicon-On-Insulator (FD-SOI) MOSFETs, with a special focus on short channel effects and scattering mechanisms.

## II. EXPERIMENTAL DETAILS

### A. Devices under study and experimental setup (Heading 2)

The present work reports the results of measurements on HKMG 28nm FDSOI MOSFET technology (7 nm silicon film thickness, 1.7nm EOT gate oxide and 30nm BOX). More fabrication details can be found in [7]. The devices under study share the same channel width, of  $W = 1 \mu\text{m}$ , with channel length spanning from  $L = 30 \text{ nm}$  to  $L = 1 \mu\text{m}$  [7]. I-V characterization was performed in a SUSS MicroTec cryostation with tungsten probes connected to a HP 4155 analyzer. The measurements were performed at temperatures ranging from 25K to 300 K, using liquid nitrogen. The electrical parameters were extracted using the Y-function method [8], in order to suppress any influence of series resistance.

### B. Low Temperature effects at first glance

When going to deep cryogenic temperature, there are two main effects affecting the performance and behaviour of MOSFET transistors: the free carrier concentration is dictated by Boltzmann statistics and the carrier mobility is limited by electron-phonon scattering.

- According to Boltzmann statistics, when shifting the operation to lower temperatures, there are fewer and fewer electrons promoted in the conduction band: this results in a consequent increase of the threshold voltage and a decrease of the subthreshold slope (as  $T$  decreases).
- As the temperature is reduced, so is the vibrational energy in the semiconductor lattice: this causes a reduction of the related phonon scattering, allowing an increase in the low-field mobility inside the channel material.

A good measure of these two effects can be drawn from Fig. 1, showing the input characteristics of a  $L = 1000 \text{ nm}$  channel length device across different operation temperatures. Going down to 25K results in a threshold voltage increase,

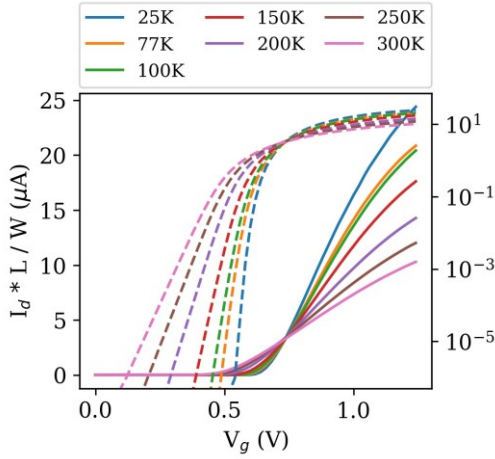


Fig. 1. Normalized drain current with respect to length to width ratio versus gate voltage ( $L = W = 1 \mu\text{m}$ ).

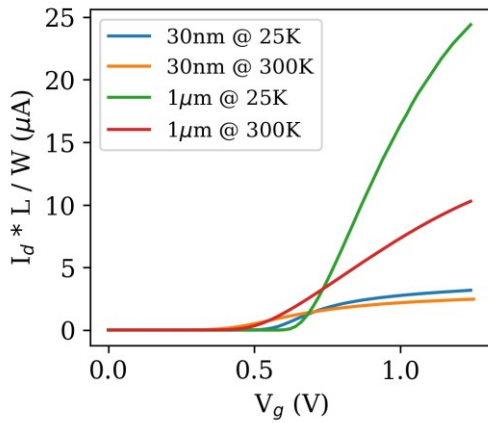


Fig. 2. Normalized drain current versus gate voltage comparison for  $L = 30 \text{ nm}$  and  $L = 1000 \text{ nm}$  at  $T = 25$  and  $300 \text{ K}$ .

while simultaneously the drain current in strong inversion is enhanced thanks to the mobility increase. These two competing mechanisms are cancelling each other out at around  $V_g = 0.75 \text{ V}$ , where the curves are crossing.

It is also important to probe the effect of a decreasing channel length on the  $I_d$ - $V_g$  curves of a MOSFET transistor. As we can appreciate in Fig.2, at both  $300 \text{ K}$  and  $25 \text{ K}$ , a decrease of the channel length (in the figure, from  $1000 \text{ nm}$  to  $30 \text{ nm}$ ) causes a deformation in the linearity of the drain current in strong inversion: consistently across the measured temperature range, the drain current  $I_d$  has an increased downwards bending at high  $V_g$  for shorter channel length.

### C. Parameter Extraction Method: the Y-function approach

In order to extract the critical parameters from the input characteristics of the measured devices, we referred to the work [9] and the proposed Y-function: starting from the formula of the drain current with the first and second order mobility attenuation factors (1), we combined it with the transconductance ( $g_m = dI_d/dV_g$ ) so as to obtain the Y-function (2).

$$I_d = \frac{G_m V_d (V_g - V_{th})}{1 + \theta_1 (V_g - V_{th}) + \theta_2 (V_g - V_{th})^2}, \quad G_m = \frac{W}{L} C_{ox} \mu_0 \quad (1)$$

$$Y = \frac{I_d}{\sqrt{g_m}} = \frac{\sqrt{G_m V_d} (V_g - V_{th})}{\sqrt{1 - \theta_2 (V_g - V_{th})^2}} \quad (2)$$

According to its formulation, the Y-function is free from any first order (scattering and access resistance-related) attenuation. To rectify the effect of the second order attenuation factor on Y, and grant it linearity even in strong inversion (high  $V_g$ ), the function was corrected as according to (3) [9].

$$Y' = Y \sqrt{1 - \theta_2 (V_g - V_{th})} \quad (3)$$

Furthermore, looking at Figs. 3 and 4, the improved Y-function method shows a reasonably good linearity in strong inversion region at both small channel lengths and low operation temperatures. Therefore, this method allowed us to perform a reliable parameter extraction under all temperature conditions.

### III. RESULTS AND DISCUSSION

By applying the improved Y-function method, we extracted the main parameters concerning the MOSFET operation down to deep cryogenic temperatures, that can be attributed to the aforementioned two main effects.

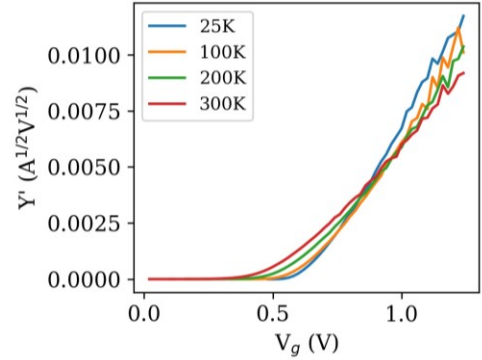


Fig. 3. Corrected Y function vs gate voltage for a  $L = 120 \text{ nm}$  channel device and various temperatures.

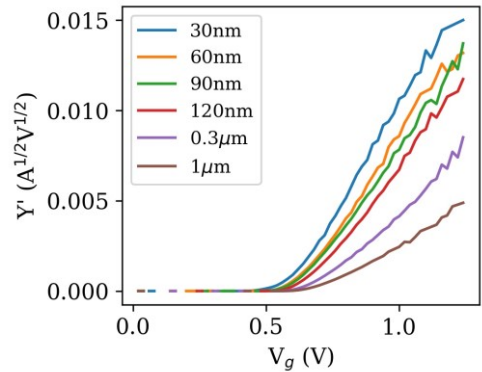


Fig. 4. Corrected Y function vs gate voltage for all measured devices at  $T = 25 \text{ K}$ .

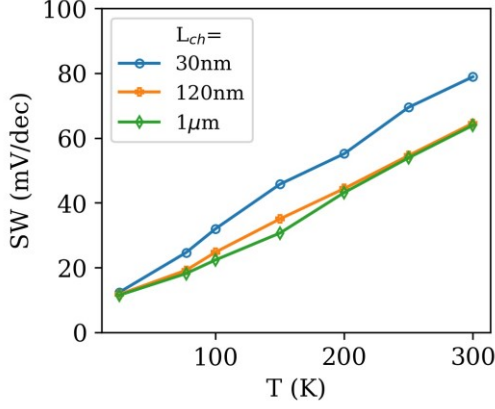


Fig. 5 Extracted values of Subthreshold Swing vs temperature for different device channel lengths.

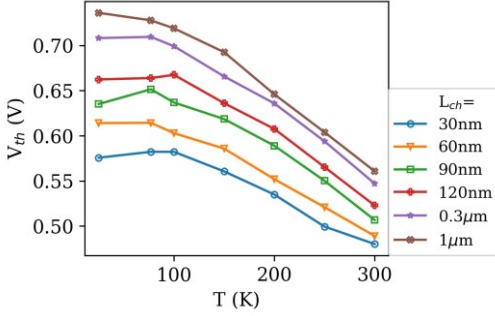


Fig. 6 Extracted values of threshold voltage vs temperature for all measured devices.

#### A. Switching parameters and short channel effects

As the temperature decreases, the subthreshold swing decreases linearly for all gate lengths, up to a plateau of around 10 mV/dec [10, 11], as shown in Fig. 5. On the other hand, the threshold voltage increases with a decreasing temperature, down to about 100K, where the nondegenerate Boltzmann statistics transition to degenerate, making the threshold voltage reach a plateau as seen in Fig. 6. [2]

Moreover, as one can observe in Fig. 7, the roll-off of the threshold voltage with respect to a decreasing channel length is almost not at all affected by the changing temperature. We can attribute this to the fact that the electrostatic control of the channel by the gate is not affected by the operating temperature, making this specific short channel effect (SCE) uninfluenced by the varying temperature.

#### B. Mobility and Phonon Scattering

A decreasing temperature causes a decrease in phonon scattering, yielding, as expected, an increase of the carrier mobility. Nevertheless, Fig. 8 shows that the low-field mobility has a significantly different temperature dependence trend for each channel length. This effect is easily imputable to the difference in predominant scattering mechanism between long and short channel devices: in fact, phonon scattering is the predominant mechanism only in long channel devices; on the other hand, short channel devices are sensitive to neutral impurity scattering [12] close to source and drain, resulting in a

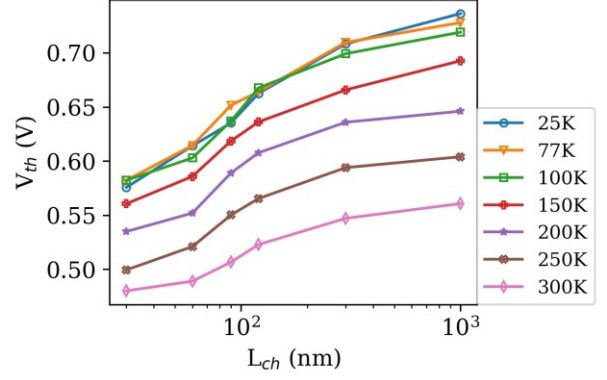


Fig. 7. Extracted values of threshold voltage vs channel length.

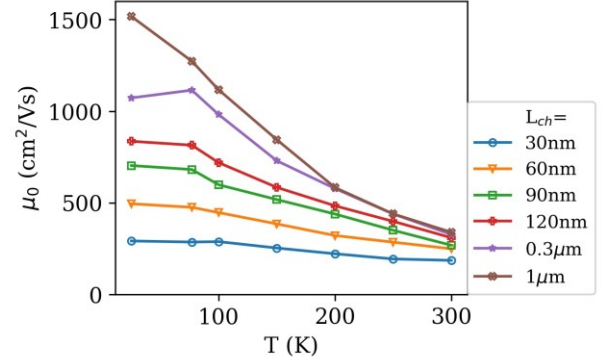


Fig. 8. Extracted values of low-field mobility vs temperature.

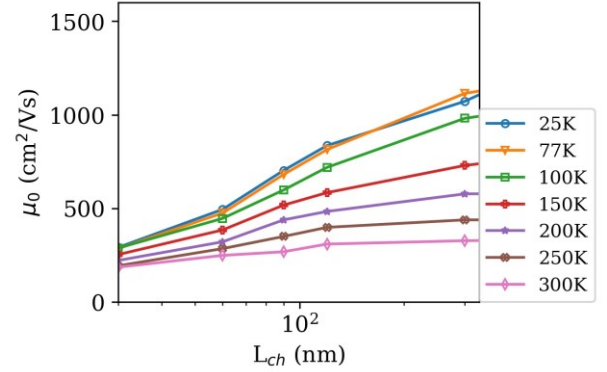


Fig. 9. Extracted values of low-field mobility vs channel length.

much less temperature dependent mobility for  $L = 30$  nm. This reveals a drawback, since it means that short channel FD-SOI MOSFETs cannot have the same performance boost at low temperatures as their longer counterparts (Fig. 9).

#### C. Source-drain series resistance

It is lastly worth to mention how from the attenuation of the drain current in the strong inversion region, we can extract a general formula [8] of the attenuation coefficient (4) and, particularly, its first order factor,  $\theta_1$  (Fig. 10).

$$\theta_1 + \theta_2(V_g - V_{th}) = \frac{G_m}{I_d} - \frac{1}{V_g - V_{th}} \quad (4)$$

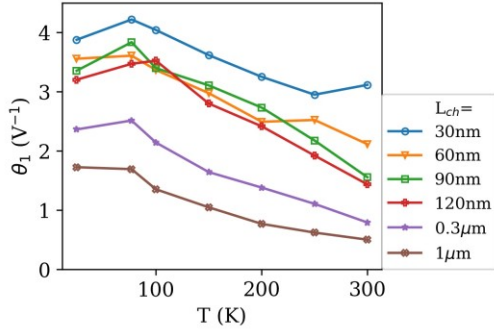


Fig.10. Extracted values of first-order mobility attenuation factor vs temperature.

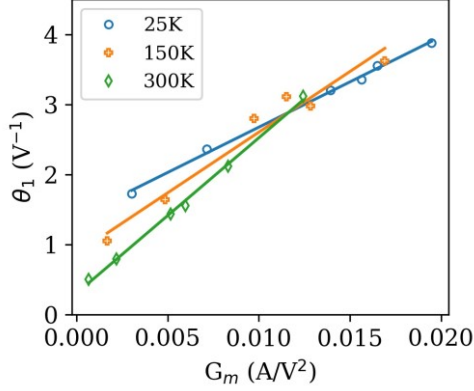


Fig. 11. Extracted values of low-field mobility vs Gm factor (1).

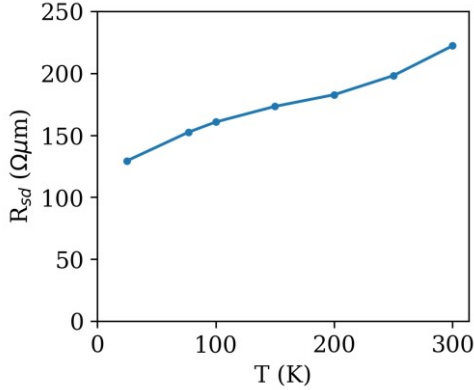


Fig. 12. Extracted values of Source-to-Drain resistance vs temperature.

Also, if we take a look at the formulation of the first order attenuation factor (5), we see how it is linearly dependent on the source-drain series resistance,  $R_{sd}$ , through the factor  $G_m$  and we can therefore plot it as its function.

$$\theta_1 = \theta_{1,0} + G_m R_{sd} \quad (5)$$

In Fig. 11, we can see how for different temperatures the dependence of  $\theta_1$  on  $G_m$  has different linear slopes: this allows extracting the values of  $R_{sd}$  for different temperatures. The source-drain series resistance shows (Fig. 12) a metallic behaviour, with a linear decrease with decreasing temperature, down to a remaining value, corresponding to other material properties.

## IV. CONCLUSION

To summarize, we have carried out a thorough study of planar FD-SOI MOSFET devices, with channel length spanning from 1 micron down to 30 nm, and for a temperature ranging from 25 K up to room temperature.

The measurements and data analysis have shown that modern devices comply with theoretical predictions and reveal generally improved operation properties at deep cryogenic temperatures: threshold voltage and mobility increase, while subthreshold swing and source-to-drain resistance decrease. However, we also demonstrated that, although the performance is improved at low temperature for such kind of devices, the margin of this improvement is sensibly smaller for short channel devices compared to long channel devices.

## ACKNOWLEDGMENT

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