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Lambert-W Function-based Parameter Extraction for FDSOI MOSFETs Down to Deep Cryogenic Temperatures

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Abstract

The applicability of the Lambert-W function-based parameter extraction methodology is demonstrated for 28nm FDSOI MOSFETs down to deep cryogenic temperatures (4.2K). The Lambert-W function enables to accurately model the inversion charge and drain current MOSFET characteristics from weak to strong inversion, while using the classical mobility law down to liquid helium temperature. The main MOSFET parameters were extracted versus temperature and gate length, showing the temperature independence of short channel effects and the strong mobility degradation at short channel length due to increased neutral defect scattering.

Keywords: MOSFET, FDSOI, parameter extraction, Lambert-W function, cryogenic temperature.

1. Introduction

The MOSFET electrical parameters extraction is a key topic for CMOS technology characterization and optimization. With the advent of quantum computing, requiring CMOS readout electronics at cryogenic temperatures, there is a strong need for updating MOSFET parameter extraction methodologies in advanced technologies down to very low temperatures, 4.2K and below [1-5]. In the past years, such methodologies were developed in strong inversion region using conventional threshold voltage and mobility extraction procedures [6,7] or specific Y-function based extraction techniques [8,9]. In recent years, MOSFET parameters were also extracted at cryogenic temperatures using compact models like, e.g., EKV in FDSOI MOS devices [10] or BSIM in bulk MOS transistors [11]. In addition, a full gate voltage range Lambert-W function-based methodology was recently developed allowing electrical parameters extraction in FDSOI MOSFETs at room temperature [12]. It should also be mentioned that the Lambert-W function has been used for the MOSFET modelling as it is the rigorous solution of undoped body MOS transistors [13] and an approximate solution for a doped MOS device [14].

In this paper, we propose, for the first time, to apply the Lambert-W (LW) function for the inversion charge and drain current modelling as a function of gate voltage and, by turn, for MOSFET parameter extraction down to deep cryogenic temperatures. To this end, we first show the validity of the Lambert-W function for the description of the gate-to-channel capacitance and inversion charge with gate voltage from weak to strong inversion in large area 28nm FDSOI MOSFETs down to liquid helium temperatures. Then, we demonstrate the applicability of the Lambert-W function-based method to fit the drain current down to very low temperatures using a classical mobility law, providing the dependence of subthreshold slope ideality factor, threshold voltage and mobility parameters with gate length and temperature.

2. Experiments and methods

The measurements were performed on 28nm FDSOI MOSFETs with silicon film thickness $t_{\text{si}}=7\text{nm}$ and buried oxide (BOX) thickness $t_{\text{box}}=25\text{nm}$ from STMicroelectronics. NMOS transistors were processed from (100) handle substrate, with $\langle 100 \rangle$ -oriented channel, and a high-k/metal gate Gate-First architecture [15]. Low- V_{th} transistors were available with un-doped channel through a doped back plane (NWELL doping $N_{\text{A}}=10^{18}\text{cm}^{-3}$) below the BOX. Thin gate oxide (with equivalent oxide thickness $EOT=1.1\text{nm}$) devices with mask gate length L varying from 30nm up to 10 μm and with gate width $W=1\mu\text{m}$ or 10 μm were tested using a cryogenic probe station down to 4.2K. Note that the effective gate length has been checked by split CV technique and found close to the mask length.

The gate-to-channel capacitance $C_{gc}(V_g)$ was measured with an HP 4284 LCR meter at 1MHz frequency and 10mV AC level using the standard split C-V technique. The drain current $I_d(V_g)$ MOSFET transfer characteristics were recorded in linear region ($V_d=30-50mV$) with an HP4156 parameter analyser. All the measurements were made at zero back bias. Influence of body bias can be found elsewhere [16].

The MOSFET parameter extraction was performed on the $C_{gc}(V_g)$ and $I_d(V_g)$ characteristics using the same Lambert-W function based procedure as in [12] for room temperature. The equations and parameters used for the curve modelling are recalled below.

The $C_{gc}(V_g)$ and $Q_i(V_g)$ curves were fitted with Eqs. (1) and (2) with C_{ox} and b as fitting parameters [12]:

$$C_{gc}(V_g, T) = \frac{bQ_i(V_g, T)C_{ox}}{C_{ox} + bQ_i(V_g, T)} \quad (1)$$

$$Q_i(V_g, T) = C_{ox}\eta kT/qLW(e^{\frac{V_g - V_t}{\eta kT/q}}) \quad (2)$$

$$\frac{Q_i}{C_{gc}} = \frac{1}{b} + \frac{Q_i}{C_{ox}} \quad (3)$$

where kT/q is the thermal voltage, C_{ox} is the gate oxide capacitance, η is the subthreshold slope ideality factor, V_t is the threshold voltage and with $b = q/(\eta kT)$.

The effective mobility μ_{eff} and $I_d(V_g)$ curves were modelled using Eqs. (4) and (5) with fitting parameters η , V_t , μ_0 , θ_1 and θ_2 [12]:

$$\mu_{eff}(Q_i) = \frac{\mu_0}{1 + \theta_1(Q_i/C_{ox}) + \theta_2(Q_i/C_{ox})^2} \quad (4)$$

$$I_d(V_g, T) = \frac{W}{L} \mu_{eff}(Q_i(V_g, T)) Q_i(V_g, T) V_d \quad (5)$$

where μ_0 is the low field mobility, $\theta_1 = \theta_{10} + R_{sd}\beta$ and θ_2 are the first order and second order mobility attenuation coefficients, θ_{10} being the intrinsic first order mobility attenuation factor, R_{sd} source/drain access series resistance and $\beta = W.C_{ox}.\mu_0/L$ gain factor.

A conventional Levenberg-Marquardt algorithm was used for the curve fitting optimization.

3. Results and discussion

3.1. Capacitance and inversion charge characteristics

$C_{gc}(V_g)$ characteristics were measured on large area MOSFETs with $W=L=10\mu m$ for better accuracy. The inversion charge was obtained after integration of the $C_{cg}(V_g)$ curves starting from $V_g=0V$ as is usual in split C-V technique. Typical $C_{gc}(V_g)$ and associated $Q_i(V_g)$ characteristics are shown in Fig.1 (a)-(b)-(c) for various temperatures from 300K down to 4.2K. Note the steeper onset of the inversion charge with the temperature lowering. As proposed in [17,18], the plot Q_i/C_{gc} vs Q_i

(Fig. 1(d)) can be used, according to Eq. (3), to extract the gate oxide capacitance from the slope, giving here $C_{ox} \approx 2 \mu\text{F}/\text{cm}^2$, independently of temperature. Indeed, the nice superposition of the $Q_i/C_{gc}(Q_i)$ curves for all the temperatures is revealing the rather temperature independence of the slope and so of C_{ox} .

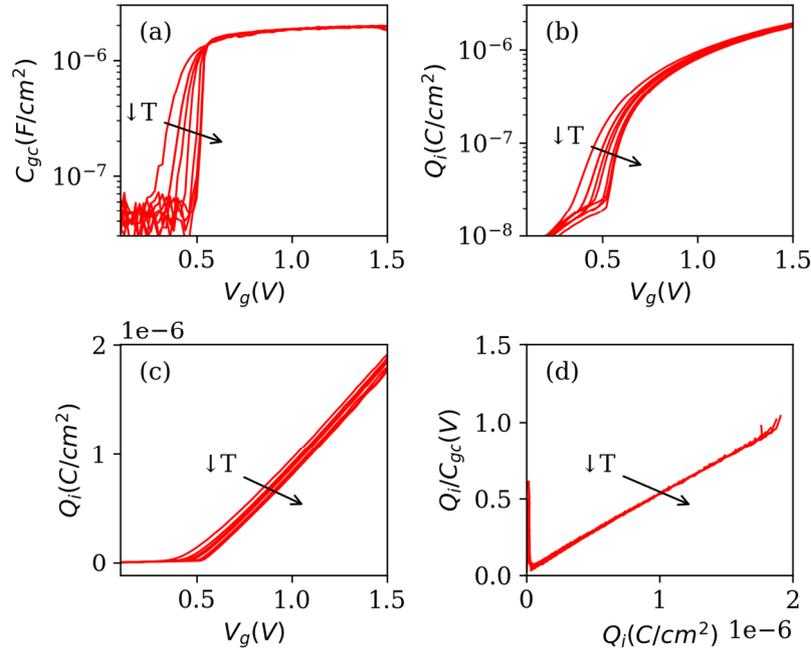


Fig. 1. $C_{gc}(V_g)$ (a), $Q_i(V_g)$ (b) and (c), and $Q_i/C_{gc}(Q_i)$ (d) characteristics for various temperatures $T(\text{K})=4.2, 10, 20, 50, 100, 150, 200, 250$ and 300 ($W=L=10\mu\text{m}$).

Figures 2 (a)-(b)-(c) show the best fits of the $Q_i(V_g)$ and $C_{gc}(V_g)$ characteristics, which can be obtained with the Lambert-W function model of Eqs. (1) and (2) for temperatures varying from 300K down to 4.2K . The extracted fitting parameters for V_t and η are plotted in Fig. 2 (d), indicating a quasi-linear increase of V_t with temperature decrease and a $\approx 1/T$ dependence of η (see below). The excellent agreement achieved between model and experiment emphasizes the validity of the Lambert-W function to adequately describe the capacitance and inversion charge MOSFET characteristics vs gate voltage down to deep cryogenic temperatures. The latter feature fully justifies that the Lambert-W $Q_i(V_g)$ model can further be used for the drain current transfer characteristics modelling and, by turn, MOSFET parameter extraction.

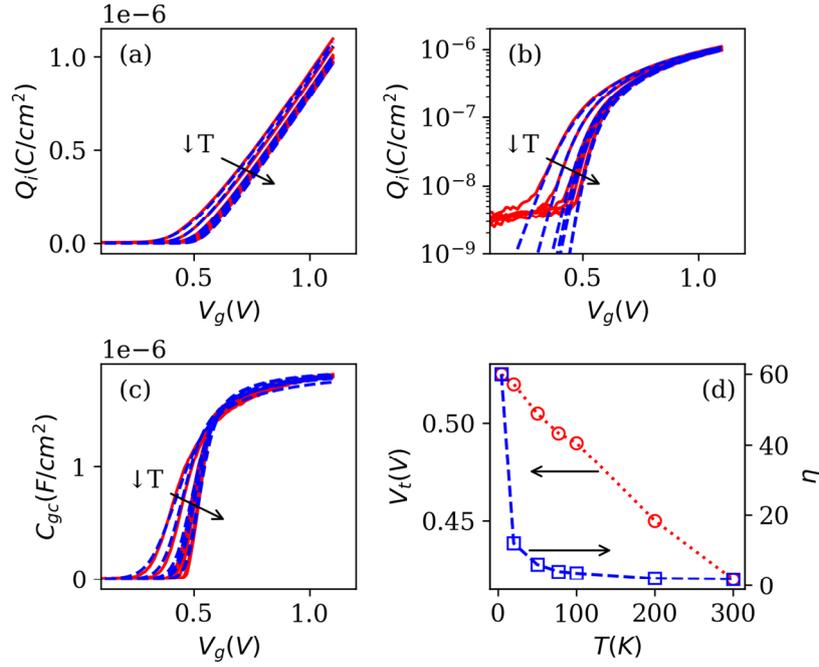


Fig. 2. Experimental (red solid lines) and Lambert-W model fitted (blue dashed lines) $Q_i(V_g)$ (a) and (b), $C_{gc}(V_g)$ (c) characteristics for various temperatures T (K)=4.2, 20, 50, 77, 100, 200 and 300 ($W=L=10\mu\text{m}$). (d) V_t and η parameter variations with temperature T .

3.2. Drain current transfer characteristics of long channel devices

Drain current $I_d(V_g)$ transfer characteristics were first measured in linear region ($V_d=50\text{mV}$) on long channel FDSOI MOSFETs with $W=L=10\mu\text{m}$ to obtain the intrinsic parameters free from source/drain access resistance effect. Typical drain current $I_d(V_g)$, transconductance $g_m(V_g)$ and Y-function $Y(V_g) = I_d/\sqrt{g_m}$ characteristics are shown in Fig. 3 (red solid lines) for various temperatures from 300K down to 4.2K. It should be said that the Y-function $Y(V_g)$ is used to eliminate the source-drain series resistance impact [19, 20]. Similarly, one can notice again the strong increase of the subthreshold slope with the temperature decrease, as well as the significant increase of drain current at high gate voltage, maximum transconductance and average Y-function slope with temperature lowering. The three latter features are related to the improvement of the carrier mobility as the temperature is reduced, as will be shown below. Moreover, a zero temperature coefficient (ZTC) bias point [21] is also noticeable on all characteristics above threshold, around $V_g=0.6\text{V}$.

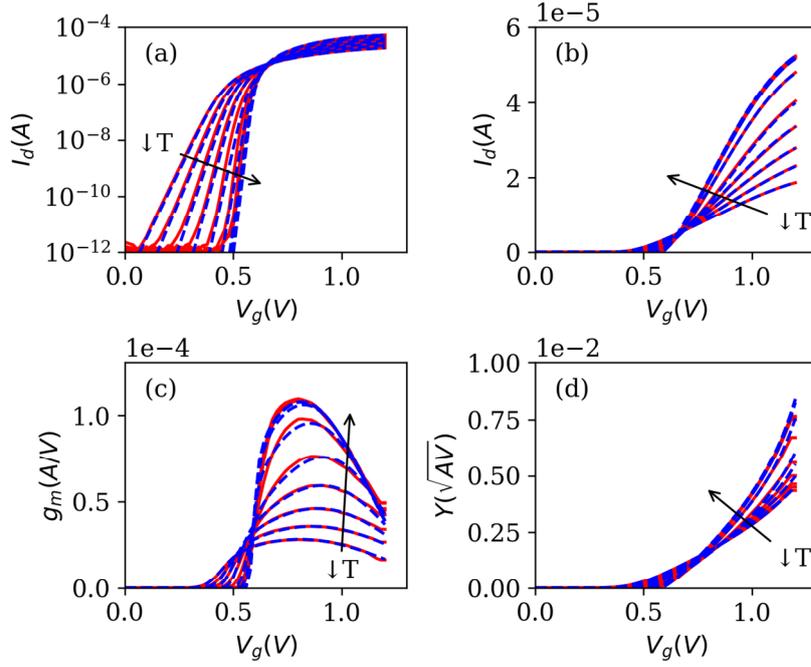


Fig. 3. Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) $I_d(V_g)$ (a) and (b), $g_m(V_g)$ (c) and $Y(V_g)$ (d) characteristics for various temperatures $T(K)=4.2, 10, 20, 50, 100, 150, 200, 250$ and 300 ($V_d=50\text{mV}$, $W=L=10\mu\text{m}$).

Figure 3 also displays the best fits of the $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ characteristics (blue dashed lines), which can be reached with the Lambert-W function model of Eqs. (2), (4) and (5) for temperatures ranging from 300K down to 4.2K . The very good agreement between model and experiment underlines the usefulness of the Lambert-W function to effectively describe the drain current, the transconductance and the Y-function as a function of gate voltage from weak to strong inversion, using a classical mobility law given by Eq. (4) down to very low temperatures.

The extracted fitting parameters V_t , η , μ_0 , θ_1 and θ_2 obtained from Fig. 3 are plotted in Fig. 4 as a function of temperature. As in the C-V extraction, the threshold voltage V_t is increasing quasi linearly with the temperature reduction before saturating, whereas the ideality factor η nearly varies as $1/T$. The low field mobility μ_0 increases with temperature lowering, as is usual, due to phonon scattering reduction [7, chap. 1], before saturating. Both V_t and μ_0 flattening at very low temperature likely stems from inversion layer degeneracy [7, chap. 1&2]. The first-order mobility attenuation coefficient θ_1 lies around $\approx -1\text{V}^{-1}$ ($\pm 15\%$) over the temperature range, while the second-order attenuation coefficient θ_2 increases from 0.8V^{-2} to 1.6V^{-2} as the temperature is reduced. The latter θ_2 feature is related to the higher influence of surface roughness scattering at lower temperatures as the carriers get closer to the oxide/channel interface [7, chap. 1&2].

It is also worth noticing in Fig. 4 that the Lambert-W function extracted parameters V_t , η and μ_0 are close to those obtained by the Y-function method [19, 20], emphasizing once more the consistency of the Lambert-W function methodology.

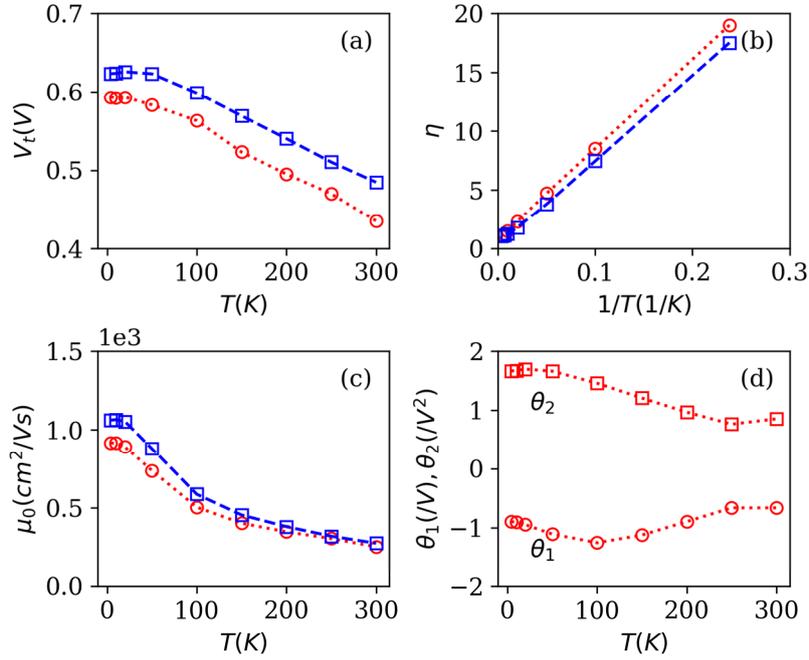


Fig. 4. V_t (a), η (b), μ_0 (c) parameter variations as extracted from Lambert-W function fits (red dotted lines) and from Y-function method (blue dashed lines), and θ_1 with θ_2 (d) versus temperature ($V_d=50\text{mV}$, $W=L=10\mu\text{m}$).

The effective mobility μ_{eff} obtained from the Lambert-W function fits and defined in Eq. (4) has been plotted in Fig. 5 (a) (red solid lines) and compared to the effective mobility determined by standard split C-V method based on $Q_i(V_g)$ data of Fig. 1 and drain current curves of Fig. 3 (blue dashed lines). As can be seen, both μ_{eff} values merge well at moderate and strong inversion, while strongly differing just above and below threshold. The latter point can be explained, on one hand, by the finite μ_{eff} value ($=\mu_0$) inherent to the classical mobility law used in Eq. (4) reached below threshold, and, on the other hand, by the erroneous μ_{eff} zero value returned by the split C-V method close to and below threshold [22,23]. Nevertheless, it should be noted that the maximum μ_{eff} values, μ_{max} , obtained by both methods and plotted in Fig. 5 (b) are very close to each other, which proves again the physical consistency of the mobility extracted by the Lambert-W function fits. It is worth noting that the negative values for θ_1 obtained by the Lambert-W extraction allow modelling the increase of μ_{eff} above threshold. This is necessary for mimicking the low temperature mobility law where Coulomb scattering induces such a mobility increase at very low temperatures [9,24].

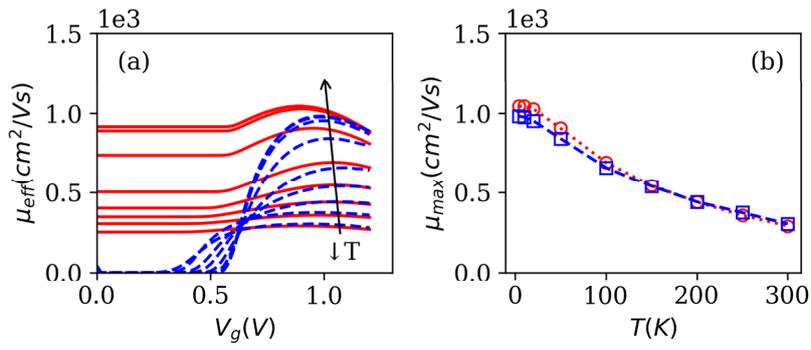


Fig. 5. (a) μ_{eff} variations with V_g and (b) maximum μ_{eff} variations with temperature as obtained from Lambert-W function fits (red lines) and split C-V technique (blue dashed lines). ($V_d=50\text{mV}$, $W=L=10\mu\text{m}$).

3.3. Drain current transfer characteristics of short channel devices

Drain current $I_d(V_g)$ transfer characteristics were then measured in linear region ($V_d=30\text{mV}$) on short channel FDSOI MOSFETs with gate length varying from 30nm up to $1\mu\text{m}$ and gate width $W=1\mu\text{m}$. Typical drain current $I_d(V_g)$, transconductance $g_m(V_g)$ and Y-function $Y(V_g)$ characteristics are presented in Figs 6 and 7 (red solid lines) for these various gate lengths and for $T=300\text{K}$ and $T=25\text{K}$, respectively. Note the excellent vertical scaling of the characteristics with the gate length reduction for both temperatures.

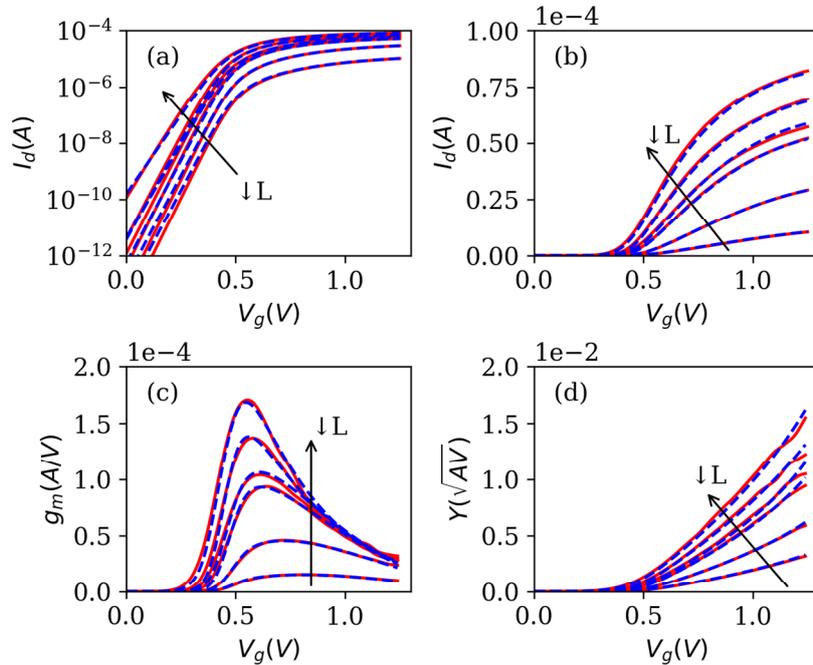


Fig. 6. Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) $I_d V_g$ (a) and (b), $g_m(V_g)$ (c) and $Y(V_g)$ (d) characteristics for various gate lengths $L(\text{nm})=30, 60, 90, 120, 300$ and 1000 measured at $T=300\text{K}$ ($V_d=30\text{mV}$, $W=1\mu\text{m}$).

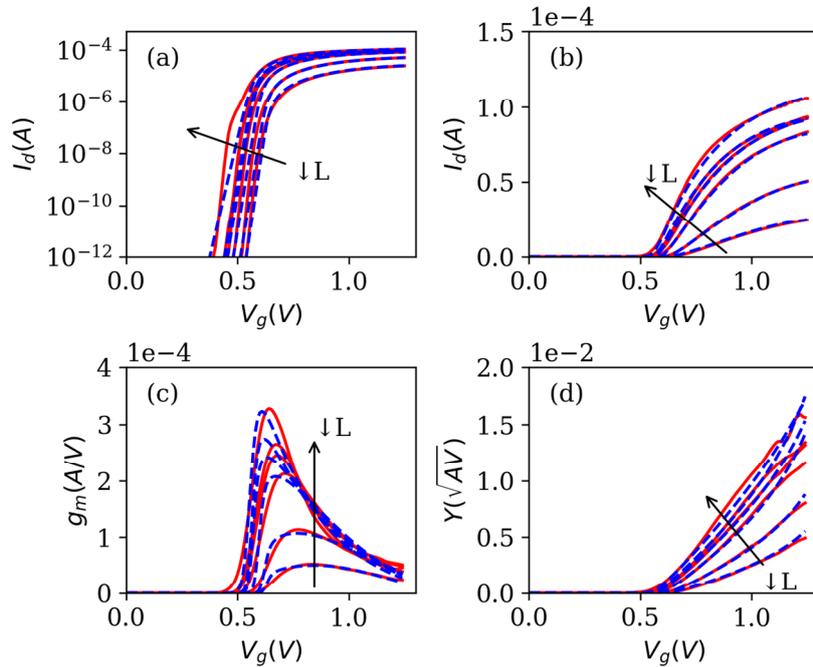


Fig. 7. Experimental (red solid lines) and Lambert-W model fit (blue dashed lines) $I_d V_g$ (a) and (b), $g_m(V_g)$ (c) and $Y(V_g)$ (d) characteristics for various gate lengths $L(\text{nm})=30, 60, 90, 120, 300$ and 1000 measured at $T=25\text{K}$ ($V_d=30\text{mV}$, $W=1\mu\text{m}$).

Figures 6 and 7 also illustrate the best fits of the $I_d(V_g)$, $g_m(V_g)$ and $Y(V_g)$ characteristics (blue dashed lines), which can be obtained with the Lambert-W function model of Eqs. (2), (4) and (5) for the corresponding experimental data. The overall good agreement between model and experiment infers again the effectiveness of the Lambert-W function to properly describe the transfer characteristics, even in short channel MOS devices, as a function of gate voltage from weak to strong inversion using a classical mobility law down to very low temperatures.

The extracted fitting parameters V_t , μ_0 , θ_1 and θ_2 obtained from Figs 6 and 7 are plotted in Fig. 8 versus gate length and for various temperatures from 25K to 300K. As can be seen, the threshold voltage V_t is exhibiting a small roll-off vs gate length due to short channel effects (SCE), whose trend are nearly independent of temperature, as expected, since SCE are mainly controlled by the device electrostatic properties [7, chap. 1]. The low field mobility μ_0 displays a degradation as the gate length is reduced, more significant for lower temperatures. This mobility collapse has been previously attributed to enhanced defective scattering at small channel length, likely due to neutral point defects

located near source and drain regions [23,25]. The first order mobility attenuation coefficient θ_1 strongly increases, almost independently of temperature, as the channel length is reduced, due to the larger impact of access resistance R_{sd} in θ_1 expression (see Eq. (4), [12]). Instead, the second order attenuation coefficient θ_2 weakly decreases with the gate length reduction, likely due to the decreased influence of vertical field in short devices.

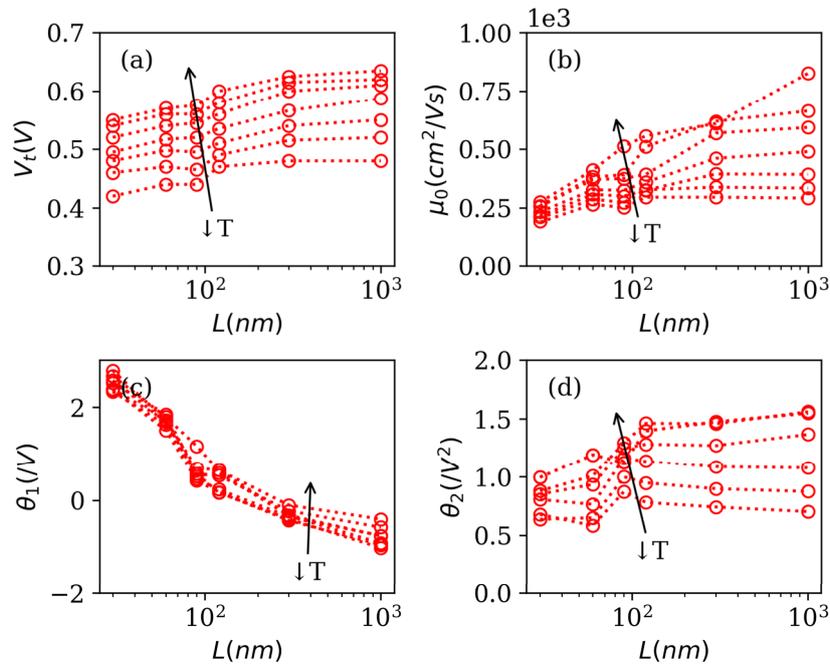


Fig. 8. V_t , μ_0 , θ_1 and θ_2 parameter variations with gate length as extracted from Lambert-W function fits for various temperatures $T(K)= 25, 77, 100, 150, 200, 250$ and 300 ($W=1\mu m$).

The extracted fitting parameters V_t , μ_0 , θ_1 and θ_2 have also been plotted in Fig. 9 versus temperature for various gate lengths in order to better analyse the temperature influence. As can be seen, the threshold voltage V_t varies similarly vs temperature for long and short channel devices, as being governed by the same carrier statistics. In contrast, the low field mobility μ_0 variations with temperature clearly reveal a strong change in scattering mechanism signature, evolving from phonon controlled one in long devices ($\propto T^{-1}$) to neutral defect one ($\propto T^0$) in short channels, as already reported for advanced CMOS technologies [23,25]. The first order mobility attenuation coefficient θ_1 is nearly constant with temperature, whereas the second order attenuation coefficient θ_2 increases with temperature lowering, similarly for all gate lengths, likely due to the higher influence of surface roughness scattering at lower temperatures.

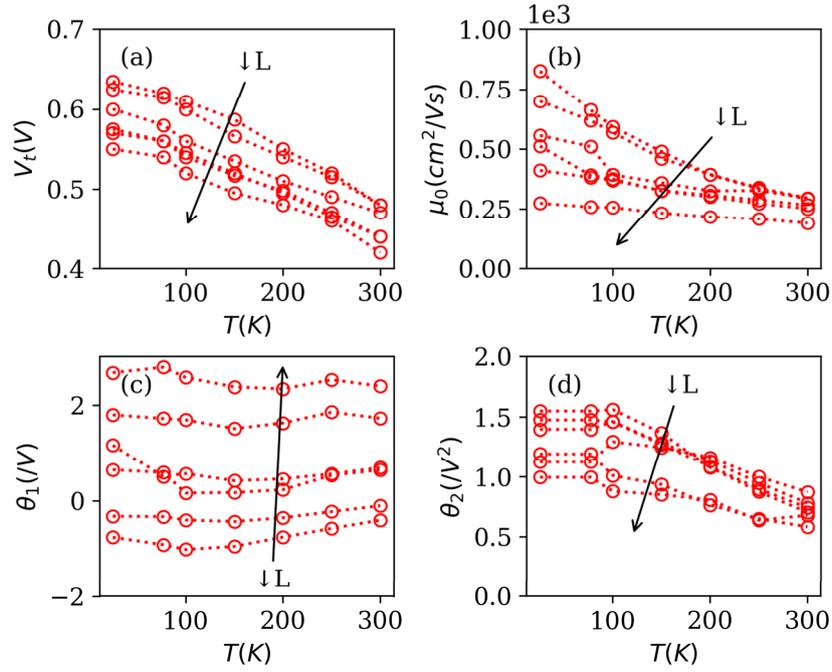


Fig. 9. V_t , μ_0 , θ_1 and θ_2 parameter variations with temperatures as extracted from Lambert-W function fits for various gate lengths $L(\text{nm})=30, 60, 90, 120, 300$ and 1000 ($W=1\mu\text{m}$).

It is also worth mentioning that, following the mobility scattering analysis of Refs [23,25], the low field mobility μ_0 variations with channel length and temperature have been well modeled by Eq. (6), in which the Matthiessen rule is used to combine phonon and neutral scattering mechanisms as,

$$\mu_{0,mod} = \left[\frac{1}{\mu_{ph}} \cdot \frac{T}{300} + \frac{1}{\mu_N} \cdot \left(1 + \frac{L_c}{L} \right) \right]^{-1} \quad (6)$$

where μ_{ph} is the phonon-limited mobility at room temperature, μ_N is the temperature independent neutral defect-limited mobility for long channel, L_c being a critical channel length. As a matter of fact, Fig. 10 (a) and (b) shows the best fits which can be achieved with Eq. (6) on the low field mobility data of Fig. 4(c) and Fig. 9(b) with only 3 parameters (μ_{ph} , μ_N and L_c). In Fig. 10 (c) and (d) are also displayed the variations of the neutral defect scattering rate percentage, % neutral, versus gate length and temperature, clearly revealing its increase with gate length reduction and/or temperature lowering. Therefore, these results confirm once more that the mobility degradation observed at short gate length in this 28nm FDSOI technology can be well interpreted by the enhanced presence of neutral defects as the channel is reduced, as was previously observed in other CMOS technologies [23,25]. Moreover, it should also be mentioned that these low field mobility variations with channel and temperature are in full agreement with those obtained from Y-function extraction on the same technology [26], which emphasizes again the relevance of the Lambert-W function-based parameter extraction methodology for FDSOI MOSFETs.

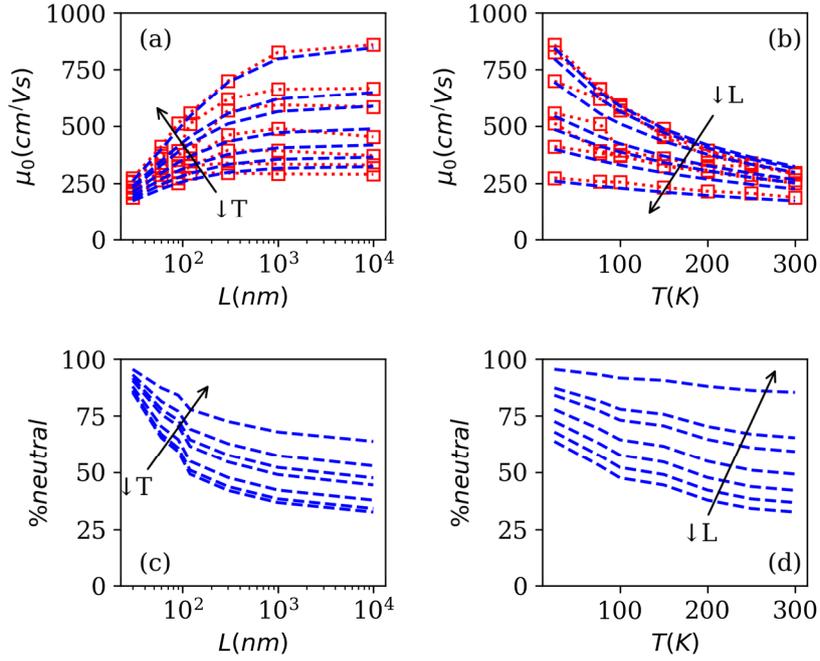


Fig. 10. Experimental (red dotted lines) and modelled (blue dashed lines) variations of low field mobility μ_0 with channel length (a) and temperature (b) as obtained from Eq. (6) with parameters $\mu_{ph}=480\text{cm}^2/\text{Vs}$, $\mu_N=1000\text{cm}^2/\text{Vs}$ and $L_c=80\text{nm}$ (Exp. data from Figs 4c and 9b). Variations of the neutral defect scattering rate percentage % neutral versus gate length (c) and temperature (d) as obtained from mobility modelling with Eq. (6).

Finally, Fig. 11 (a) shows that the increase of the ideality factor η with the temperature reduction is similar for all gate lengths, with larger values for shorter devices due to short channel effect. Actually, this increase of η at lower temperature can be explained by the saturation of the subthreshold swing (SW) for temperatures below 30-40K, since we have $\eta=SW/(kT/q)$ [27,28]. Fig. 11 (b) displays the variations of the first order mobility attenuation coefficient θ_1 with the gain factor parameter $\beta(L)$, parametrized by the channel lengths for various temperatures. As can be seen, θ_1 varies linearly with β as expected due to the increased influence of R_{sd} as the gate length is reduced. As is usual [12,19], the access resistance is extracted from the slope $\theta_1(\beta)$, giving typical values of R_{sd} varying from 230 to 260 $\Omega.\mu\text{m}$ for temperatures increasing from 25K to 300K (Eq. 4).

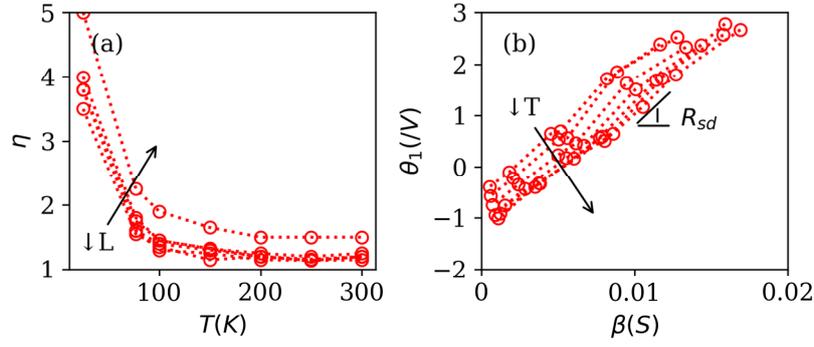


Fig. 11. (a) n parameter variations with temperature for various gate lengths L (nm)=30, 60, 90, 120, 300 and 1000. (b) θ_1 parameter variations with $\beta=W.C_{ox}\cdot\mu_0/L$ gain factor for various temperatures T (K)= 25, 77, 100, 150, 200, 250 and 300 ($W=1\mu\text{m}$).

3. Summary and Conclusion

The applicability of the Lambert-W function-based MOSFET parameter extraction methodology on 28nm FDSOI MOSFETs has been demonstrated down to deep cryogenic temperatures, from long to short channel lengths. Thanks to the accurate Lambert-W function modelling of the inversion charge and drain current MOSFET characteristics from weak to strong inversion, the main parameters were extracted versus temperature and gate length, showing the temperature independence of short channel effects and the strong mobility degradation at short channel lengths due to increased defective scattering. It should also be mentioned that this Lambert-W function modelling of the drain current could easily be extended to nonlinear operation region as in [29], and, therefore, could next constitute a suitable MOSFET compact model to be used in circuit simulation at deep cryogenic conditions.

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References

- [1] J.M. Hornibrook, et al., “Cryogenic control architecture for large-scale quantum computing”, *Phys. Rev. Applied*, 3, 024010-1 (2015).
- [2] R. Maurand, et al., « A CMOS silicon spin qubit », *Nature Commun.*, 7, 13575 (2016).
- [3] E. Charbon et al., “Cryo-CMOS for Quantum Computing,” *IEEE International Electron Devices Meeting (IEDM)*, pp. 343–346, 2016.
- [4] S. J. Pauka et al., “Characterizing Quantum Devices at Scale with Custom Cryo-CMOS,” *Physical Review Applied*, 13, 054072-1, (2020).
- [5] L. Omar Lopez, et al, “A Performance Comparative at Low Temperatures of Two FET Technologies: 65 nm and 14 nm”, *17th Int. Conf. on Electrical Engineering, Computing Science and Automatic Control*, p. 9299192, 2020.
- [6] E. A. Gutiérrez, J. Deen, and C. Claeys, “Low temperature electronics: physics, devices, circuits, and applications”. Academic Press, 2000.
- [7] F. Balestra and G. Ghibaudo, “Device and Circuit Cryogenic Operation for Low Temperature Electronics”. Kluwers, 2001.
- [8] G. Ghibaudo and F. Balestra, “A method for MOSFET parameter extraction at very low temperature”, *Solid-State Electron.*, 32, 221 (1989).
- [9] A. Emrani, F. Balestra, G. Ghibaudo, “Generalized mobility law for drain current modeling in Si MOS transistors from liquid helium to room temperatures”, *IEEE Trans Electron Devices*, 40, 564 (1993).
- [10] A. Beckers, et al, “Characterization and modeling of 28-nm FDSOI CMOS technology down to cryogenic temperatures,” *Solid State Electronics*, 159, 106, (2019).
- [11] Chao Luo, Zhen Lia, Teng-Teng Lua, Jun Xu, Guo-Ping Guoa, “MOSFET characterization and modeling at cryogenic temperatures”, *Cryogenics*, 98, 12 (2019).
- [12] T. A. Karatsori, C. G. Theodorou, E. G. Ioannidis, S. Haendler, E. Josse, C. A. Dimitriadis and G. Ghibaudo, “Full gate voltage range Lambert-function based methodology for FDSOI MOSFET parameter extraction”, *Solid State Electronics*, 111, 123 (2015).
- [13] A. Ortiz-Conde, F. J. García Sánchez y M. Guzmán, "Exact analytical solution of channel surface potential as an explicit function of gate voltage in undoped-body MOSFETs using the lambert w function and a threshold voltage definition therefrom", *Solid-State Electronics*, 47, 2067 (2003).
- [14] A. Ortiz-Conde, F.J. García Sánchez, J. Muci, A. Terán Barrios, J.J. Liou, and C.-S. Ho, "Revisiting MOSFET threshold voltage extraction methods", *Microelectronics Reliability*, 53, 90 (2013).

- [15] N. Planes et al., “28nm FDSOI technology platform for high-speed low-voltage digital applications”, in Symposium on VLSI Technology, Digest of Technical Papers, 33, pp. 133–134 (2012).
- [16] B. Cardoso Paz, et al, “Front and back channels coupling and transport on 28 nm FD-SOI MOSFETs down to liquid-He temperature”, Solid-State Electronics, 186, 108071 (2021).
- [17] B. Mohamad, G. Ghibaudo, C. Leroux, E. Josse, G. Reimbold, “Full Front and Back Split C-V characterization of CMOS devices from 14nm node FDSOI technology”, IEEE S3S Conference, Sonoma, California, USA (Oct 2015).
- [18] G. Ghibaudo, “Electrical characterization of advanced FDSOI CMOS devices”, Nano-electronic Devices ISTE OpenScience, 2, 1-18 (2018).
- [19] G. Ghibaudo, “A new method for the extraction of MOSFET parameters”, Electronics Letters, 24, 543 (1988).
- [20] S. Jain, “Measurement of threshold voltage and channel length of submicron MOSFETs”, IEE Proc. Cir. Dev. Syst., 135, 162 (1988).
- [21] I. M. Filanovsky and A. Allam, “Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits,” IEEE Trans. Circuits Syst. I Fundam. Theory Appl., 48 (7), pp. 876–884 (2001).
- [22] S. Takagi, A. Toriumi, M. Iwase, H. Tango, “On the universality of inversion layer mobility in Si MOSFET's: Part I-effects of substrate impurity concentration”, IEEE Transactions on Electron Devices, 41, 2357 (1994).
- [23] G. Ghibaudo, “Mobility characterization in advanced FD-SOI CMOS devices” in Semiconductor-On-Insulator Materials for Nano-electronics Applications, Springer, Berlin, p. 307, 2010.
- [24] G. Ghibaudo, “Transport in the inversion layer of a MOS transistor. Use of Kubo-Greenwood formalism”, Journal Phys. C: Solid State Physics, 19, 767 (1985).
- [25] M. Shin, M. Shi, M. Mouis, A. Cros, E. Josse, G.-T. Kim and G. Ghibaudo, “Low temperature characterization of mobility in 14nm FD-SOI CMOS devices under interface coupling conditions”, Solid State Electronics, 108, 30 (2015).
- [26] F. Serra Di Santa Maria, C.Theodorou, M. Cassé, F. Balestra and G. Ghibaudo, Low temperature behavior of FD-SOI MOSFETs from micro- to nano-meter channel lengths, Proc. WOLTE 14, Workshop on Low Temperature Electronics, virtual, Italy (April 2021). To be published in IEEE Xplore.

- [27] G. Ghibaudo, M. Aouad, M. Casse, S. Martinie, F. Balestra, “On the modelling of temperature dependence of subthreshold swing in MOSFETs down to cryogenic temperature”, *Solid-State Electronics*, 170, 107820 (2020).
- [28] A. Beckers , F. Jazaeri , and C. Enz, “Theoretical Limit of Low Temperature Subthreshold Swing in Field-Effect Transistors”, *IEEE Electron Device Letters*, 41, 276 (2020).
- [29] T. A. Karatsori, C. G. Theodorou, E. Josse, C. A. Dimitriadis, , and G. Ghibaudo, “All operation region characterization and modeling of drain and gate current mismatch in 14nm Fully Depleted SOI MOSFETs”, *IEEE Trans. Electron Devices*, 64, 2080 (2017).