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(Invited) How to Achieve Low Thermal Resistance and High Electrothermal Ruggedness in Ga_2O_3 Devices?

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Ultra-wide bandgap gallium oxide (Ga_2O_3) devices have recently emerged as promising candidates for power and RF electronics. The low thermal conductivity of Ga_2O_3 has arguably been the most serious concern for these devices. Despite many simulation studies, there still lacks an experimental report on the thermal resistance and electrothermal ruggedness of a large-area, packaged Ga_2O_3 device. Recently, our team for the first time demonstrated large-area Ga_2O_3 devices with different packaging configurations and measured the thermal resistance and surge current capabilities of these packaged Ga_2O_3 devices. This paper reviews the key results in our efforts. It is shown that, contrary to some popular belief, Ga_2O_3 devices with proper packaging can achieve high thermal performance in both short transients and the steady state. The double-side-packaged Ga_2O_3 Schottky rectifiers show a junction-to-case thermal resistance lower than that of the similarly-rated commercial SiC Schottky rectifiers. In addition, these Ga_2O_3 rectifiers can survive a higher peak surge current as compared to SiC rectifiers. The critical enabler for these excellent performances is the direct junction cooling with minimal heat going through the Ga_2O_3 chip. Our work proves the viability of Ga_2O_3 devices for high power applications and manifests the significance of packaging for their die-level thermal management.

Introduction

Ultra-wide-bandgap (UWBG) semiconductor gallium oxide (Ga_2O_3) has been promoted for years as a promising candidate for power electronics and RF applications, due to its high critical electrical field (E-field), controllable n-type doping, and the availability of large-diameter wafers by the melt growth (1, 2). Recently, kilovolt-class Ga_2O_3 Schottky barrier diodes (SBDs) have been demonstrated with a peak junction E-field exceeding the critical E-field of GaN and SiC (3-5). However, a fundamental limitation of Ga_2O_3 is its low thermal conductivity (k_T = 0.1-0.3 $Wcm^{-1}K^{-1}$), which is about 1/6 of the k_T of Si, 1/10 of GaN, and 1/20 of SiC. The resulting high thermal resistance of Ga_2O_3 chip has brought serious concerns regarding the current and power scalability of Ga_2O_3 devices and their electrothermal ruggedness. As a result, questions have long persisted on the true viability of Ga_2O_3 devices for industrial power and RF applications.

Despite many simulation and modeling works on the thermal management of Ga_2O_3 devices (6-9), there has been no experimental report on the packaging and thermal management of large-area Ga_2O_3 devices. The lack of these data makes it difficult to compare Ga_2O_3 with commercial device technologies (e.g., Si, SiC, GaN) and evaluate the true application space of Ga_2O_3 devices. Some recent works characterized the channel (or junction) temperature in Ga_2O_3 devices (10-12), and developed various methods to reduce the temperature (13, 14), but all of these devices have small areas with a current much lower than 1 Amp, and none of these devices are packaged.

To fill these gaps, our team for the first time demonstrated large-area, packaged Ga_2O_3 devices and characterized their thermal resistance and transient electrothermal ruggedness. This paper reviews the key results, with the details published in (15-18). Vertical Ga_2O_3 SBDs with a 3×3 mm^2 Schottky contact area were fabricated, showing a forward current over 20 A and a breakdown voltage (*BV*) over 600 V. Small-area Ga_2O_3 SBDs fabricated on the same wafer exhibited capabilities to operate at high temperatures up to 600 K (18). The fabricated large-area SBDs were then packaged in the bottom- and double-side-cooling configurations using the nanosilver sintering as the die attach.

To evaluate the device's steady-state thermal performance, the junction-to-case thermal resistance ($R_{\theta JC}$) of a double-side-packaged Ga_2O_3 SBD was measured in the bottom-side- and junction-side-cooling configurations. The $R_{\theta JC}$ is an essential metric in the datasheet of any commercial power device. The $R_{\theta JC}$ characterization was based on the transient dual interface method, i.e., JEDEC 51-14 standard (19). The $R_{\theta JC}$ of the junction- and bottom-cooled Ga_2O_3 SBDs was measured to be 0.5 K/W and 1.43 K/W, respectively. The former $R_{\theta JC}$ was found to be lower than that of similarly-rated commercial SiC SBDs. This low $R_{\theta JC}$ is attributable to the heat extraction directly from the Schottky junction instead of through the Ga_2O_3 chip.

Surge current is an essential ruggedness metric listed in any power diode's datasheet and the most important indicator of a device's transient electrothermal ruggedness (15, 20). It measures the device's capability of temporarily sustaining a current much higher than the rated current. A surge-current test circuit was prototyped to produce a 10-ms-wide half-sinusoidal current waveform based on the JEDEC standard. The surge-current tests revealed a critical surge current of 37.5 A for the single-side-packaged Ga_2O_3 SBD and 68 A for the double-side-packaged Ga_2O_3 SBD. The latter Ga_2O_3 SBD shows a ratio between the peak surge current and the rated current higher than that of the similarly-rated commercial SBDs. This superior capability is attributable to the small temperature dependence of on-resistance (R_{ON}) of Ga_2O_3 devices, which strongly reduces the thermal runaway, and the double-side-cooled packaging, which allows direct junction cooling.

Our results have removed some critical concerns regarding the thermal performance and ruggedness of Ga_2O_3 devices and suggested the strong need for the device-packaging co-design for Ga_2O_3 devices. The co-optimization should also be performed in the context of circuit operations, e.g., transient dynamics in a surge (short) current profile.

Bare-Die Device: Fabrication and High-Temperature Characteristics

High-temperature characterizations of bare-die devices are the pre-requisites for the thermal study of packaged Ga_2O_3 devices. Hence, we first fabricated small-area vertical

Ga_2O_3 SBDs (3, 18). A critical knowledge gap of Ga_2O_3 devices in the literature was the lack of reports on the high-voltage blocking capability at high temperatures. This gap makes the applicability of Ga_2O_3 devices in harsh-environment power applications questionable. To this end, we focused on evaluating the high-voltage blocking capabilities of our bare-die Ga_2O_3 SBDs at high temperatures.

The commercially available Ga_2O_3 wafer from Novel Crystal Technologies consists of a 10-µm Si-doped n-Ga_2O_3 epitaxial drift layer (net donor concentration ~2×10^{16} cm^{-3}) grown on a 2-inch n^+-Ga_2O_3 (001) substrate (Sn: 1.3×10^{19} cm^{-3}). The substrate was thinned down to a thickness of 500 µm. The device fabrication is detailed in (3, 18, 21, 22). A layer of SiO_2 was deposited, followed by patterned wet etch, which functions as the hard mask for Ga_2O_3 mesa etch. Then a 1-µm-thick spin-on-glass (SOG) was deposited and selectively wet etched to produce a controllable bevel angle (3), which functions as the field plate (FP) dielectrics. A Ti/Au Ohmic contact is formed on the backside of the substrate, and a Ni/Au stack is deposited as the Schottky and FP metals. The device structure is illustrated in Fig. 1(a). Fig. 1(b) shows scanning electron microscopy (SEM) images of the edge termination region, revealing a bevel angle of 45° in the FP dielectrics and Ga_2O_3 mesa. Fig. 1(c) and (d) show the forward I-V and high-bias reverse I-V characteristics of the fabricated Ga_2O_3 SBDs, respectively, demonstrating the capability of blocking at least 500 V up to 600 K. The high-bias leakage current can be explained by a combination of the thermionic-field emission (TFE) across the Schottky barrier and the electron hopping via the defect states in the depletion region (18). The latter mechanism was widely reported in other wide-bandgap high-voltage power devices, e.g., GaN (23-27) and SiC (28-30). These results verify the high-temperature stability of high-voltage Ga_2O_3 SBDs.

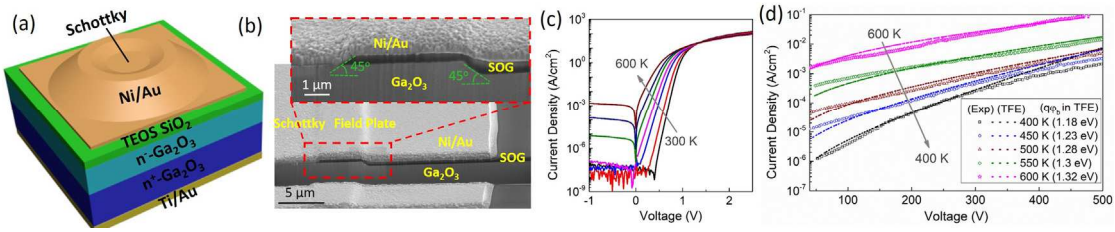

Figure 1. (a) Schematic of the fabricated small-area Ga_2O_3 SBD, and (b) the SEM image of the edge termination region. (c) Forward and (d) reverse I-V characteristics of the Ga_2O_3 SBD at various temperatures from 300 K to 600 K.

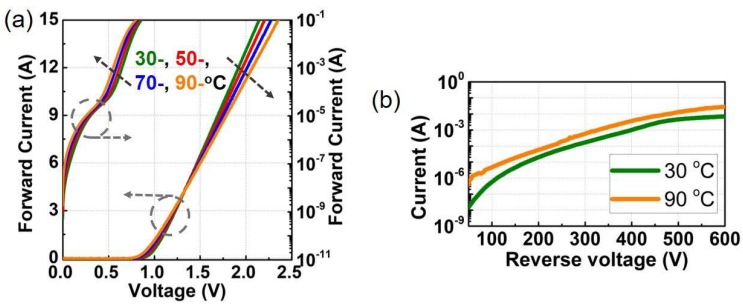

Figure 2. (a) Forward and (b) reverse I-V characteristics of the large-area vertical Ga_2O_3 SBD at various temperatures from 30 °C to 90 °C.

Subsequently, large-area vertical Ga_2O_3 SBDs with a Schottky contact area of 3×3 mm^2 were fabricated on the same wafer. To simplify the device structure to maximize the device fabrication yield (and leave margin for packaging yield), our first-generation large-area Ga_2O_3 SBDs employ only a planar FP without the mesa structure. According to the simulation (3), a small FP bevel angle can reduce the E-field crowding. Hence, a ~15° bevel angle in the FP was fabricated. Fig. 2(a) and (b) show the forward and reverse I-V characteristics of the fabricated large-area Ga_2O_3 SBDs, respectively, revealing a 0.83 V turn-on voltage (V_{ON}) extracted at 1 A/cm^2, a forward current of 15 A at 2.15 V, an on/off ratio of ~10^{10}, and a capability to block at least 600 V.

Device Packaging

The packaging started with depositing 100-nm-thick Ti and 200-nm-thick Ag on both sides of contacts as adhesion layers to the sintered nanosilver bond-line. Ti also serves as a barrier layer to prevent metal diffusion during the sintering process. A nanosilver paste from NBE Technologies was then used for the die attach by a pressureless sintering process in air (31, 32). More details on the sintering process were reported in (16). Devices with single-side- and double-side-cooled packages were then prototyped, as shown in Fig. 3(a) and (b). For the single-side-cooled package, the cathode of the Ga_2O_3 chip was sintered on a 1-mm thick Ag plate, and wire-bonds were attached on the top anode. For the double-side-cooled package, each terminal of the Ga_2O_3 chip was sintered on a 1-mm thick Ag plate. Fig. 3(c) shows a double-side-cooled package mounted on a ceramic substrate with wire-bond connections, ready for surge tests. Substrate and wire-bonds were not used for the thermal resistance tests.

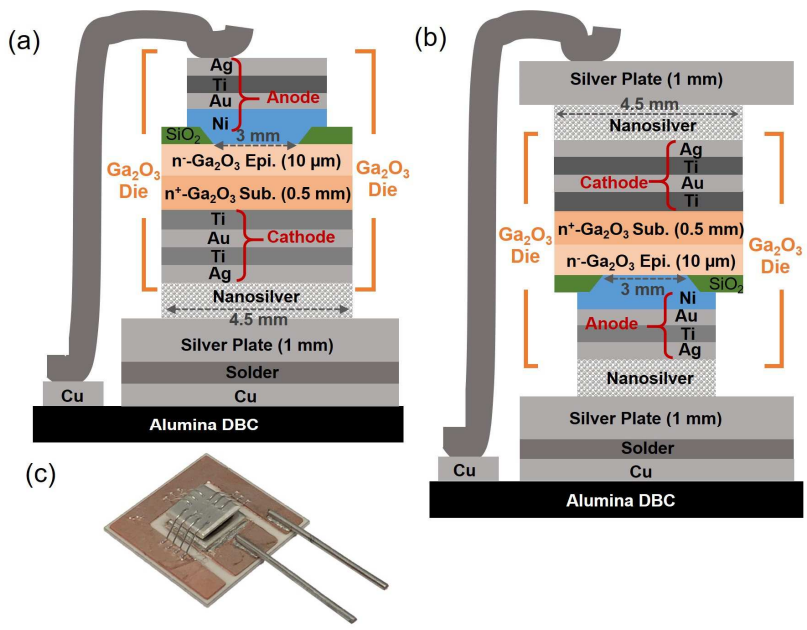

Figure 3. Schematic of the large-area Ga_2O_3 packaged in (a) single-side-cooled and (b) double-side-cooled configurations. (c) Photo of a double-side-packaged device.

Thermal Resistance Measurement

The $R_{\theta JC}$ measurement was based on the transient dual interface method (TDIM) (i.e., JEDEC 51-14 standard (19)). This TDIM method relies on two transient thermal

impedance curves (Z~t) measured with different contact thermal resistances between the package case surface and the ambient. The Z value at the separation point of the two curves is extracted as the device steady-state $R_{\theta JC}$ (19).

Fig. 4(a) shows our $R_{\theta JC}$ measurement set-up using an Analysis Tech Phase 12B Semiconductor Thermal Analyzer. The Ga_2O_3 SBD was placed on a water-cooling cold plate with a 26 °C constant temperature. An indium foil was attached to each Ag plate to conduct electric signals. The top plastic clamp has very low thermal conductivity, ensuring the heat extraction dominantly towards the bottom water-cooling plate. Fig. 4(b) and (c) show the $R_{\theta JC}$ measurement of the double-side packaged Ga_2O_3 SBD under bottom-side- and junction-side-cooling.

The $R_{\theta JC}$ measurements started by applying a dc bias to the SBD for self-heating until the junction reaches the steady state (junction temperature = T_j). The power was then cut off, and the T_j evolution was measured by monitoring a thermo-sensitive electrical parameter (TSEP) (33). For our Ga_2O_3 SBDs, the TSEP was selected as the forward voltage at 10 mA, which showed good linearity with T_j. With T_j, the Z~t curve was calculated. For each $R_{\theta JC}$ test, two Z~t curves were acquired by using two different thermal interface materials (TIMs) between the indium foil and the cold plate, i.e., some silicone oil (lower k_T) and some thermal grease (higher k_T). The separation point of the two heating Z~t curves was extracted as $R_{\theta JC}$ (19). Fig. 4(d) and (e) show the measured Z~t curves of our packaged Ga_2O_3 SBD in the bottom-side- and junction-side-cooling schemes, respectively, revealing a much lower $R_{\theta JC}$ (0.5 K/W) under the junction-side cooling as compared to the $R_{\theta JC}$ (1.43 K/W) under the bottom-side cooling.

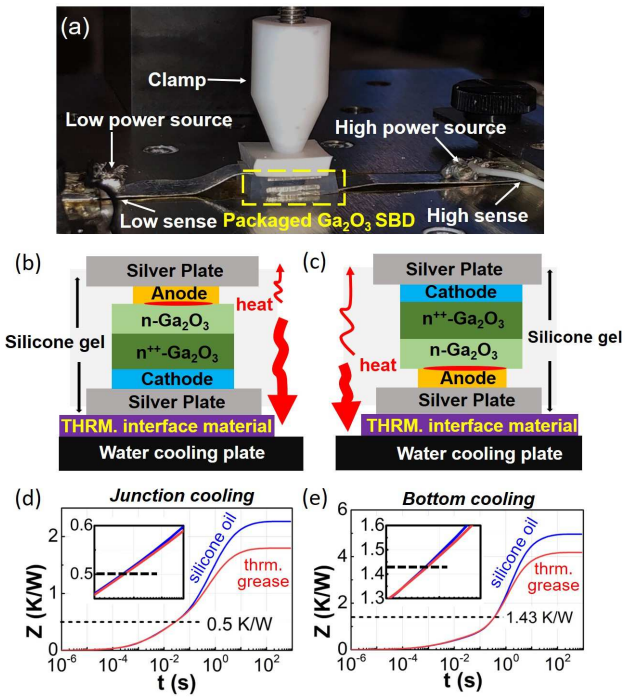

Figure 4. (a) Photo of the thermal resistance test setup. Schematic of $R_{\theta JC}$ measurements under (b) bottom-side cooling and (c) junction-side cooling. Z~t curves of the Ga_2O_3 SBD measured with two TIMs under (d) junction-side- and (e) bottom-side-cooling, and the extracted $R_{\theta JC}$ under two cooling schemes.

Table I compares the $R_{\theta JC}$ of our Ga_2O_3 SBDs against commercial 600-V SiC SBDs with a similar current rating and different TO-series packages. The $R_{\theta JC}$ of our junction-side cooled Ga_2O_3 SBD is lower than that of commercial SiC SBDs with a similar package size and current rating. This suggests the feasibility of employing the proper packaging to overcome the low k_T of Ga_2O_3.

TABLE I. Thermal resistance comparison between Ga_2O_3 SBDs and commercial SiC SBDs with similar current ratings and package sizes.

Device	Package	Package Size* (mm^2)	V_{ON} (V)	I_F (A)**	Cooling	$R_{\theta JC}$ (K/W)
Ga_2O_3 SBD (this work)	Double-side	7.3×7.3	0.83	13	Junction	0.5
					Bottom	1.43
SiC SBD (C3D10060G)	TO-263-2	6.5×7.9	0.85	18	Bottom	1.2
SiC SBD (E3D08065G)	TO-263-2	6.5×7.9	0.85	14.5	Bottom	1.47
SiC SBD (C6D04065E)	TO-252-2	5.2×4.3	0.85	12	Bottom	2.89

*Size of the die-attached thermal pad. **Forward current at 2 V.

Surge Current Test

Fig. 5(a) and (b) show the surge-current test circuit and the prototype, respectively. The working principle and implementation of the test circuit are detailed in (16, 20). A 10-ms-wide half-sinusoidal current waveform was produced by a resonance circuit comprising a 2.2-mH inductor and a 4.7-mF capacitor). SiC MOSFETs were used as the control switches. The peak surge current (I_{peak}) was stepped up by increasing the power supply voltage (V_{DC}). After each single-pulse surge-current test, the device was measured on the curve tracer to identify any possible degradation. It should be noted that the device cooling in this section is in the context of a 10-ms transient instead of the steady state. The thickness of Ag plate (1 mm) is designed to ensure that the heat diffusion is confined in the plate during the 10-ms transient (15, 16), while the outer solder, DBC, and wire bond do not contribute to the heat dissipation in this transient.

Fig. 5(c) and (d) show the current/voltage waveforms in the surge current tests with increased I_{peak} for the Ga_2O_3 SBDs with the bottom-side and double-side packages. The Ga_2O_3 SBD with the bottom-side-cooling package was found to fail in the surge test with an I_{peak} of 39 A. The failure I_{peak} is much higher (70 A) in the double-side-cooled SBD. Fig. 5(e) and (f) show the surge I-V loops of the SBDs with both types of packages. Both I-V loops are clockwise, due to the increased R_{on} at higher T_j, and the loop area is correlated to the R_{on} (and T_j) increase in the surge test. With a similar I_{peak} (e.g., 30 A), the loop area of the double-side-cooled SBD is smaller than that of the bottom-side-cooled SBD, suggesting a smaller T_j increase. Transfer characteristics of the double-side-cooled SBD were measured after each surge test with increased I_{peak}. Almost no device degradation is shown with I_{peak} up to 60 A. At 68 A I_{peak}, higher leakage current is present, suggesting that degradation emerges in the Schottky contact.

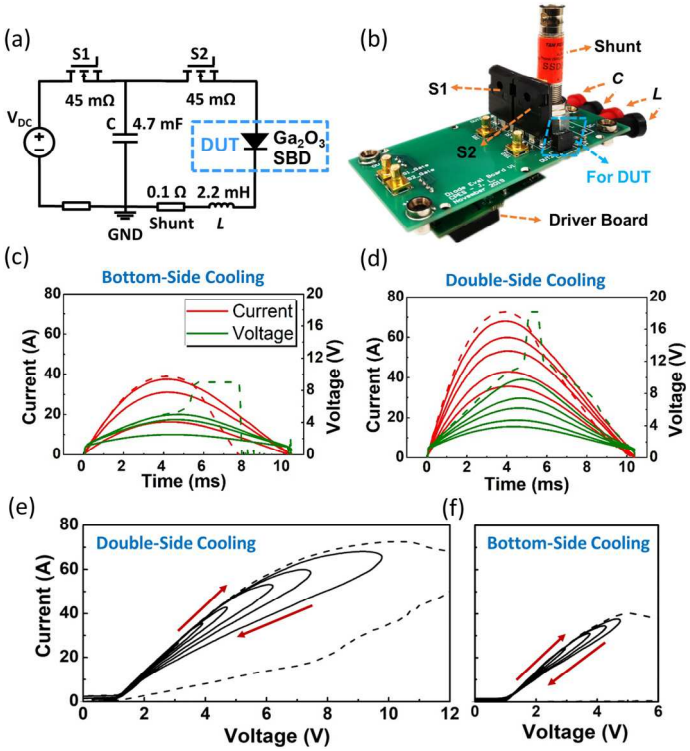

Figure 5. (a) Circuit diagram and (b) photo of the surge current test board. Current/voltage waveforms of the (c) bottom-side- and (d) double-side-cooled Ga_2O_3 SBDs in the surge current tests. I-V loops of the (e) double-side- and (f) bottom-side-cooled devices.

An important device ruggedness metric for practical power applications is the ratio between the maximum I_{peak} in 10-ms surge current tests and the rated current. The rated currents of the bottom-side-cooled and double-side-cooled Ga_2O_3 SBDs were determined by the calibrated static electrothermal simulations (16) when the T_j reaches 150 °C, being 6.2 A for the bottom-side-cooled device and 9.2 A for the double-side-cooled device. For comparison, several commercial SiC SBDs with similar ratings (600-V voltage rating and 4~11 A current ratings) were tested in the same surge current test setup to identify their maximum surge currents. As shown in Table II, despite the low k_T of Ga_2O_3 (1/20 of SiC), the fabricated Ga_2O_3 SBDs, particularly the ones with double-side-cooling package, show comparable, or even superior surge current capabilities as compared to the similarly-rated commercial SiC SBDs.

TABLE II. Comparison of the surge current capability of SiC and Ga_2O_3 Schottky barrier diodes

Device	Rated Current (A)	Max Surge Current (A)	Max surge current over rated current
SiC SBD (CSD01060A)	4	20.3	5.1
SiC SBD (CSD02060A)	8	26.9	3.36
SiC SBD (CSD03060A)	11	31.8	2.89
Bottom-side-packaged Ga_2O_3 SBD	6.2	37.5	6.05
Double-side-packaged Ga_2O_3 SBD	9.2	68	7.4

Mixed-Mode Electrothermal Simulations

To understand the electrothermal dynamics within the device structure, mixed-mode electrothermal TCAD simulations were performed in Silvaco Atlas. The mixed-mode simulation combines physics-based device models and circuit arrangements, enabling to reveal the device internal dynamics in at any switching transient. Some exemplar mixed-mode TCAD simulations for power devices are available in (34-36). In this work, self-consistent electrothermal device models are solved in a circuit arrangement consistent with that shown in Fig. 5(a). The electrothermal model settings and boundary conditions are similar to (37). The temperature-dependent k_T, heat capacity, and electron mobility models for Ga_2O_3 and nanosilver die attach are detailed in (16).

Fig. 6(a)-(d) show the simulated distributions of heat flux and temperatures in the double-side-cooled SBD at the peak T_j transient in the surge current test with $I_{peak} \sim 68$ A. Fig. 6(a) and (c) show the simulated contours in the entire device structure, while Fig. 6(b) and (d) show the junction region. The heat flux distribution in the double-side-cooled SBD reveals that most heat is dissipated directly from the Schottky junction instead of through the Ga_2O_3 die. This explains the lower T_j in the double-side-cooled SBD as compared to that in the bottom-side-cooled SBD at a similar I_{peak}. As shown in Fig. 6(d), the simulated peak temperature is located within the Ga_2O_3 drift layer in the double-side-cooled SBD. By contrast, in the usual static operations of a SBD, the peak temperature is located at the Schottky junction. The double-side package moves the peak temperature from the Schottky contact region into the robust bulk Ga_2O_3, which allows the device to sustain a higher T_j before degradation of the Schottky contact.

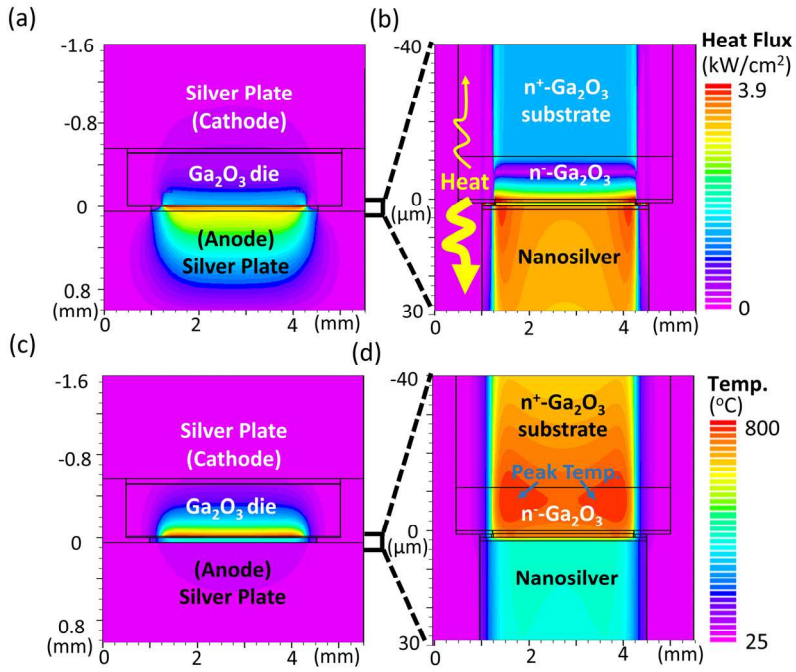

Figure 6. Simulated heat flux contour in the (a) entire packaged device and (b) device junction region, and simulated temperature distributions in the (c) entire device and (d) junction region, in a double-side-packaged Ga_2O_3 SBD at the peak T_j transient in the surge current test with 68 A T_{peak}.

Strategies for Further Improvement

The well-calibrated electrothermal simulations allow an exploration of the further improvement in the steady-state and transient thermal performance of Ga_2O_3 devices. Fig. 7 shows the simulated junction-to-coolant (-ambient) thermal resistance as a function of heat transfer coefficient (HTC), in which the HTC represents different cooling methods, for our vertical Ga_2O_3 SBDs in the bottom-, junction- and double-side cooling schemes. The results suggest that the junction-cooling is essential for Ga_2O_3 devices, as it allows over 60-70% reduction in the junction-to-ambient thermal resistance. The double-side-cooling can further reduce the junction-to-ambient thermal resistance by 30~40%. An HTC over 10^3 W/m^{2}K (e.g., forced water cooling) is preferable for external cooling; a lower HTC may lead to a fast increase in the junction-to-ambient thermal resistance for Ga_2O_3 devices.

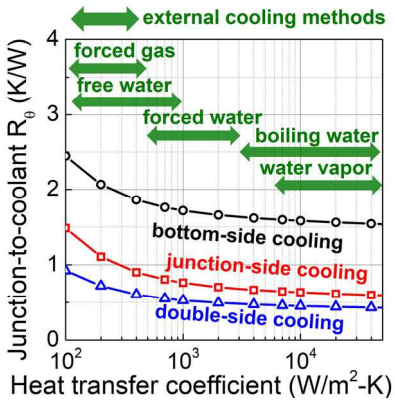

Figure 7. Simulated junction-to-coolant thermal resistance of the Ga_2O_3 SBD as a function of HTC at the case surface, under the bottom-, junction- and double-side cooling. The HTC ranges for different external cooling techniques are marked in green.

For the transient electrothermal ruggedness, the simulation in the previous section has shown that most of the heat does not reach the external surface of the 1-mm Ag plate. Hence, if this Ag plate continues to apply, the external cooling with different HTC is not expected to significantly impact the device's surge current capability. Instead, the device and package structure within the Ag plate are more critical.

To further understand the design space of the surge current capabilities of Ga_2O_3 devices, two additional thermal management approaches were considered: thinning of the Ga_2O_3 substrate, and bonding Ga_2O_3 device layers to a SiC substrate (13, 14). Using the calibrated simulation models, Fig. 8 shows the simulated peak T_j as a function of surge I_{peak} for the different Ga_2O_3 device structures (16). A similarly-rated SiC SBD with identical substrate thickness was also simulated as a reference. In Ga_2O_3 devices, the substrate thinning provides little improvement in the surge current capabilities when compared to the use of junction cooling, since most of the heat is directly extracted from the junction. Whereas, if low-k_T SiC substrate is used in Ga_2O_3 devices, the heat extraction through the bulk chip can be improved significantly. Hence, the surge current capabilities can be further improved in the double-side-cooled Ga_2O_3-on-SiC device as compared to the bottom-side-cooled one. Finally, the simulation predicts that the Ga_2O_3 SBDs on SiC substrate can provide significantly superior surge current capability when

compared to the similarly-rated SiC SBDs, as the Ga_2O_3-on-SiC SBD combines the inherent thermal stability of Ga_2O_3 devices and the high k_T of SiC substrate.

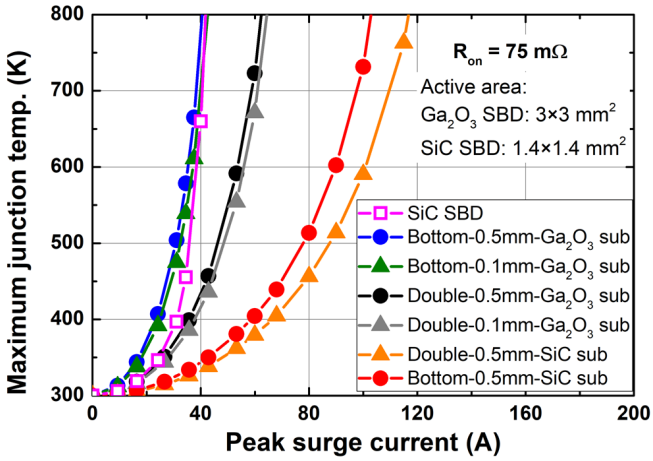

Figure 8. Simulated max peak T_j as a function of peak surge current in 10-ms surge tests for the double-side-cooled and bottom-side-cooled Ga2O3 SBDs on the 0.5-mm-thick Ga_2O_3 substrate, 0.1-mm-thick Ga_2O_3 substrate, and 0.5-mm-thick SiC substrate. A thermal boundary resistance of 0.01 K/(W·cm^2) was set at the Ga_2O_3/SiC bonding interface. Identical electrical conductivity was set for Ga_2O_3 and SiC substrates. The simulated SiC SBD has a 0.5-mm-thick substrate and a bottom-side-cooled package. Caughey-Thomas model was used for the SiC electron mobility.

Summary

The low k_T of Ga_2O_3 is a key roadblock to remove for the industrial applications of any Ga_2O_3 power and RF devices. To ensure the relevance to future applications, we believe that the thermal management of Ga_2O_3 devices has to be studied in the context of large-area, packaged device or, in the future, the power modules. This is because many thermal parameters revealed in small-area devices cannot be scaled to predict the performance of large-area devices by simply considering the device area enlargement, not to mention the electro-thermal coupled parameters such as the surge current capability.

To this end, we for the first time demonstrated the large-area Ga_2O_3 devices with different packaging configurations and measured the thermal resistance and surge current capabilities of these packaged Ga_2O_3 devices. We found that, contrary to some popular belief, Ga_2O_3 devices with proper packaging can achieve high thermal performance in both short transients and the steady state. The double-side-packaged Ga_2O_3 Schottky rectifiers show a junction-to-case thermal resistance lower than that of the similarly-rated commercial SiC Schottky rectifiers. In addition, these double-side-packaged Ga_2O_3 rectifiers can survive a higher peak surge current as compared to SiC rectifiers. The critical enabler for these excellent performances is the direct junction cooling with minimal heat going through the Ga_2O_3 chip. Strategies for further improving the transient and steady-state thermal performance of Ga_2O_3 devices have been identified, with the former being the transfer of Ga_2O_3 device layers to low-k_T substrate, and the latter being the addition of external cooling technologies. Our work proves the viability of Ga_2O_3 devices for high power applications, manifests the significance of packaging for their die-

level thermal management, and suggests some new capabilities that Ga_2O_3 devices can enable for power electronics.

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