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# Low Thermal Resistance (0.5 K/W) Ga<sub>2</sub>O<sub>3</sub> Schottky Rectifiers with Double-Side Packaging

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**Abstract**— The low thermal conductivity of Ga<sub>2</sub>O<sub>3</sub> has arguably been the most serious concern for Ga<sub>2</sub>O<sub>3</sub> power and RF devices. Despite many simulation studies, there is no experimental report on the thermal resistance of a large-area, packaged Ga<sub>2</sub>O<sub>3</sub> device. This work fills this gap by demonstrating a 15-A double-side packaged Ga<sub>2</sub>O<sub>3</sub> Schottky barrier diode (SBD) and measuring its junction-to-case thermal resistance ( $R_{\theta JC}$ ) in the bottom-side- and junction-side-cooling configurations. The  $R_{\theta JC}$  characterization is based on the transient dual interface method, i.e., JEDEC 51-14 standard. The  $R_{\theta JC}$  of the junction- and bottom-cooled Ga<sub>2</sub>O<sub>3</sub> SBD was measured to be 0.5 K/W and 1.43 K/W, respectively, with the former  $R_{\theta JC}$  lower than that of similarly-rated commercial SiC SBDs. This low  $R_{\theta JC}$  is attributable to the heat extraction directly from the Schottky junction instead of through the Ga<sub>2</sub>O<sub>3</sub> chip. The  $R_{\theta JC}$  lower than that of commercial SiC devices proves the viability of Ga<sub>2</sub>O<sub>3</sub> devices for high-power applications and manifest the significance of proper packaging for their thermal management.

**Index Terms**— ultra-wide bandgap, gallium oxide, packaging, Schottky barrier diodes, thermal resistance.

## I. INTRODUCTION

Ultra-wide-bandgap semiconductor gallium oxide (Ga<sub>2</sub>O<sub>3</sub>) has been promoted for years as a promising candidate for power electronics and RF applications, due to its high critical electrical field, controllable n-type doping, and the availability of large-diameter wafers by the melt growth [1]–[5]. Whereas a fundamental limitation of Ga<sub>2</sub>O<sub>3</sub> is its low thermal conductivity ( $k_T = 0.1\text{--}0.3\text{ Wcm}^{-1}\text{K}^{-1}$  [1]), which is about 1/6 of the  $k_T$  of Si, 1/10 of GaN, and 1/20 of SiC. The resulting high thermal resistance of Ga<sub>2</sub>O<sub>3</sub> chip has brought serious concerns regarding the current and power scalability of Ga<sub>2</sub>O<sub>3</sub> devices and their competitiveness in industrial power and RF applications.

The thermal resistance is an essential metric in the datasheet of any power device. Despite some simulation and modeling works [6]–[11], there has been no experimental reports of the thermal resistance of a large-area, packaged Ga<sub>2</sub>O<sub>3</sub> device. The lack of this data makes it difficult to compare Ga<sub>2</sub>O<sub>3</sub> with commercial device technologies (e.g., Si, SiC, GaN) and evaluate the application space of Ga<sub>2</sub>O<sub>3</sub> devices. Some recent works characterized the channel (or junction) temperatures in Ga<sub>2</sub>O<sub>3</sub> devices [12]–[15] and studied different approaches to lower device temperatures, e.g., heterogenous integration [16]–[20] and substrate thinning [21]. However, all of these devices

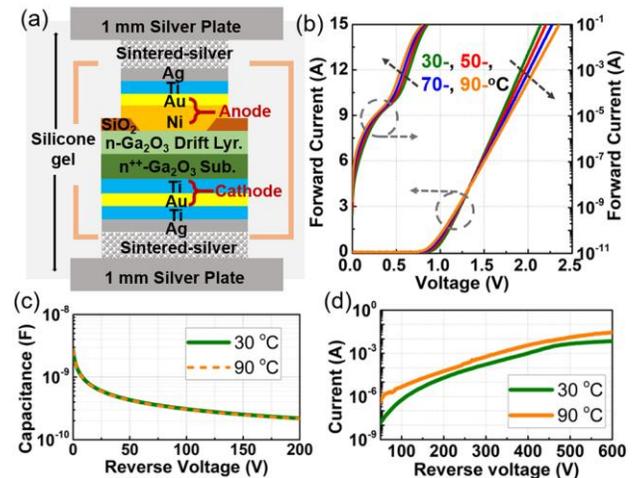


Fig. 1 (a) Schematic of the double-side packaged Ga<sub>2</sub>O<sub>3</sub> SBD encapsulated in silicone gel. Temperature-dependent (b) forward I-V, (c) C-V and (d) reverse I-V (up to 600 V) characteristics of the packaged device.

have small areas with a current much lower than 1 Amp, and none of these devices are packaged.

This work fills this critical knowledge gap by demonstrating a 15-A double-side-packaged vertical Ga<sub>2</sub>O<sub>3</sub> Schottky barrier diode (SBD) and characterizing its junction-to-case thermal resistance ( $R_{\theta JC}$ ) following the JEDEC 51-14 standard [22]. The  $R_{\theta JC}$  of the same device were measured in the bottom-side- and junction-side-cooling schemes, where the bottom-side cooling is dominant in the packages of commercial devices. The  $R_{\theta JC}$  of the junction-cooled Ga<sub>2</sub>O<sub>3</sub> SBD was found to be smaller than that of similarly-rated commercial SiC SBDs. These results remove some of the key thermal concerns for Ga<sub>2</sub>O<sub>3</sub> devices.

## II. DEVICE FABRICATION AND PACKAGING

Fig. 1(a) shows the schematic of the packaged Ga<sub>2</sub>O<sub>3</sub> SBD. The Ga<sub>2</sub>O<sub>3</sub> wafer consists of a 10- $\mu\text{m}$  n-Ga<sub>2</sub>O<sub>3</sub> drift layer (Si:  $\sim 10^{16}\text{ cm}^{-3}$ ) grown on a 2-inch n<sup>+</sup>-Ga<sub>2</sub>O<sub>3</sub> substrate. The substrate was thinned down to 500  $\mu\text{m}$  [23]. The device fabrication is similar to the ones in [23], [24]. The cathode ohmic contact was formed by Ti/Au, and the anode Schottky contact by Ni/Au. A planar field plate was made by 1- $\mu\text{m}$  SiO<sub>2</sub>. A Ti/Ag (100/200 nm) stack was deposited on both contacts as adhesion layers to the sintered nanosilver bond-line. Ti also serves as a barrier layer to prevent the metal diffusion in the sintering process.

The device packaging process was similar to that in [25]. For

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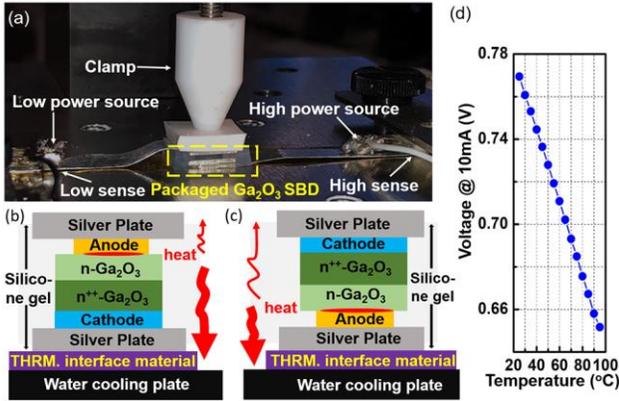


Fig. 2. (a) Photo of the test setup. Schematic of  $R_{\theta}$  measurements under (b) bottom-side cooling and (c) junction-side cooling. (d) The forward voltage at 10 mA current as a function of temperature of the packaged  $\text{Ga}_2\text{O}_3$  SBD.

die attach, a 50- $\mu\text{m}$ -thick nanosilver paste was sintered without pressure at 250  $^{\circ}\text{C}$  [26]. Each side of the chip was bonded to a 1-mm-thick silver (Ag) plate. Some low- $k_T$  silicone gel was applied to encapsulate the chip. The Schottky contact area was  $3 \times 3 \text{ mm}^2$ , the total  $\text{Ga}_2\text{O}_3$  chip size was  $4.6 \times 4.6 \text{ mm}^2$ , and the Ag plate size was  $7.3 \times 7.3 \text{ mm}^2$ .

Fig. 1(b)-(d) show the forward I-V, reverse C-V, and reverse I-V characteristics of the packaged  $\text{Ga}_2\text{O}_3$  SBD, revealing a turn-on voltage ( $V_{\text{ON}}$ ) of 0.83 V extracted at  $1 \text{ A/cm}^2$ , a forward current of 15 A at 2.15 V, an on/off ratio of  $\sim 10^{10}$  extracted at 2 V/-50 V, and a breakdown voltage ( $BV$ ) over 600 V. Note that a simple planar field plate was used in this work, hence the  $BV$  and reverse leakage current have much room for improvement. By adding a mesa, a  $BV$  up to 1100 V was demonstrated on a similar wafer in small-area devices [23]. The  $N_D$  extracted from the C-V characteristics is  $\sim 2 \times 10^{16} \text{ cm}^{-3}$ , and it shows small temperature dependence.

### III. THERMAL RESISTANCE MEASUREMENTS

The  $R_{\theta\text{JC}}$  measurement was based on the transient dual interface method (TDIM) (i.e., JEDEC 51-14 standard [22]). This TDIM method relies on two transient thermal impedance curves ( $Z \sim t$ ) measured with different contact thermal resistances between the package case surface and the ambient. The  $Z$  value at the separation point of the two curves is close to the device steady-state  $R_{\theta\text{JC}}$  [22]. This method avoids the errors caused by traditional thermocouple methods [27], and has been widely used for Si [28], [29], SiC [30], and GaN [31] devices.

Fig. 2(a) shows our  $R_{\theta\text{JC}}$  measurement set-up using an Analysis Tech Phase 12 Semiconductor Thermal Analyzer. The  $\text{Ga}_2\text{O}_3$  SBD was placed on a water-cooling cold plate with a 26 $^{\circ}\text{C}$  constant temperature. An indium foil was attached to each Ag plate to conduct electric signals. A top plastic clamp applied a  $\sim 15$ -psi pressure to ensure good and consistent contacts. As this clamp has very low thermal conductivity, this setup allows heat extraction dominantly towards the bottom water-cooling plate. Fig. 2(b) and (c) show the bottom- and junction-cooling measurements of the same double-side packaged  $\text{Ga}_2\text{O}_3$  SBD.

In the TDIM method, the junction temperature ( $T_j$ ) is usually monitored by continuously measuring a thermo-sensitive electrical parameter (TSEP) [32]. The forward voltage at 10 mA was selected as the TSEP for our  $\text{Ga}_2\text{O}_3$  SBDs, which shows an

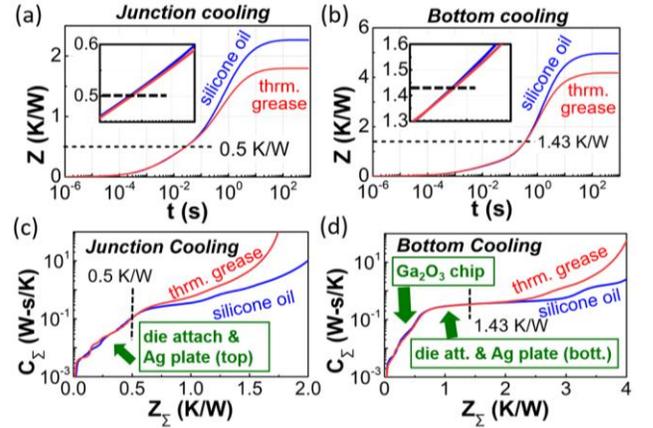


Fig. 3. Transient thermal impedance curves of the  $\text{Ga}_2\text{O}_3$  SBD measured with two TIMs under the (a) junction- and (b) bottom-side cooling. The insets show the zoom-in plot of the separation point. Calculated structure function with two TIMs in the (c) junction- and (d) bottom-side cooling.

excellent linearity with the temperature (Fig. 2(d)). This test was performed in an oven with the thermocouple and electrical wires placed into the oven via small holes on the oven surface to allow the TSEP and temperature measurements.

The  $R_{\theta\text{JC}}$  measurements started by applying a forward dc bias to the SBD for self-heating, producing a power ( $P_H$ ), until the steady state was reached with a constant  $T_j$  ( $T_{j0}$ ). Subsequently, the dc power was cut off, and the TSEP was monitored to obtain the evolution of  $T_j(t)$  in the cooling phase. The  $Z \sim t$  curve was calculated by  $Z_{\theta\text{JC}}(t) = (T_{j0} - T_j(t))/P_H$  [22], [27]. As our TSEP is in the SBD subthreshold region, minimal heating is produced in its testing ( $< 7.6 \text{ mW}$ ), and a high signal-to-noise ratio are ensured in the  $Z$  measurement.

For each  $R_{\theta\text{JC}}$  test, two  $Z \sim t$  curves were acquired by using two different thermal interface materials (TIMs) between the indium foil and the cold plate, i.e., some silicone oil (lower  $k_T$ ) and some thermal grease (higher  $k_T$ ). The separation point of the two heating  $Z \sim t$  curves was extracted as  $R_{\theta\text{JC}}$  by the Analyzer software following the JEDEC standard [22]. The  $R_{\theta\text{JC}}$  of a commercial SiC SBD (SCS220KGHR) was first measured. The measured value (0.6 K/W) agreed with the datasheet value (0.62 K/W), validating our test setup and procedure.

Fig. 3(a) and (b) show the measured  $Z \sim t$  curves of our packaged  $\text{Ga}_2\text{O}_3$  SBD in the bottom-side- and junction-side-cooling schemes, respectively, revealing a much lower  $R_{\theta\text{JC}}$  (0.5 K/W) under the junction-side cooling as compared to the  $R_{\theta\text{JC}}$  (1.43 K/W) under the bottom-side cooling.

A cumulative structure function can be calculated from each  $Z \sim t$  curve [22], which gives the sum of thermal capacitances ( $C_{\Sigma}$ ) with respect to the sum of thermal resistances ( $R_{\Sigma}$ ) in the packaged device structure, measured from the point of heating excitation (i.e., junction) toward the ambient. Each slope in this function represents either a new material or an increase in the cross sectional area of the heat flow or both [29].

Fig. 3(c) and (d) show the calculated structure function of the packaged  $\text{Ga}_2\text{O}_3$  SBD in the bottom- and junction-side-cooling schemes, respectively, each scheme with two TIMs. The separation points show good consistency with those extracted from  $Z \sim t$  curves. The function before the separation point provides the structure information within the package case.

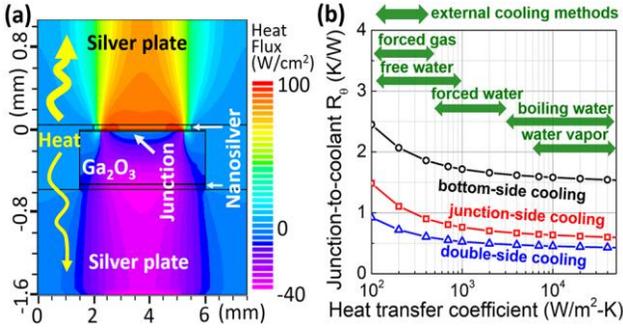


Fig. 4. (a) Simulated heat flux contours in the  $\text{Ga}_2\text{O}_3$  SBD cross-section under the double-side cooling. The positive and negative values represent the upwards and downwards flux, respectively. The bottom and top case temperatures are set as  $26^\circ\text{C}$  (i.e.,  $\text{HTC} = \infty$ ). (b) Simulated junction-to-coolant thermal resistance of the  $\text{Ga}_2\text{O}_3$  SBD as a function of HTC at the case surface, under the bottom-, junction- and double-side cooling. The HTC ranges for different external cooling techniques are marked in green.

The key difference between the junction- and bottom-cooling functions is that the former shows an almost constant slope before the separation point while the latter shows two regions with different slopes. The slope in the junction-cooling function corresponds to the nano-Ag attach and Ag plate (Fig. 3(c)). The almost constant slope suggests little heat up into the  $\text{Ga}_2\text{O}_3$  chip. The first slope in the bottom-cooling function corresponds to the  $\text{Ga}_2\text{O}_3$  chip (Fig. 3(d)), as its span ( $\sim 0.8$  K/W) is close to the calculated  $R_\theta$  using the  $\text{Ga}_2\text{O}_3$   $k_T$  and chip geometries ( $R_\theta = 0.5\text{-mm}/0.25\text{-Wcm}^{-1}\text{K}^{-1}/22\text{-mm}^2 = 0.9\text{-K/W}$ ). The second slope corresponds to the bottom attach and Ag plate. Its  $R$  and  $C$  spans ( $\sim 0.5$  K/W and  $\sim 0.1$  Ws/K) before the separation point are similar to the counterparts in the junction-cooling function.

Based on the measured  $R_{\theta\text{JC}}$ , 3-D TCAD simulations were performed in Silvaco Atlas to evaluate the device  $R_\theta$  in various external cooling conditions. The electrothermal models were similar to [33], and the material models (e.g.,  $k_T$  of  $\text{Ga}_2\text{O}_3$  and nanosilver, interface  $R_\theta$ ) were based on [25]. A copper plate with a geometry similar to the experimental setup was added to the package surface where the external cooling is applied. The simulated  $R_{\theta\text{JC}}$  and I-V characteristics were calibrated with the experimental data. The calibration revealed that the  $k_T$  of sintered nanosilver is  $\sim 1$   $\text{Wcm}^{-1}\text{K}^{-1}$  [25], suggesting the room for further improvement of the sintering process.

Fig. 4(a) shows the simulated heat flux contours in a double-side-cooled SBD with  $26^\circ\text{C}$  fixed on both package surfaces [i.e., infinite heat transfer coefficient (HTC)]. Most heat flows via the junction side of the package, agreeing with the expectation from the much lower junction-cooled  $R_{\theta\text{JC}}$ .

Fig. 4(b) shows the simulated junction-to-coolant (-ambient)  $R_\theta$  as a function of HTC (representing different cooling methods) for our  $\text{Ga}_2\text{O}_3$  SBD in the bottom-, junction- and double-side cooling schemes. The results suggest that the junction-cooling is essential for  $\text{Ga}_2\text{O}_3$  devices and the double-side-cooling can further reduce  $R_\theta$  by 30~40%. An HTC over  $10^3$   $\text{W/m}^2\text{K}$  (e.g., forced water cooling) is preferable for external cooling; a lower HTC may lead to a fast increase in  $R_\theta$  for  $\text{Ga}_2\text{O}_3$  devices.

Table I benchmarks the  $R_{\theta\text{JC}}$  of our  $\text{Ga}_2\text{O}_3$  SBDs against commercial 600-V SiC SBDs with a similar current rating and different TO-series packages (the dominant packages for commercial power devices), as well as a small-area unpackaged

TABLE I. Thermal resistance comparison between  $\text{Ga}_2\text{O}_3$  SBDs and commercial SiC SBDs with similar current ratings and package sizes.

Device	Package	Package Size* (mm <sup>2</sup> )	$V_{\text{ON}}$ (V)	$I_{\text{F}}$ (A)** @ 2 V	Cooling	$R_{\theta\text{JC}}$ (K/W)
$\text{Ga}_2\text{O}_3$ SBD (this work)	Double-side	7.3×7.3	0.83	13	Junction Bottom	0.5 1.43
SiC SBD (C3D10060G)	TO-263-2	6.5×7.9	0.85	18	Bottom	1.2
SiC SBD (E3D08065G)	TO-263-2	6.5×7.9	0.85	14.5	Bottom	1.47
SiC SBD (C6D04065E)	TO-252-2	5.2×4.3	0.85	12	Bottom	2.89
$\text{Ga}_2\text{O}_3$ SBD [14]	no package		$\sim 1$	$\sim 0.02$	Bottom	$\sim 4.5$

\*Size of the die-attached thermal pad. \*\*Forward current at 2 V.

$\text{Ga}_2\text{O}_3$  SBD reported previously [14]. The  $R_{\theta\text{JC}}$  of our junction-side cooled  $\text{Ga}_2\text{O}_3$  SBD is lower than that of commercial SiC SBDs with a similar package size and current rating. As a more direct comparison, if TO-263-2 package is used for our  $\text{Ga}_2\text{O}_3$  SBDs,  $R_{\theta\text{JC}}$  is estimated to be 0.61 and 1.54 K/W for the anode facing up and down, respectively. This estimation assumes the use of solder alloy as die attach with a thickness of 150- $\mu\text{m}$  and  $k_T$  of  $0.23$   $\text{Wcm}^{-1}\text{K}^{-1}$  instead of Ag sintering.

#### IV. SUMMARY

This work presents the first  $R_{\theta\text{JC}}$  data of large-area, packaged  $\text{Ga}_2\text{O}_3$  devices measured following the JEDEC standard. The packaged  $\text{Ga}_2\text{O}_3$  SBD shows over 15 A current and 600 V  $BV$ . The  $R_{\theta\text{JC}}$  under the junction-side- and bottom-side-cooling is 0.5 W/K and 1.43 W/K, respectively. The difference is primarily attributable to the low- $k_T$   $\text{Ga}_2\text{O}_3$  chip. The  $R_{\theta\text{JC}}$  of our  $\text{Ga}_2\text{O}_3$  SBD under the junction cooling is lower than  $R_{\theta\text{JC}}$  of similarly-rated commercial SiC SBDs, suggesting the feasibility of using the proper packaging to overcome the low  $k_T$  of  $\text{Ga}_2\text{O}_3$  and thereby enable  $\text{Ga}_2\text{O}_3$  devices for high-power applications.

#### REFERENCES

- [1] S. J. Pearton, J. Yang, P. H. Cary, F. Ren, J. Kim, M. J. Tadjer, and M. A. Mastro, "A review of  $\text{Ga}_2\text{O}_3$  materials, processing, and devices," *Appl. Phys. Rev.*, vol. 5, no. 1, p. 011301, Jan. 2018, doi: 10.1063/1.5006941.
- [2] M. Higashiwaki and G. H. Jessen, "Guest Editorial: The dawn of gallium oxide microelectronics," *Appl. Phys. Lett.*, vol. 112, no. 6, p. 060401, Feb. 2018, doi: 10.1063/1.5017845.
- [3] J. Y. Tsao, S. Chowdhury, M. A. Hollis, D. Jena, N. M. Johnson, K. A. Jones, R. J. Kaplar, S. Rajan, C. G. V. de Walle, E. Bellotti, C. L. Chua, R. Collazo, M. E. Coltrin, J. A. Cooper, K. R. Evans, S. Graham, T. A. Grotjohn, E. R. Heller, M. Higashiwaki, M. S. Islam, P. W. Juodawlkis, M. A. Khan, A. D. Koehler, J. H. Leach, U. K. Mishra, R. J. Nemanich, R. C. N. Pilawa-Podgurski, J. B. Shealy, Z. Sitar, M. J. Tadjer, A. F. Witulski, M. Wraback, and J. A. Simmons, "Ultrawide-Bandgap Semiconductors: Research Opportunities and Challenges," *Adv. Electron. Mater.*, vol. 4, no. 1, p. 1600501, 2018, doi: 10.1002/aelm.201600501.
- [4] Y. Zhang and T. Palacios, "(Ultra)Wide-Bandgap Vertical Power FinFETs," *IEEE Trans. Electron Devices*, vol. 67, no. 10, pp. 3960–3971, Oct. 2020, doi: 10.1109/TED.2020.3002880.
- [5] W. Li, K. Nomoto, Z. Hu, T. Nakamura, D. Jena, and H. G. Xing, "Single and multi-fin normally-off  $\text{Ga}_2\text{O}_3$  vertical transistors with a breakdown voltage over 2.6 kV," in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, p. 12.4.1-12.4.4, doi: 10.1109/IEDM19573.2019.8993526.
- [6] P. Paret, G. Moreno, B. Kekelja, R. Kotecha, X. Feng, K. Bennion, B. Mather, A. Zakutayev, S. Narumanchi, S. Graham, and S. Kim, "Thermal and Thermomechanical Modeling to Design a Gallium Oxide Power Electronics Package," in *2018 IEEE 6th Workshop on Wide*

- Bandgap Power Devices and Applications (WiPDA)*, Oct. 2018, pp. 287–294, doi: 10.1109/WiPDA.2018.8569139.
- [7] B. K. Mahajan, Y.-P. Chen, J. Noh, P. D. Ye, and M. A. Alam, “Electrothermal performance limit of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> field-effect transistors,” *Appl. Phys. Lett.*, vol. 115, no. 17, p. 173508, Oct. 2019, doi: 10.1063/1.5116828.
- [8] C. Yuan, Y. Zhang, R. Montgomery, S. Kim, J. Shi, A. Mauze, T. Itoh, J. S. Speck, and S. Graham, “Modeling and analysis for thermal management in gallium oxide field-effect transistors,” *J. Appl. Phys.*, vol. 127, no. 15, p. 154502, Apr. 2020, doi: 10.1063/1.5141332.
- [9] B. Chatterjee, K. Zeng, C. D. Nordquist, U. Singiseti, and S. Choi, “Device-Level Thermal Management of Gallium Oxide Field-Effect Transistors,” *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 9, no. 12, pp. 2352–2365, Dec. 2019, doi: 10.1109/TCPMT.2019.2923356.
- [10] R. Sharma, E. Patrick, M. E. Law, J. Yang, F. Ren, and S. J. Pearton, “Thermal Simulations of High Current  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky Rectifiers,” *ECS J. Solid State Sci. Technol.*, vol. 8, no. 7, pp. Q3195–Q3201, Jan. 2019, doi: 10.1149/2.0361907jss.
- [11] C. Buttay, H.-Y. Wong, B. Wang, M. Xiao, C. Dimarino, and Y. Zhang, “Surge current capability of ultra-wide-bandgap Ga<sub>2</sub>O<sub>3</sub> Schottky diodes,” *Microelectron. Reliab.*, vol. 114, p. 113743, Nov. 2020, doi: 10.1016/j.microrel.2020.113743.
- [12] N. A. Blumenschein, N. A. Moser, E. R. Heller, N. C. Miller, A. J. Green, A. Popp, A. Crespo, K. Leedy, M. Lindquist, T. Moule, S. Dalcanale, E. Mercado, M. Singh, J. W. Pomeroy, M. Kuball, G. Wagner, T. Paskova, J. F. Muth, K. D. Chabak, and G. H. Jessen, “Self-Heating Characterization of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Thin-Channel MOSFETs by Pulsed  $I-V$  and Raman Nanothermography,” *IEEE Trans. Electron Devices*, vol. 67, no. 1, pp. 204–211, Jan. 2020, doi: 10.1109/TED.2019.2951502.
- [13] J. W. Pomeroy, C. Middleton, M. Singh, S. Dalcanale, M. J. Uren, M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki, and M. Kuball, “Raman Thermography of Peak Channel Temperature in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFETs,” *IEEE Electron Device Lett.*, vol. 40, no. 2, pp. 189–192, Feb. 2019, doi: 10.1109/LED.2018.2887278.
- [14] B. Chatterjee, A. Jayawardena, E. Heller, D. W. Snyder, S. Dhar, and S. Choi, “Thermal characterization of gallium oxide Schottky barrier diodes,” *Rev. Sci. Instrum.*, vol. 89, no. 11, p. 114903, Nov. 2018, doi: 10.1063/1.5053621.
- [15] M. H. Wong, Y. Morikawa, K. Sasaki, A. Kuramata, S. Yamakoshi, and M. Higashiwaki, “Characterization of channel temperature in Ga<sub>2</sub>O<sub>3</sub> metal-oxide-semiconductor field-effect transistors by electrical measurements and thermal modeling,” *Appl. Phys. Lett.*, vol. 109, no. 19, p. 193503, Nov. 2016, doi: 10.1063/1.4966999.
- [16] W. Xu, Y. Wang, T. You, X. Ou, G. Han, H. Hu, S. Zhang, F. Mu, T. Suga, Y. Zhang, Y. Hao, and X. Wang, “First Demonstration of Wafer-scale Heterogeneous Integration of Ga<sub>2</sub>O<sub>3</sub> MOSFETs on SiC and Si Substrates by Ion-Cutting Process,” in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, p. 12.5.1-12.5.4, doi: 10.1109/IEDM19573.2019.8993501.
- [17] Z. Cheng, V. D. Wheeler, T. Bai, J. Shi, M. J. Tadjer, T. Feygelson, K. D. Hobart, M. S. Goorsky, and S. Graham, “Integration of polycrystalline Ga<sub>2</sub>O<sub>3</sub> on diamond for thermal management,” *Appl. Phys. Lett.*, vol. 116, no. 6, p. 062105, Feb. 2020, doi: 10.1063/1.5125637.
- [18] Y. Zhang and K. J. Chen, “Overcoming the limitations of gallium oxide through heterogeneous integration,” *Sci. China Phys. Mech. Astron.*, vol. 64, no. 1, p. 217331, Aug. 2020, doi: 10.1007/s11433-020-1596-5.
- [19] Y. Wang, W. Xu, G. Han, T. You, F. Mu, H. Hu, Y. Liu, X. Zhang, H. Huang, T. Suga, X. Ou, X. Ma, and Y. Hao, “Temperature-dependent characteristics of Schottky barrier diode on heterogeneous  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> (201)-Al<sub>2</sub>O<sub>3</sub>-Si Substrate,” *J. Phys. Appl. Phys.*, vol. 54, no. 3, p. 034004, Oct. 2020, doi: 10.1088/1361-6463/abbeb2.
- [20] Y. Wang, W. Xu, T. You, F. Mu, H. Hu, Y. Liu, H. Huang, T. Suga, G. Han, and X. Ou, “ $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFETs on the Si substrate fabricated by the ion-cutting process,” *Sci. CHINA Phys. Mech. Astron.*, vol. 63, pp. 1–4, 2020.
- [21] Y.-T. Yu, X.-Q. Xiang, X.-Z. Zhou, K. Zhou, G.-W. Xu, X.-L. Zhao, and S.-B. Long, “Device Topological Thermal Management of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> Schottky Barrier Diodes,” *Chin. Phys. B*, accepted, 2021, doi: 10.1088/1674-1056/abee2.
- [22] “TRANSIENT DUAL INTERFACE TEST METHOD FOR THE MEASUREMENT OF THE THERMAL RESISTANCE JUNCTION-TO-CASE OF SEMICONDUCTOR DEVICES WITH HEAT FLOW THROUGH A SINGLE PATH | JEDEC.” <https://www.jedec.org/standards-documents/docs/jesd51-14-0> (accessed Apr. 10, 2021).
- [23] N. Allen, M. Xiao, X. Yan, K. Sasaki, M. J. Tadjer, J. Ma, R. Zhang, H. Wang, and Y. Zhang, “Vertical Ga<sub>2</sub>O<sub>3</sub> Schottky Barrier Diodes With Small-Angle Beveled Field Plates: A Baliga’s Figure-of-Merit of 0.6 GW/cm<sup>2</sup>,” *IEEE Electron Device Lett.*, vol. 40, no. 9, pp. 1399–1402, Sep. 2019, doi: 10.1109/LED.2019.2931697.
- [24] B. Wang, M. Xiao, X. Yan, H. Y. Wong, J. Ma, K. Sasaki, H. Wang, and Y. Zhang, “High-voltage vertical Ga<sub>2</sub>O<sub>3</sub> power rectifiers operational at high temperatures up to 600 K,” *Appl. Phys. Lett.*, vol. 115, no. 26, p. 263503, Dec. 2019, doi: 10.1063/1.5132818.
- [25] M. Xiao, B. Wang, J. Liu, R. Zhang, Z. Zhang, C. Ding, S. Lu, K. Sasaki, G.-Q. Lu, C. Buttay, and Y. Zhang, “Packaged Ga<sub>2</sub>O<sub>3</sub> Schottky Rectifiers With Over 60-A Surge Current Capability,” *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 8565–8569, Aug. 2021, doi: 10.1109/TPEL.2021.3049966.
- [26] J. N. Calata, T. G. Lei, and G.-Q. Lu, “Sintered nanosilver paste for high-temperature power semiconductor device attachment,” *Int. J. Mater. Prod. Technol.*, vol. 34, no. 1–2, pp. 95–110, Jan. 2009, doi: 10.1504/IJMPT.2009.022406.
- [27] E. Deng, W. Chen, P. Heimler, and J. Lutz, “Temperature Influence on the Accuracy of the Transient Dual Interface Method for the Junction-to-Case Thermal Resistance Measurement,” *IEEE Trans. POWER Electron.*, vol. 36, no. 7, p. 10, 2021.
- [28] V. Székely and T. Van Bien, “Fine structure of heat flow path in semiconductor devices: A measurement and identification method,” *Solid-State Electron.*, vol. 31, no. 9, pp. 1363–1368, Sep. 1988, doi: 10.1016/0038-1101(88)90099-8.
- [29] M. R. Rencz, “Measuring partial thermal resistances in a heat-flow path,” *IEEE Trans. Compon. Packag. Technol.*, vol. 25, no. 4, p. 7, 2002.
- [30] J. K. Kim, “Thermal simulation and measurement of SiC MOSFETs,” in *2019 IEEE 21st Electronics Packaging Technology Conference (EPTC)*, Dec. 2019, pp. 331–335, doi: 10.1109/EPTC47984.2019.9026682.
- [31] Y. Zhai, F. Liang, C. Guo, and Y. Liu, “Transient dual interface measurement of junction-to-case thermal resistance in AlGaIn/GaN HEMT utilizing an improved infrared microscope,” *Microelectron. Reliab.*, p. 6, 2016.
- [32] Y. Avenas, L. Dupont, and Z. Khatir, “Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters—A Review,” *IEEE Trans. POWER Electron.*, vol. 27, no. 6, p. 12, 2012.
- [33] Y. Zhang, M. Sun, Z. Liu, D. Piedra, H. S. Lee, F. Gao, T. Fujishima, and T. Palacios, “Electrothermal Simulation and Thermal Performance Study of GaN Vertical and Lateral Power Transistors,” *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2224–2230, Jul. 2013, doi: 10.1109/TED.2013.2261072.