Superconducting V_3Si for quantum circuit applications

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V_3Si thin films are known to be superconducting with transition temperatures up to 15 K, depending on the annealing temperature and the properties of the substrate beneath. Here we investigate the film structural properties in the prospect of further integration in silicon technology for quantum circuits. Two challenges have been identified: (i) the large difference in thermal expansion rate between V_3Si and the Si substrate leads to large thermal strains after thermal processing, and (ii) the undesired silicide phase VSi_2 forms when V_3Si is deposited on silicon. The first of these is studied by depositing layers of 200 nm V_3Si on wafers of oxidized silicon and sapphire, neither of which react with the silicide. These samples are then heated and cooled between room temperature and 860 °C, during which in-situ XRD measurements are performed. Analysis reveals a highly non-linear stress development during heating with contributions from crystallization and subsequent grain growth, as well as the thermal expansion mismatch between silicide and substrate, while the film behaves thermo-elastically during cooling. The second challenge is explored by depositing films of 20, 50, 100 and 200 nm of V_3Si on bulk silicon. For each thickness, six samples are prepared, which are then annealed at temperatures between 500 and 750 °C, followed by measurements of their resistivity, residual resistance ratio and superconducting critical temperature. A process window is identified for silicide thicknesses of at least 100 nm, within which a trade-off needs to be made between the quality of the V_3Si film and its consumption by the formation of VSi_2.

I. INTRODUCTION

Quantum technologies based on solid state matter are now spreading from academic laboratories to the most advanced semiconductor foundries[1,2]. Among the materials to be integrated, superconducting thin films are of major interest as they are part of many quantum architectures. For instance, such films can be used to manipulate, read and couple superconducting or spin qubits with the use of superconducting resonators[3,4], and are also developed for non-dissipative interconnections or can even be part of the quantum device itself when integrated as source and drain contacts of CMOS transistors. Since silicon very-large scale integration (VLSI) is by far the most advanced nanofabrication technology, it is advantageous to identify superconducting materials that are fully compatible with such an environment. Among those, silicides appears as the most suitable materials[5,6], and as V_3Si has the highest known critical temperature of any silicide known so far[7,8], it is a prime candidate for these applications. In working towards its integration, two key problems have been identified: (i) a reduction in the superconducting critical temperature due to increased thermal strain after annealing[9], and (ii) the formation of the non-superconducting phase VSi_2 at the interface with a silicon channel or substrate.

In systems where reservoirs of both Si and V are available, the undesired phase VSi_2 is expected to form, which is both the first phase to nucleate[10] and is thermodynamically favored[11]. This rules out the self-aligned silicide (SALICIDE) process for the formation of the desired V_3Si, in which pure metal is deposited on exposed silicon contacts. Instead, it has motivated the adoption of V_3Si sputtering from compound targets[12,13]. In this approach, an annealing step is required after deposition to trigger the crystallization. This thermal processing leads to the buildup of strain in the final silicide film, which is known to negatively affect its critical temperature[14–19]. Earlier work has shown that this strain depends strongly on the mismatch in thermal expansion coefficient (TEC) between the silicide and the substrate, and can lead to a suppression in superconducting critical temperature T_c by 2 K on silicon[9]. Section II provides a detailed analysis of the impact of crystallization, grain growth and thermal expansion mismatch on the strongly temperature-dependent development of stress in V_3Si thin films.

Besides causing the buildup of large tensile stresses, thermal processing of V_3Si on silicon substrates also leads to the formation of VSi_2. The presence of VSi_2 at the interface between the superconducting V_3Si and the Si substrate may not be a problem per se. It is imperative, however, that a layer of V_3Si with a thickness on the order of its superconducting coherence length remains. The simultaneous formation of the two silicide phases after the deposition of amorphous V_3Si on bulk silicon wafers is discussed in section III. We find that when 50 nm or less of V_3Si is deposited, no superconductivity is observed after crystallization annealing. For layers of 100 or 200 nm, the superconducting critical temperature of the film is found to initially improve with annealing temperature, until at some point superconductivity disappears when all V_3Si is consumed by a growing layer of VSi_2.

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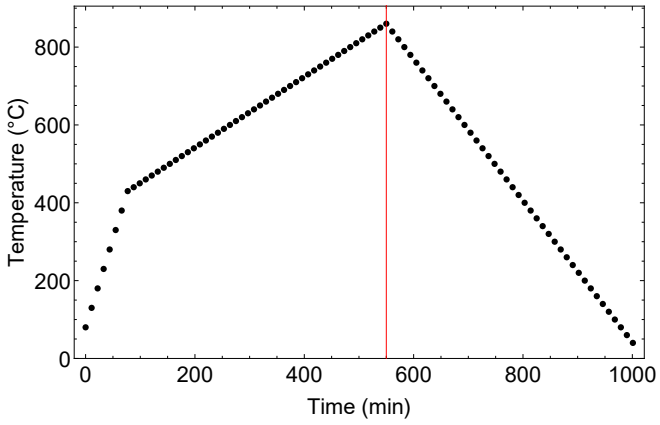

FIG. 1: Temperature profile versus annealing time applied during the in-situ XRD experiments. The red line in this and the following graphs in this section indicates the maximum temperature reached, after which cooling starts.

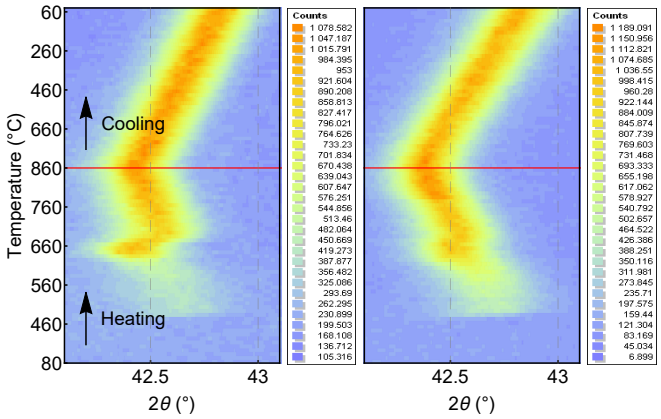

FIG. 2: In-situ out-of-plane XRD patterns measured during the V_3Si crystallization on **(Left)** a sapphire substrate and **(Right)** a silicon substrate.

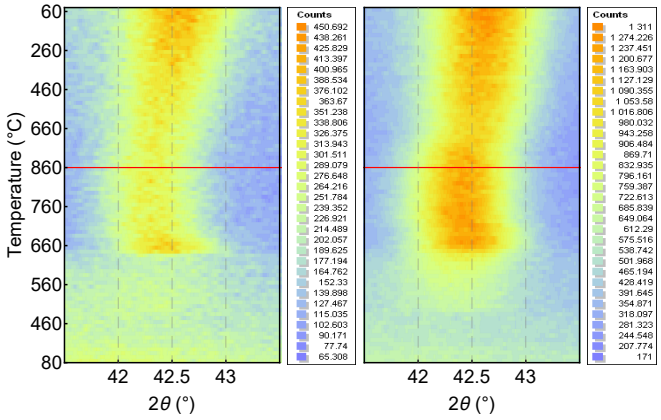

FIG. 3: In-situ in-plane XRD patterns measured during the V_3Si crystallization on **(LEFT)** a sapphire substrate and **(RIGHT)** a silicon substrate.

II. IN-SITU XRD ANALYSIS

Sputtering a V_3Si target leads to the deposition of an amorphous layer of the desired intermetallic compound which presents superconductivity at temperatures of around 1 K, far below that of the crystalline form (measured but not shown). In order to nucleate the crystalline V_3Si phase, heat has to be applied. In the present section, the V_3Si was isolated from any potential element (V and Si especially) that would affect the crystallization phenomenon. Thus, depositing the intermetallic compound on oxides (silica and sapphire) offers the possibility to study the isolated film by itself, affected by the substrate only mechanically. The evolution of the stresses in the V_3Si film as a function of the annealing temperature is monitored by in-situ X-ray diffraction (XRD) using a Smartlab Rigaku X-ray diffractometer equipped with a copper (Cu K_α) source, a punctual detector and a DHS 1100 Anton Paar furnace using a nitrogen atmosphere at a pressure slightly above ambient, i.e. 1.25 bar, to avoid atmospheric contamination.

Layers of 200 nm V_3Si were deposited on two types of substrates: oxidized silicon with a 20 nm thick surface oxide, and sapphire. Both in-plane and out-of-plane XRD measurements were performed on different samples of each substrate. For both measurements, a parallel slit analyzer with an angular aperture of 0.114 ° for out-of-plane measurement and 1 ° for in-plane ones, is positioned in front of the detector in order to be insensitive to peak shift due to the radial displacement of the sample induced by thermal expansion of the sample holder. This way, the observed peak shift is only related to a real d-spacing variation. For both measurements, 2θ–ω scans around the V_3Si (210) close to $2\theta = 43$ ° were performed. Profiles were acquired while heating the samples from 50 °C up to 860 °C and then during cooling from 860 °C to room temperature. The temperature profile versus time is given in Fig. 1.

Peak fitting was performed with the HighScore Plus software from PANalytical. From those fittings, the d-spacing of the V_3Si (210) peak and the integral breadth of the peak were considered. The V_3Si crystallization followed by in-situ XRD is shown as a contour map for the out-of-plane measurements in Fig. 2 and the in-plane measurements in Fig. 3.

During heating, for both substrates, a characteristic peak of (210) V_3Si is observed above 500 °C, which marks the crystallization temperature of the as-deposited amorphous V_3Si layer. Thus, one can deduce that the nucleation temperature of V_3Si crystalline phase is close to 500 °C. From in-plane and out-of-plane peak positions, one can extract the stress and the temperature-dependent stress-free lattice parameter of the layer. Assuming a bi-axial state of stress in the layer, it can be deduced following the $\sin^2\psi$ methodology[20],

$$\varepsilon_\psi = \frac{(d_\psi - d_0)}{d_0} = \frac{1}{2}S_2(hkl)\sigma\sin^2\psi + 2S_1(hkl)\sigma, \qquad (1)$$

where σ is the in-plane bi-axial state of stress, ε_ψ and d_ψ are the strain and the d-spacing along the direction ψ, respectively, d_0 is the stress-free d-spacing and ψ is the angle between the considered direction and the normal to the surface. $\frac{1}{2}S_2(hkl)$ and $S_1(hkl)$ are the X-ray Elastic Constants (XEC) for the hkl plane considered. The XEC can be easily

calculated[21] by knowing the single-crystal elastic constants of the V_3Si structure[22]. For the (210) plane, using the arithmetic average of the Voigt and Reuss XEC, known as the Neerfeld limit, we found $\frac{1}{2}S_2(210) = 6.69\times10^{-6}\,\mathrm{MPa}^{-1}$ and $S_1(210) = -1.66\times10^{-6}\,\mathrm{MPa}^{-1}$. The in-plane stress is then given by[20]

$$\sigma = \frac{2}{S_2(hkl)}\left(\frac{d_\parallel - d_\perp}{d_0}\right), \qquad (2)$$

and the stress-free d-spacing, d_0, by

$$d_0 = \frac{d_\perp - A d_\parallel}{1-A}, \quad \text{where} \quad A = \frac{4S_1(hkl)}{S_2(hkl)+4S_1(hkl)}. \qquad (3)$$

In Fig. 4a, the stress evolution deduced from this analysis is plotted versus the annealing temperature for both types of substrate. In both cases, the initial stress at crystallization is highly tensile (around +1500 MPa). This is in agreement with the expected volume shrinkage occurring during the crystallization, assuming that the density of the amorphous phase is smaller than the density of the crystalline phase. This tensile stress is then partially relaxed.

In Fig. 4c,d the integral breadth (IB) evolution of the (210) peak vs annealing temperature is plotted, which can be correlated to the crystallite size through the Scherrer equation[23,24]. This figure shows that the IB is high at the crystallization temperature and then goes down with increasing temperature, a behavior that is similar for the in-plane and out-of-plane directions, and can be interpreted as a crystallite size increase. However, one should note that the in-plane and and out-of-plane setup was different and can not be compared directly.

Indeed, for the in-plane setup, the IB decreased down to 1° at 650°C and it kept constant during further annealing This value of 1° is the instrumental width given by a silicon reference powder, which implies that the in-plane crystallite size is very large above 650°C and can no longer be estimated from IB broadening. As we observe an increase of the crystallite size out of plane up to 860°C, we may assume that the lateral crystallite size also continues to grow up to this temperature. In the case of the out-of-plane measurements, the setup was more accurate, and the estimated crystallite size is about 30 nm for the highest annealing temperature. It can clearly be concluded that there is a strong anisotropy in grain size on both substrates. On both substrates, the in-plane IB stabilizes at 650 °C due to saturation of the instrument resolution, while the detected out-of-plane crystallite size increases continuously to the maximum temperature of the experiment.

During cooling, the stress evolution exhibits a linear behavior, in agreement with a pure thermoelastic stress induced by the TEC mismatch between the film and the substrate. This is confirmed by looking at the in-plane lattice parameter evolution with temperature (Fig 4b). The behavior is linear as expected, but more interestingly, the slope of these straight lines is $7.3\times10^{-6}\,°\mathrm{C}^{-1}$ and $4.2\times10^{-6}\,°\mathrm{C}^{-1}$ for the sapphire and Si substrate respectively, in good agreement with the in-plane TEC of sapphire ($6.5\times10^{-6} < \alpha < 7.6\times10^{-6}\,°\mathrm{C}^{-1}$ in the temperature range 300–800 °C)[25], and with the TEC of Si ($3.6\times10^{-6} < \alpha < 4.3\times10^{-6}\,°\mathrm{C}^{-1}$ in the temperature

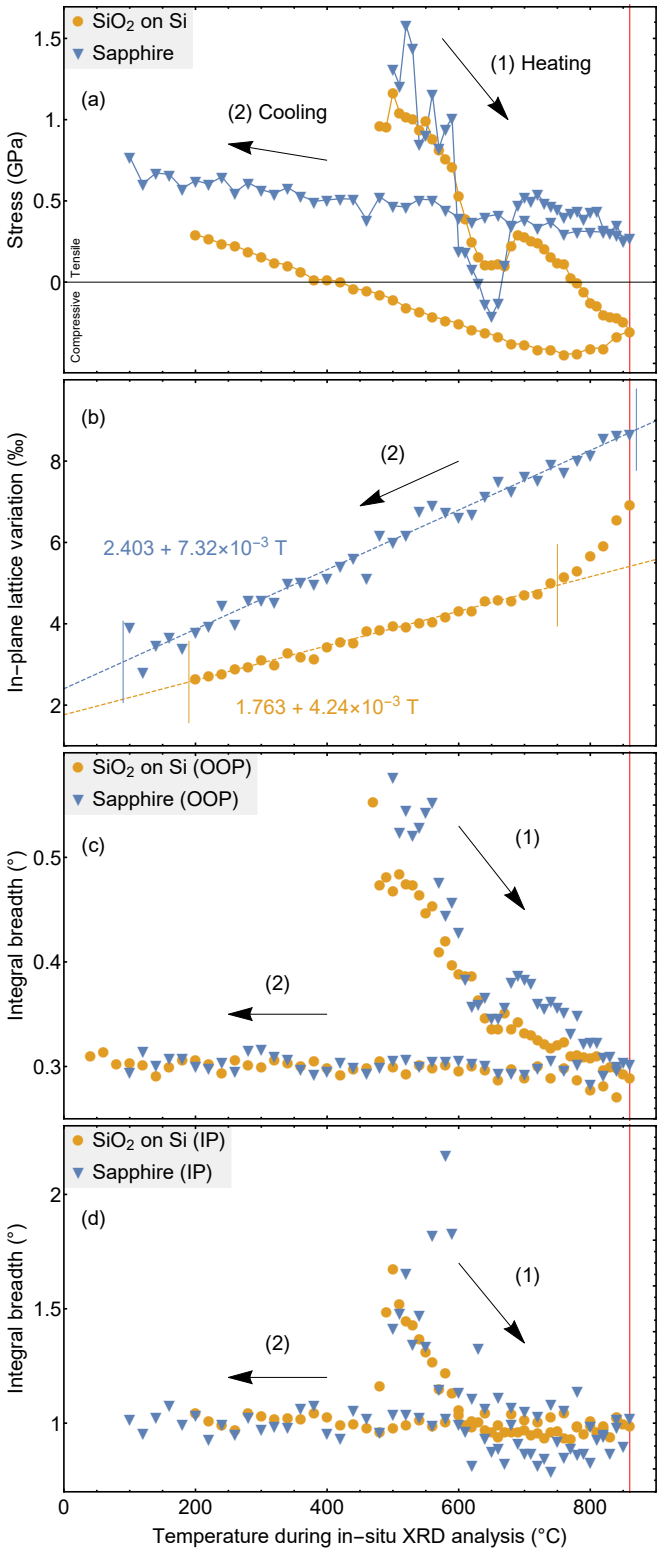

FIG. 4: **(a)** Stress evolution versus annealing temperature for both the sapphire and the silicon substrates. **(b)** Strain of the V_3Si layer versus the annealing temperature during cooling. **(c,d)** Out-of-plane and in-plane integral breadth of the V_3Si (210) peak versus annealing temperature.

range 200–800 °C)[26]. From the stress-free lattice parameter extraction, we calculated a TEC of the V_3Si phase of $9.2 \times 10^{-6}\,°C^{-1}$. The TEC mismatch between the film and the substrate should therefore have added a tensile stress to the stress measured at 860 °C, in agreement with the observation in Fig. 4a. As expected, since the TEC mismatch is larger with the Si substrate than with the sapphire, the tensile stress increase faster on Si than on sapphire. Extrapolating this thermoelastic behavior to the device operating temperature (i.e. a few K), a stress level of $0.87(7)$ GPa is obtained for V_3Si on sapphire and $0.91(3)$ GPa for V_3Si on silicon. Of course these values depend on the initial residual stress before cooling, and thus on the thermal budget applied to the samples. Since the slow cooling occurred entirely thermoelastically and followed the TEC of the substrate, it is not expected that the rate of cooling has any impact on the final stress obtained. The difference in room-temperature strain between this report and those found in earlier experiments where in-situ XRD analysis was performed up to 1000 °C[9] is thus attributed to differences in the maximum temperature that was reached.

III. COMPETITION BETWEEN V_3Si AND VSi_2 FORMATION

A second set of experiments was performed to study the stability of the superconducting V_3Si phase on a silicon substrate. After sputter deposition of V_3Si on a silicon substrate, an intermixing layer of Si and V can be expected to form where the atomic concentration of vanadium ranges from zero in the substrate to $3/4$ within the deposited layer. Above this mixed zone, the precise matching of the deposited atomic ratio to the stoichiometry of V_3Si will prevent the formation of VSi_2. Within the mixed zone however, VSi_2 nucleation is likely to occur. Since this mixed zone is interfaced from below by pure silicon, and from above by V_3Si, its disappearance or consumption by V_3Si formation would require that V move upwards while leaving progressively purified Si behind. Such movement is prevented by the chemical potential, as the thermodynamically stable state in the presence of excess silicon is for the vanadium to be bound in VSi_2[11]. Furthermore, even if a V reservoir were present in the form of a super-stoichiometric vanadium concentration (i.e. above 75%) in the deposited layer, it is unlikely that the mixed zone would be consumed by V_3Si formation. Since silicon is the dominant diffusing species in VSi_2 and at the V/Si interface, with diffusion rates of two orders of magnitude higher than that of V in V_3Si[27,28], any part of the intermixing layer with lower vanadium concentration than that of V_3Si is expected to quickly extend downward and decrease in V content due to upward Si diffusion, preventing V_3Si growth and aiding the formation of VSi_2.

Once VSi_2 and V_3Si are both present, competition will arise between the further growth of either silicide. While V_3Si ($V_{0.75}Si_{0.25}$) has a larger effective heat of formation (EHF) from pure V and Si per mole of atoms involved in total[11], the energy gain *per vanadium atom* is greater for VSi_2 ($V_{0.33}Si_{0.67}$), of which three times as many molecules can be

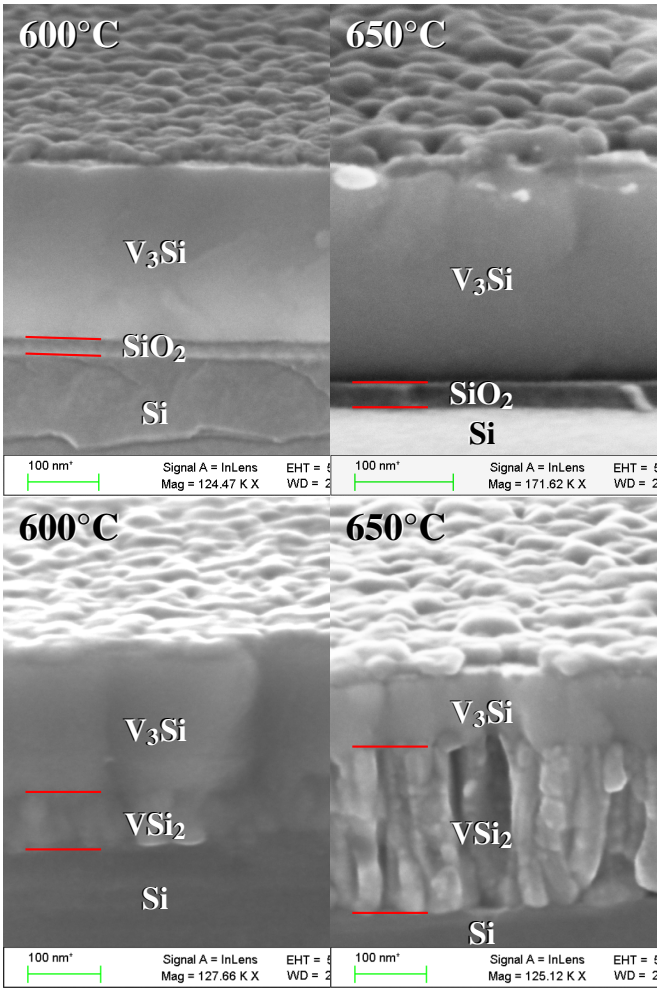

FIG. 5: **(Top)** A 200 nm layer of V_3Si is deposited on a silicon substrate with 20 nm of thermal oxide and is annealed at 600 °C (left) and 650 °C (right). No formation of VSi_2 observed. **(Bottom)** When an equal thickness of V_3Si is deposited on HF-cleaned silicon and annealed at 600 °C (left) and 650 °C (right), a VSi_2 layer with distinct morphology appears.

formed for a fixed amount of vanadium. When V_3Si interfaces with silicon, it is therefore energetically favorable for the following reaction to occur (EHF indicated below),

$$\underbrace{V_3Si}_{-45.2\,\mathrm{kJ/mol\ at}} + \underbrace{5Si}_{0} \rightarrow \underbrace{3VSi_2}_{-40.2\,\mathrm{kJ/mol\ at}}, \qquad (4)$$

where an energy of 181 kJ/mol is gained per mole of V_3Si that is transformed. Scanning electron microscope (SEM) images of the growth of the VSi_2 phase during thermal processing are shown in Fig. 5.

To study this interplay, a different set of samples was prepared in addition to those discussed in section II. Layers with thicknesses of 20, 50, 100 and 200 nm of V_3Si were deposited onto 200 mm (100)-oriented silicon wafers from a compound V_3Si target using RF magnetron sputtering equipment. This target had a measured silicon content of be-

tween 22.7 ± 0.2 at.% (WDXRF) and 25.7 ± 0.2 at.% (supplied data), which could further differ from the final Si content in the deposited layer by 1 at.%[13]. These wafers were cleaned with hydrofluoric acid (HF) before entering the sputtering chamber. Smaller pieces of $2 \times 2\,cm^2$ were then annealed during 2 minutes in a Jipelec furnace with a 20 °C/min ramp rate. For each thickness of V_3Si, six different samples were thermally processed at temperatures between 500 and 750 °C, as indicated in Fig. 6. These samples were then characterized by measuring their room-temperature sheet resistance (corrected for their shape and size by calculating the sheet resistance ratio of multiple unannealed wafer-sized and $2 \times 2\,cm^2$ samples), and by following the resistance of smaller samples during slow cooling to cryogenic temperatures of 2 K in order to extract both the superconducting critical temperature and the residual resistance ratio (RRR).

At 500 °C, the resistivity of the thinner layers (20, 50 and 100 nm) was found to be comparable to that of as-deposited amorphous V_3Si ($180(10)\,\mu\Omega\,cm$), while it exceeded this value by multiple orders of magnitude for the thicker layer of 200 nm (out of range for our instruments), as shown in Fig. 6a. For all thicknesses, the resistivity then decreased with annealing temperature, to values below that measured for a reference sample with 200 nm V_3Si on non-reacting sapphire annealed at 900 °C (77.1 μΩ cm, indicated as a red dashed line). Since this reference value is the lowest resistivity that we have found for any layer of crystallized V_3Si, in a sample where we confirmed by XRD measurements that no other vanadium-rich compound was formed, we take any value lower than this on silicon substrates to indicate the presence of VSi_2. The formation of VSi_2 was confirmed by XRD analysis and identified at the Si/V_3Si interface by SEM imaging (see Fig. 5, bottom).

Smaller samples of 4×10 mm were then wire bonded for four-point resistance measurements during both cooling and heating between 300 and 2 K in a Physical Properties Measurement System (PPMS). The residual resistance ratio of each sample was calculated as the ratio between the resistances at 260 K and 20 K, shown in Fig. 6b. This ratio gives insight into the material properties of the silicide layer since the resistance at low temperatures is dominated by impurity and defect scattering[29]. For higher annealing temperatures the RRR is greater for thicker layers (with the exception of the 200 nm sample annealed at 750 °C, which is also an outlier in terms of resistivity), which is consistent with the lower quality of thinner films as reported before[12]. After annealing at 550 °C, however, we find that the RRR is highest in samples where only 20 nm of V_3Si was deposited, followed by 50 nm and 100 nm, in that order. This could be an indication that a nearly homogeneous VSi_2 layer has already started to form at the V_3Si/Si interface in the thinnest of these films, with inhomogeneity increasing for thicker films of 50 and 100 nm. Complete homogenization of a 20 nm film during two minutes would suggest however that Si, the dominant diffusing species in VSi_2 formation[27], has diffused with a diffusivity of at least $1.8\,nm^2\,s^{-1}$, values that have only been reported for annealing temperatures of 650 °C[30]. The higher RRR at 550 °C of the sample with 200 nm deposited V_3Si suggests that this layer is too thick for diffusion to have already caused mixing throughout the entire

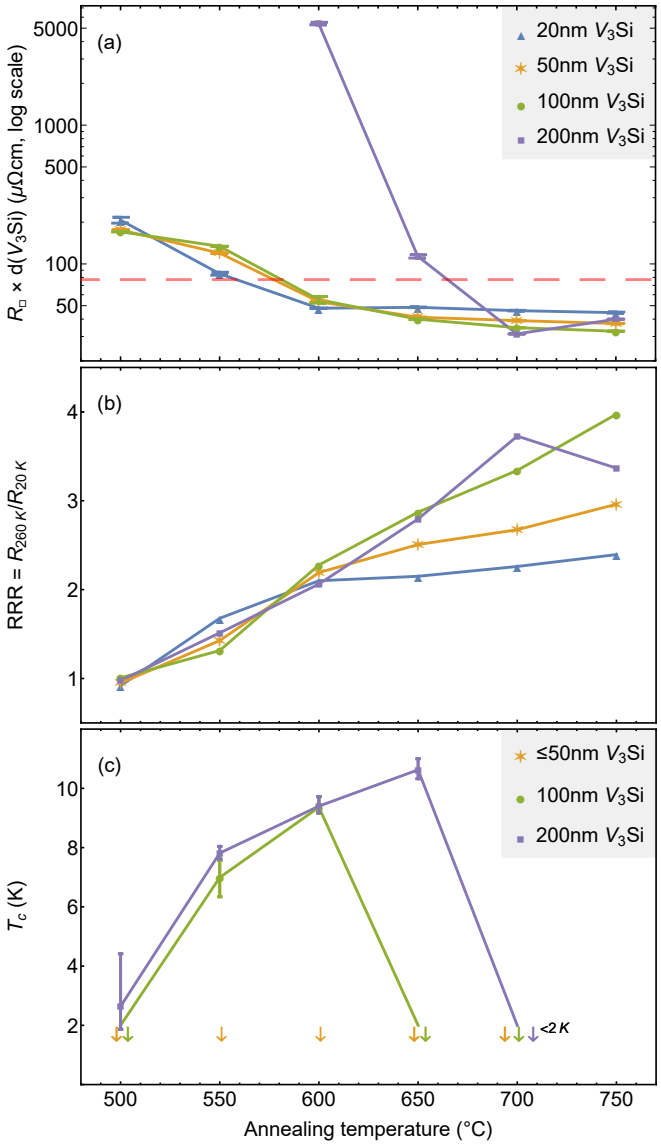

FIG. 6: **(a)** The resistivity of each annealed sample, red dashed line indicates the lowest resistivity expected for V_3Si (see main text). **(b)** The residual resistance ratio (RRR). **(c)** The critical temperature, taken to be the point where 50% of the normal resistance is lost, with error bars indicating temperatures at which 10% and 90% of normal-state resistance is observed. Arrows down (↓) indicate that the critical temperature (if any) is below 2 K.

film, and this relatively high value could be attributed to crystallization of V_3Si.

This appearance of crystalline V_3Si at temperatures of around 500 °C is consistent with the in-situ XRD analysis on non-reactive substrates discussed in section II (see especially Fig. 2). This is further corroborated by the appearance of superconductivity at temperatures above 2 K as shown in Fig. 6c, to be contrasted with the critical temperature of 0.9 K of amorphous 200 nm-thick V_3Si layers on silicon substrates prepared under identical conditions[9]. A critical temperature

of 10.62 K (10% and 90% transitions at 10.32 and 11.00 K, respectively) was attained after annealing at 650 °C in a 200 nm deposited film, identical to that obtained on samples where VSi_2 formation was prevented by a 20 nm film of SiO_2, with a superconducting transition that is only 12% wider[9]. This suggests that the nearby formation of VSi_2 does not have a significant impact on the superconducting properties of the remaining V_3Si. Meanwhile, the absence of superconductivity above 2 K in samples with 20 or 50 nm deposited V_3Si, after annealing at any temperature, confirms that Si diffusion and VSi_2 formation rapidly remove or even prevent crystallization of V_3Si altogether in thinner films.

IV. DISCUSSION

Instead of forming vanadium silicide by reactive diffusion, V_3Si was directly sputtered from a compound target at the right stoichiometry, giving the advantages of having a sharp interface between the deposited layer and the substrate, and requiring no solid-state reaction to reach the desired phase. However, the interface must be better controlled in terms of impurities, and the V_3Si is amorphous after deposition. First, the crystallization was studied on 2 types of substrate, oxidized silicon with a 20 nm thick SiO_2 surface layer and monocrystalline sapphire (Al_2O_3). It was clear no reaction occurred with either of these substrates at any temperature. Earlier work showed that the mismatch in TEC with the substrates strongly impacts the stress built up during the growth of V_3Si, which can lower the superconducting critical temperature[9].

Layer crystallization started at 500 °C, leading to high tensile stress on either substrate up to 650 °C. This stress then relaxed with increasing temperature, both due to atomic diffusion and the relatively low TEC of the substrates. From 650 °C to around 800 °C, an increase in tensile stress together with a decrease in the out-of-plane IB can be explained by grain growth in fair agreement with the model of P. Chaudari[31]. During cooling, the V_3Si stress behavior matches perfectly with TEC of silicon and sapphire substrate, indicating a purely thermoelastic behavior. It is thus clear that the thermomechanical properties of the substrate strongly impact the stress development in the V_3Si film, which can be mitigated by proper choice of annealing conditions.

Since V_3Si is amorphous after deposition, crystallization by subsequent thermal processing is required to achieve the desired superconducting properties. However, on a silicon substrate this has the undesired side effect of VSi_2 nucleation. In fact, in the thinnest films that were studied, with 20 and 50 nm of deposited silicide, a nearly homogeneous VSi_2 layer had already started to form at the interface with the substrate before any crystallization of V_3Si was observed by critical temperature measurements. The inhomogeneity of this interfacial layer increased with film thickness from 20 to 100 nm. Full consumption of the deposited V_3Si occurred at higher temperatures between 600–650 °C and 650–700 °C for layers of 100 and 200 nm, respectively, allowing for V_3Si crystallization, as well as grain growth. The critical temperatures thus obtained on a silicon substrate prior to complete V_3Si consumption are identical, within experimental error, to those obtained on SiO_2[9], indicating no detrimental effect of diminished thickness or proximity to growing VSi_2 on the quality of the superconductor. This is in contrast with earlier results obtained by V_3Si sputtering from a compound target on heated Si substrates with 800 nm of thermal SiO_2, where a strong dependence of film thickness was found below 200 nm[12]. This variation in thickness was at the time attributed to the presence of impurities such as oxygen, while earlier reports had argued that the chemical composition of the layer was unimportant, and any variations that it causes in T_c are due to a change in lattice parameter[14]. Since no reaction with the substrate occurs on SiO_2 (see Fig. 5), and the critical temperature is independent of the thickness of crystalline V_3Si itself, the reduced T_c reported in this earlier study[12] could also be attributed to differences in grain growth, or stress development during cooling from 560 °C, at which the layers were deposited, to cryogenic temperatures in the range of 10–15 K.

V. CONCLUSION

Superconducting thin films are of increasing interest as solid-state quantum technologies are scaled up. To facilitate large-scale fabrication, as well as co-integration with classical electronics, it is important that the choice of superconducting material is compatible with CMOS technology. This report addresses two challenges for the integration of V_3Si, which as a silicide with a superconducting critical temperature of up to 17 K[7,8] is a natural candidate for CMOS integration.

The first is the reduction in critical temperature due to thermal strain. While V_3Si is compatible with the oxides of silicon and aluminum, both currently used in VLSI devices, it is necessary to mitigate the stresses induced by the interplay between crystallization, grain growth and TEC mismatch with the substrate. It is found in this study that the final stress obtained on either substrate depends strongly on the thermal budget that the samples are subjected to, identifying annealing as a key process step to control the critical temperature of the film.

Second, thermal processing also provides a means of controlling the formation of the undesired phase VSi_2 on HF-cleaned silicon substrates. For V_3Si films thicker than 100 nm, there exists a process window where it can be crystallized before consumption by the VSi_2 phase, with a temperature range that depends on the thickness of the film.

Direct applications of V_3Si could be in high-frequency resonators on oxides or oxidized substrates, where the impact of a potential stress residual on the quality factor has to be evaluated. A further interest would be to fabricate Josephson junctions, where the weak link could either be an oxide in a vertical geometry, or silicon in a planar junction. In the latter case, a Josephson field effect transistor could be fabricated by forming V_3Si in the source and drain contacts of a CMOS transistor, in which case one is faced with a trade-off between improving the V_3Si critical temperature and limiting the growth of the VSi_2 phase.

VI. DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

VII. ACKNOWLEDGMENTS

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