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# mm-Wave Single-Pole Double-Throw switches: HBT- vs MOSFET-based designs

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**Abstract**— This paper aims to compare the performance of HBT-based and MOSFET-based mm-Wave SPDT switches in a single BiCMOS technology. To the best of authors' knowledge, a direct comparison of this function in the same integrated process has never been reported before. Measurement results on two 50-GHz integrated SPDTs reveal that the HBT-based SPDT switch yields 1.7 dB of insertion loss and 14 dB of isolation in its central frequency, with a bandwidth covering the 30-80 GHz frequency range when considering a return loss greater than 10 dB. On the other hand, the MOSFET-based SPDT switch yields 2.1 dB of insertion loss and 12 dB of isolation at center frequency and a bandwidth covering the 33-80 GHz frequency range.

**Keywords**— SPDT, BiCMOS, slow-wave, S-CPW, HBT, mm-Wave

## I. INTRODUCTION

The rapid increase in the demand of high-data-rate telecommunications has brought transceivers into the mm-Wave frequency band (i.e., 30-300 GHz). Indeed, in the recent years, the development of applications operating within this band has increased since greater frequencies lead to greater bandwidths and thus the desired increase in the data rate. For instance, current mobile telecommunications (i.e., 5G and beyond-5G), automotive, medical and security applications are found within this band.

The increase in the operating frequencies has been backed by major developments in the silicon-based technologies, such as high-performance (Bi)CMOS integrated technologies. For instance, in the recent years, these technologies are steadily moving their frequency-handling capabilities up to the sub-THz band, with transistors currently reporting  $f_T/f_{max}$  of around 500/600 GHz [1], [2]. Silicon-based technologies, as opposed to III-V technologies, offer mass production at a relatively low cost, miniaturized footprints and the possibility to integrate logic and signal analysis in the same die. Hence, they show very interesting attributes for many consumer applications.

In parallel, the successful development of mm-Wave consumer applications requires the design of state-of-the-art basic RF building blocks. One of the most widely used RF blocks is Single-Pole Double-Throw (SPDT) switch. This popular block is used to direct the signal from/to an antenna to/from the Rx/Tx path (i.e. antenna switch) [3], or more generally to control the signal flow within an RF chain, also it may be useful in Built-In Self-Test (BIST) applications [4].

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However, as for most devices, the increase in the working frequencies goes hand-to-hand with an increase in the design complexity. mm-Wave SPDTs also follow this trend, with low-frequency approaches including  $\pi$ - or  $T$ - equivalent lumped structures of transistors and high-frequency approaches that require the use of quarter-wavelength transmission lines (TLines).

These devices have generated extensive literature due to their interesting properties. In fact, thanks to the technological leaps achieved by semiconductor foundries in the recent years, SPDTs have been reported up to practically the end of the mm-Wave band (i.e., up to 285 GHz) in silicon-based technologies [5]. In addition, active competition in the literature can be observed between approaches reporting the use of Heterojunction Bipolar Transistors (HBT) [6], [7] and the use of MOSFETs [5], [8]–[11]. However, to the best of authors' knowledge, a thorough analysis of the literature reveals that a clear comparison between MOSFETs and HBTs for the fabrication of mm-Wave SPDTs in the same technology node has never been reported.

To provide a fair comparison, several conditions have to be met. First, the frequencies of operation of both SPDTs (i.e., the MOSFET-based and the HBT-based) are to be very similar. A transistor, as any other electronic device, presents a frequency-dependent behavior. In addition, similar specifications have to be defined for both switches. Finally, a simple architecture has to be privileged, in order to maximally reveal the advantages and disadvantages of the transistor choice. Based on these premises, this paper presents the implementation of two SPDT switches whose switching elements are implemented using either HBTs, or MOSFETs.

This paper is organized as follows. Section II presents the proposed architecture and the approaches taken for the design of the switches. In section III, the practical implementation of the switches is detailed together with the measurement setup and the obtained results, which are compared to the simulation-based datasets. Finally, section IV draws the main conclusions of this work.

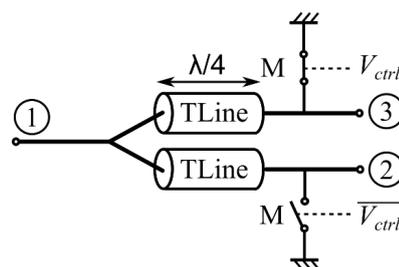


Fig. 1.  $\lambda/4$  TLine architecture for the implementation of mm-Wave SPDT switches.

## II. PROPOSED APPROACH

Even though different topologies exist, most of the reported mm-Wave switches revolve around the same architecture, which is conceptually depicted in Fig. 1. This architecture is composed of two quarter-wavelength TLines connected in between by a T-junction at one end and presenting a parallel switching transistor element at the other end. In their turn, the transistors, labelled  $M$  in the schematic view, are controlled through a voltage signal  $V_{ctrl}$ , which is alternately applied to each switch branch.

Ideally, the branch where the transistor is in a cut-off state (i.e. OFF-state) behaves as a TLine of characteristic impedance  $Z_C$ . On the other hand, at the port 1 side in Fig. 1, the branch presenting a short circuit (i.e. transistor in the linear region) behaves as an open circuit. This can be demonstrated by the fact that the impedance seen at the input,  $Z_{in}$ , of a short-circuited stub is equivalent to an open-circuit, when the electrical length of the stub,  $\theta$ , equals  $\pi/2$  rad, as shown in (1):

$$Z_{in} = jZ_C \cdot \tan(\theta) \quad (1)$$

where  $Z_C$  is the characteristic impedance of the TLine.

The simplicity of this architecture and the fact that the main performance limitation of this scheme is the performance of the transistor has made it a long-standing standard for mm-Wave switch design.

### A. Transmission line design

Even though, in this architecture, the transistor is the main contributor to the overall performance, the quarter-wavelength TLine still plays a non-negligible role. Hence, high-Quality-factor ( $Q$ -factor) TLines are necessary to improve the characteristics of the SPDT switch [7], [11]. Also, as the aim of this work is to analyze the trade-offs of using HBTs or MOSFETs of the same process flow, the impact of the TLines must be reduced to maximally reveal the effects of the transistor performance.

Hence, in this work Slow-wave CoPlanar Waveguides (S-CPWs) are considered for the integration of the quarter-wavelength TLines. This architecture was first introduced in [12] and subsequent distributed models [13] and associated model improvements were proposed [14]. A conceptual layout view of this architecture is shown in Fig. 2.

These TLines are composed of three coplanar strips, two lateral identical ground strips and a central signal strip, as in a classical CPW. However, as opposed to CPWs, electrically floating fingers (or ribbons) are placed in a transversal position relative to the propagation direction. The fingers capture the electric field while leaving the magnetic field almost unperturbed. This spatial dissociation of the electromagnetic field leads to the so-called slow-wave effect, which, in practical terms, corresponds to reducing the

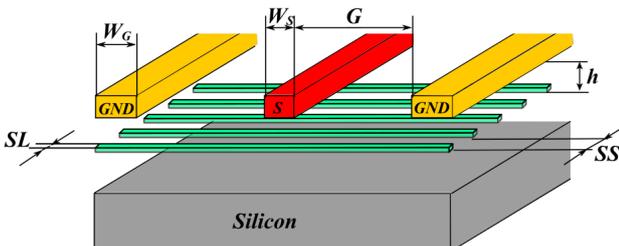


Fig. 2. Simplified view of the S-CPW architecture.

propagation velocity of the RF waves travelling across the structure, as compared to a structure without the fingers.

The concentration of the electric field between strips and fingers leads to an increase of the linear capacitance,  $C_{lin}$ , in the distributed model of the S-CPW, as compared to a CPW with the same lateral dimensions. On the other hand, as the magnetic field spatial distribution is maintained as compared to a CPW with the same lateral dimensions, the linear inductance of the S-CPW,  $L_{lin}$ , is maintained too. In this scenario, the phase velocity,  $v_\phi$ , of the S-CPW is lower than the CPW one with equal lateral dimensions, as shown by:

$$v_\phi = \frac{1}{\sqrt{L_{lin} \cdot C_{lin}}} \quad (2)$$

Thanks to the reduction of  $v_\phi$ , the necessary physical length,  $l$ , required to implement a given electrical length,  $\theta$ , at a specific frequency,  $f$ , is reduced as shown in the following expression:

$$\theta = \frac{\omega \cdot l}{v_\phi}, \quad (3)$$

where  $\omega$  represents the angular frequency (i.e.  $\omega = 2\pi f$ ). Additionally to the miniaturization effect, the reduction of the phase velocity can also lead to an increase of the  $Q$ -factor:

$$Q = \frac{\beta}{2 \cdot \alpha} = \frac{\omega}{2 \cdot v_\phi \cdot \alpha} \quad (4)$$

where  $\beta$  and  $\alpha$  are the phase and attenuation constants, respectively.  $\alpha$  is kept almost unchanged between CPW and S-CPW with similar lateral dimensions. As  $v_\phi$  reduces for S-CPW, the latter shows higher  $Q$ -factor than its CPW counterpart. For this reason, the S-CPW architecture is an interesting solution for the implementation of the  $\lambda/4$  TLines.

Finally, note that, as shown in Fig. 1, a T-Junction is present at port 1. This T-junction has a non-negligible impact on the overall performance of the structure. Indeed, these structures, as any other geometrical discontinuity, add parasitic effects and cannot be considered ideal in the mm-Wave range [15]. Hence, the effect of this section of the circuit must be carefully evaluated to achieve optimal performance.

### B. Transistor design

The switching element in Fig. 1 can be implemented using a variety of integrated devices. Thus, dedicated silicon-based technologies may offer switching solutions such as PIN diodes or Micro-Electro-Mechanical Systems (MEMS) to perform the switching function. However, these exotic solutions are not present in most of commercial technologies.

On the other hand, BiCMOS technologies are becoming extremely popular and show very competitive performance at a relatively reduced cost. Nowadays, the well-established solutions to implement the switching function across these technologies are HBTs and MOSFETs. Disregarding the chosen topology, a better performance is achieved when the most common Figure-of-Merit ( $FoM$ ) for switches presents the smallest value. This metric is defined as:

$$FoM = R_{ON} \cdot C_{OFF} \quad (5)$$

where  $R_{ON}$  and  $C_{OFF}$  are the equivalent resistance in the ON-state and capacitance in the OFF-state (i.e. transistor in the linear and cut-off regions, respectively).

This metric is technology-dependent and the accurate choice of the optimal point in a given technology ultimately determines the best trade-off between the losses and isolation of the designed SPDT switch. Note that this metric has two independent variables. Hence, in order to achieve a fair comparison,  $C_{OFF}$  is fixed to a constant value for both architectures, letting them show their best performance in terms of  $R_{ON}$ .

The parasitic effects introduced by  $C_{OFF}$  do not only lead to decreased performance due to the undesired leaking through the transistor but also shift the frequency response of the switch and lead to poor output return loss (i.e. in ports 2 and 3 of Fig. 1). For this reason, most of the architectures implement a short-circuited stub to compensate the effect of  $C_{OFF}$  (e.g. in [6]). However, as introduced before, a simplified approach is considered here to better highlight the performance of the transistors.

Finally, concerning the design of the HBT-based transistor, a reverse saturation configuration is considered. As pointed out in [6], this configuration leads to reduced parasitic capacitances and larger OFF-state resistances. For this reason, this architecture was subsequently employed in other designs as well [7].

### III. PRACTICAL IMPLEMENTATION AND RESULTS

The proposed architectures were integrated in the STM 55-nm BiCMOS technology. This SiGe-based technology features a 8-metal-layer Back-End-Of-Line (BEOL). The S-CPWs were designed stacking metals 7 and 8 for the signal and ground strips while metal 5 was used for the fingers. The signal and ground strips were designed with widths,  $W_s$  and  $W_g$ , of 12  $\mu\text{m}$ . The gap,  $G$ , between signal and ground strips was set to 49  $\mu\text{m}$ . In their turn, the finger width and spacing,  $SL$  and  $SS$ , were set to 1  $\mu\text{m}$ . Finally, the total length for these TLines is of 278  $\mu\text{m}$ .

In their turn, the HBT transistors were implemented using an NPN-type with 5 emitters and an emitter length and width of 9 and 0.38  $\mu\text{m}$ , respectively. On the other hand, the MOSFETs were integrated using NMOS transistors with a length of 55 nm and a width of 18  $\mu\text{m}$  split on two gate fingers. These transistors were biased at their base/gate level using on-wafer 1.5-k $\Omega$  resistors. These dimensions were chosen as they both represent geometries that lead to good performance (i.e.,  $FOM$ ) in the considered technology while presenting a similar  $C_{OFF}$ . Post-layout simulation reveals that the  $C_{OFF}$  of these transistors are of 20 and 22 fF while the

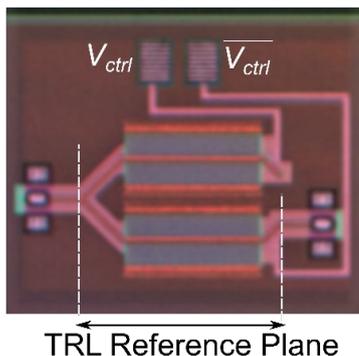


Fig. 4. Microphotograph of the MOSFET-based switch with the reference planes after TRL calibration.

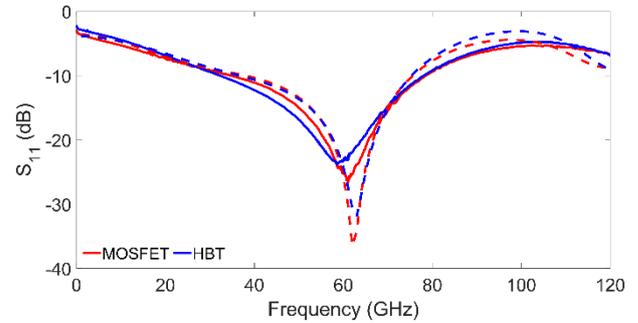


Fig. 3. Measured (solid-line) and simulated (dashed-line) magnitude of the  $S_{11}$  in the 1-120-GHz frequency range for the MOSFET- and HBT-based architectures.

ON-state resistances are 12 and 16  $\Omega$  for the HBT- and MOSFET-based architectures, respectively.

Finally, the T-junction was designed using a microstrip architecture. Note that an SPDT switch is a three-port device. However, in order to allow a two-port measurement, one of the output ports was loaded with an on-wafer 50- $\Omega$  resistor. A microphotograph of the MOSFET-based SPDT switch is shown in Fig. 4 with the measurement reference planes. The HBT-based switch shares an identical structure and hence not shown as no difference would be observable. Both circuits present a footprint of 0.12  $\text{mm}^2$ .

Measurements were carried out using an Anritsu VectorStar ME7838A4 Vector Network Analyzer (VNA), from 1 GHz to 120 GHz. An on-wafer Thru-Reflect-Line (TRL) calibration [16] was carried out setting the reference planes and the I/Os of the switch, as shown in Fig. 4. The transistors were biased using 1.2 V, which for the case of the HBT led to a 0.5-mA current, ensuring a minimal value of their  $R_{ON}$ .

Fig. 3 shows the measured (solid-line) and simulated (dashed-line) for the  $|S_{11}|$  parameter. Simulation and measurement show very good agreement for both architectures. The SPDT were designed for low insertion loss around 50 GHz where the HBT-based and the MOSFET-based show a return loss of 17 and 15 dB, respectively. If the system bandwidth is defined for a return loss greater than 10 dB, the HBT-based architecture has a 30-80-GHz frequency bandwidth while the MOSFET-based has a 33-80-GHz frequency bandwidth. Hence, if a central frequency of 50 GHz is considered, the HBT- and MOSFET-based SPDT switches show a Relative Bandwidth (RBW) of 100% and 94%, respectively.

On the other hand, Fig. 5 displays the magnitude of  $S_{21}$  in both SPDT states, thus showing the insertion loss and isolation of the fabricated switches for both simulation (dashed-lines) and measurement (solid-lines). Note that some divergences at high frequency are observed for the insertion loss when behaving as a thru connection. This can be easily

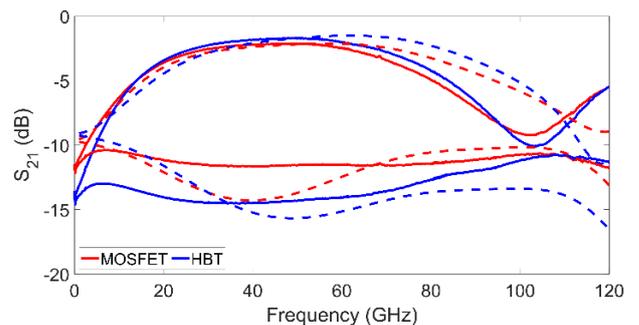


Fig. 5. Measured (solid-line) and simulated (dashed-line) magnitude of the  $S_{21}$  in the 1-120-GHz frequency range.

TABLE I COMPARISON TO STATE-OF-THE-ART SPDT SWITCHES

Ref	Tech.	Freq. (GHz)	RBW (%)	IL (dB)	Iso (dB)	Area (mm <sup>2</sup> )	Power (mW)
[6] (HBT)	90-nm BiCMOS	77-110	35	1.4	19	0.14	8
[7] (HBT)	0.25- $\mu$ m BiCMOS	5-13	88	2.5	32	0.63	18
[8] (NMOS)	90-nm CMOS	75-110	38	3	47	0.12	0
[10] (NMOS)	45-nm CMOS	90-110	10	5.3	21	0.56	0
[11] (NMOS)	65-nm CMOS	20-60	100	2.8	20	0.42	0
<b>This work (HBT)</b>	<b>55-nm BiCMOS</b>	<b>30-80</b>	<b>100</b>	<b>1.7</b>	<b>14</b>	<b>0.12</b>	<b>0.6</b>
<b>This work (NMOS)</b>	<b>55-nm BiCMOS</b>	<b>33-80</b>	<b>94</b>	<b>2.1</b>	<b>12</b>	<b>0.12</b>	<b>0</b>

explained by the density rules of the used technology demanded filling the zones beneath the S-CPWs with dummy metallic structures, leading to a greater propagation constant of these TLines, which shifted the response towards the lower frequencies. Hence, being more remarkable when the TLines achieve an electrical length of  $\pi$  rad (i.e. at around 100 GHz). At 50 GHz, the SPDT switches show 1.7-dB and 2.1-dB of insertion loss, for the HBT- and MOSFET-based architectures, respectively. Within the defined band, the former achieves a maximum insertion loss of 4.1 dB while the latter shows a maximum 4.9-dB of insertion loss. On the other hand, the isolation of the HBT-based architecture is around 14 dB throughout the considered band while the MOSFET-based shows an isolation of around 12 dB throughout the considered band. Finally, simulation-based results show that the Input 1-dB Compression Point, is achieved at 18.8 dBm for the former, and 13.6 dBm for the latter.

To put the results into perspective, the implemented devices are compared, in Table I, to the current literature this matter. Note that, for the sake of comparison fairness, only the architectures similar to the one shown in Fig. 1 are considered.

As demonstrated in Table I, the switches presented hereby show very good performance in terms of insertion loss, RBW, and reduced footprint, when compared to the literature. The degraded performance in terms of isolation can be explained thanks to the fact that no strategy to counteract the OFF-state capacitance of the transistors was addressed. However, these strategies were out of the scope of the work, as stated previously. The reduced footprint is achieved thanks to the use of the slow-wave TLines, as stated before. In addition, a close study of the literature shows that the largest RBW are reported by SPDT switches using slow-wave TLines [7], [11]. The results summarized in this table show that the HBT-based architecture reported a nearly 10% reduction on the insertion loss and a 37% increase in the isolation, when compared to the MOSFET-based architecture. On the other hand, increased performance comes at the price of a static power consumption of 0.6 mW.

#### IV. CONCLUSIONS

In this work, a comparison between the use of HBTs and MOSFETs for the design of mm-Wave SPDT switches has been carried out. To the best of our knowledge, this is the first time that such a comparison is given in a single technology for SPDTs. The superiority of the HBTs comes at the cost of

static power consumption. Hence, applications where power consumption is a critical issue should favor MOSFET-based SPDTs as their performance is comparable to the HBT-based topologies. In addition to the power saving, classical CMOS technologies are generally cheaper than BiCMOS processes. On the other hand, applications that aim at high performance and that do not have tight power consumption constraints, should favor HBT-based topologies.

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