

Review on Intelligent Power Modules

IWIPP 2021 Webinar



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Outline



- 1 Introduction**
- 2 Review of Existing Smart Power Modules**
- 3 “Smart” features**
- 4 Packaging Technologies for IPMs**
- 5 Conclusion**

Introduction

ECPE report on “smart power modules”

- Accessible to ECPE principal members
- 200 pages, 300 references
- Not included here: discussion on future trends
- <https://www.ecpe.org/>

This presentation is a literature review, all images and data belong to their respective owners.



What is a Smart Power Module?



Intelligent Power Module (IPM) ↔ Smart power module

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The following are *not* considered IPMs here:

- A standard power module with just an additional temperature sensor
- Plug-in features which mount on top of power modules
- Monolithic integrated power circuits
- Integrated power converters (e.g. DC/DC converters)
- Very specific devices such as the IGCT

What is a Smart Power Module?

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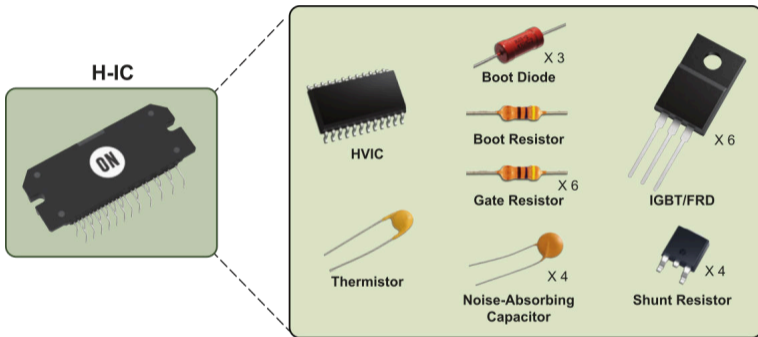
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- Very specific devices such as the IGCT

IPMs have at least (in a single package):

- 2 power devices
- Some gate driver circuitry
- Some additional features (temperature/current sensing, protections. . .)

Example of a Smart Power Module



Source: On Semiconductor [1]

Typical IPM used for motor control (3 phase inverter)

Review of Existing Smart Power Modules

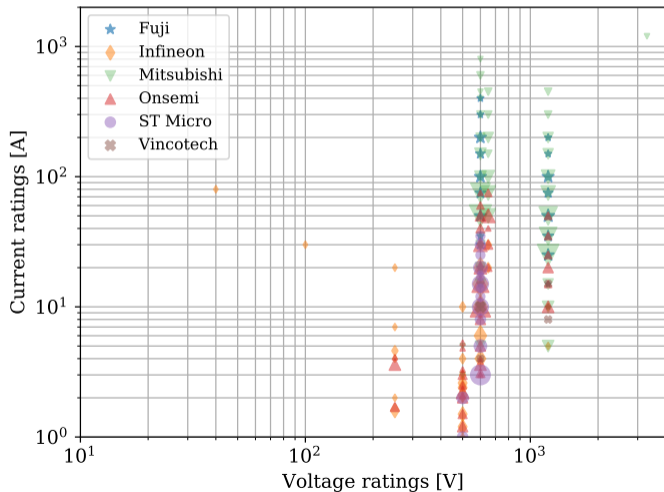
Commercial offering of IPMs



Commercial offering of IPMs



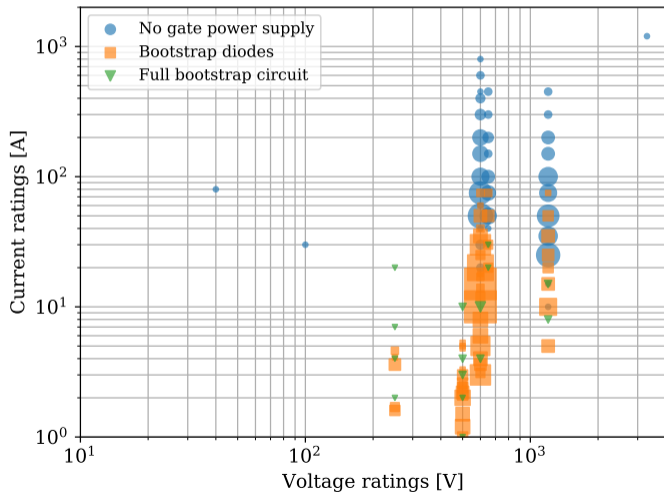
- Voltage/current ratings
- Portfolio per manufacturer



Commercial offering of IPMs



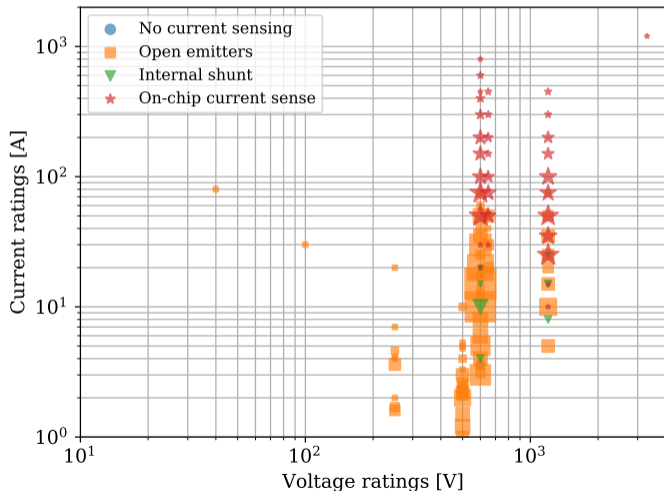
- Voltage/current ratings
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- Packaging technologies
- Gate drive power supply



Commercial offering of IPMs



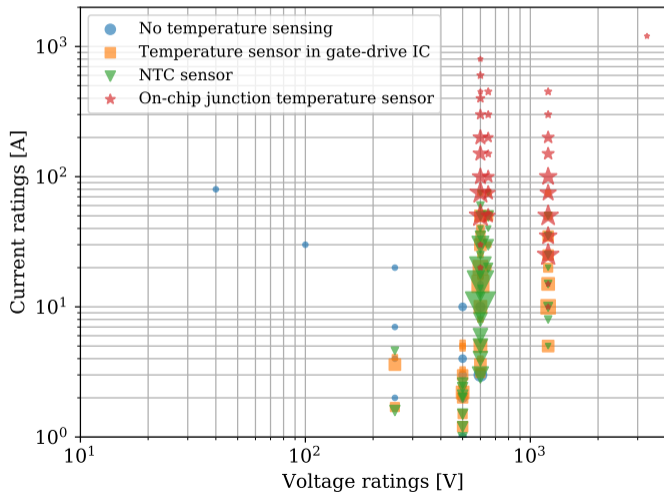
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- **Current sense technology**



Commercial offering of IPMs



- Voltage/current ratings
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- Current sense technology
- Temperature sense technology



Commercial offering of IPMs

- Voltage/current ratings
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- Current sense technology
- Temperature sense technology

→ two broad categories of IPMs:

- < 20 kVA
- > 20 kVA

Commercial offering of IPMs



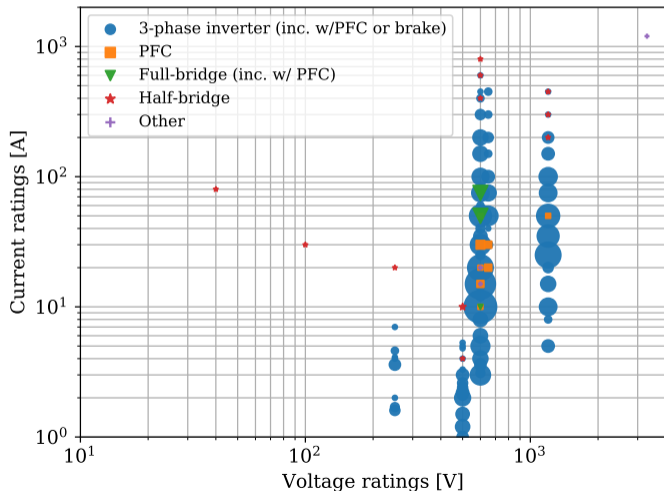
- Voltage/current ratings
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- Current sense technology
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• Topologies

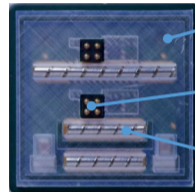
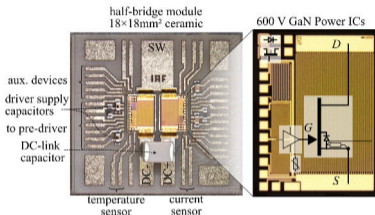
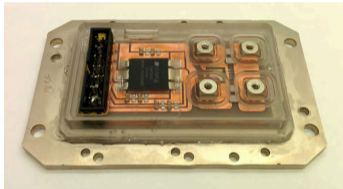
→ two broad categories of IPMs:

- < 20 kVA
- > 20 kVA

→ Mainly 3-phase inverters



IPMs in the Scientific Literature – High Switching Frequency



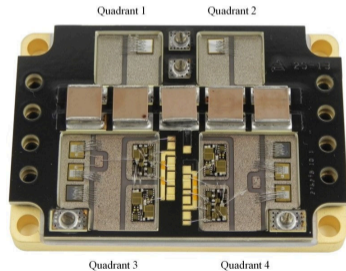
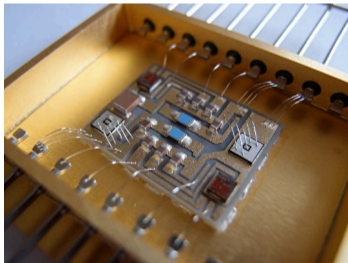
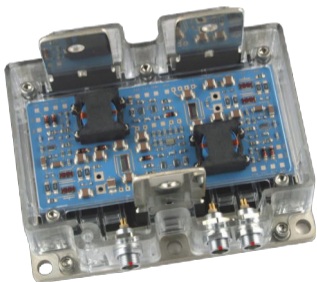
- Plastic frame
- Signal spring connector
- Power spring connector

Source: Jorgensen *et al.* [2]; Moench *et al.* [3]; Marczok *et al.* [4]

- Integration of gate driver close to the power chips
- Monolithic integration (for GaN power devices)
- Low inductance interconnects; control of parasitic capacitances

IPMs in the Scientific Literature – High Temperature

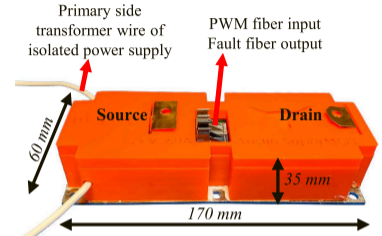
- Based on SiC power devices (JFETs), for $T_J = 250\text{ }^\circ\text{C}$ or more
- Single package for power and gate drives
- Ceramic-based + high temperature resin
- Limits: insulation functions (encapsulation, power/signal insulation)



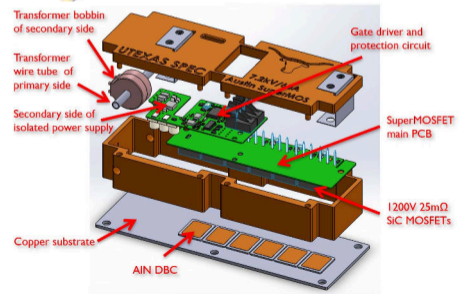
Source: Mc Pherson *et al.* [5]; El Falahi *et al.* [6]; Whitaker *et al.* [7]

IPMs in the Scientific Literature – High Voltage

- Also suited to SiC devices
- Insulation coordination between power and drive
- Can “mask” unusual device configuration
 - Bipolar transistors
 - Super Cascode...

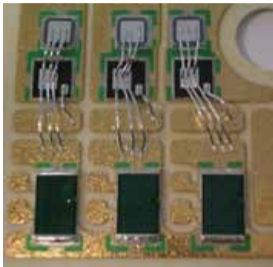


Source: Zhang *et al.* [8]



“Smart” features

Current Sensing – Some Sensor Types

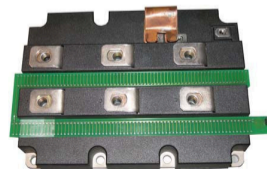
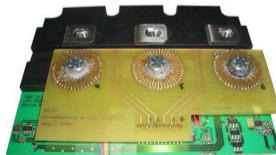
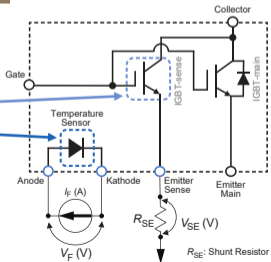
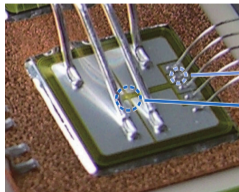
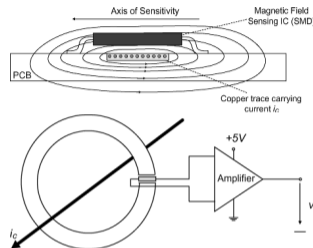


← integrated current shunts [9]

Open and closed field sensors [10] →

IGBT sensor [11]

Rogowski sensor [12]



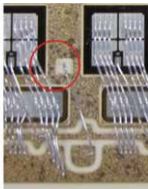
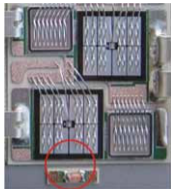
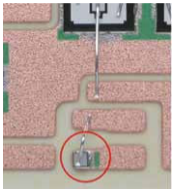
Current sensing summary



Sensor	Bandwidth		Sensitivity	Integration	Usage		Comment
	Low	high			Sens.	Prot.	
Ohm's law							
Shunt	DC	10 kHz	T	Good	++	++	limited by power dissipation
Interconnect. res.	DC	10 kHz	T	Excellent	+	++	Low SNR, high TCR
MOSFET $R_{DS(on)}$	DC	100 kHz	T, V_{GS}	Excellent	+	++	1 st quad. only, very high TCR
Faraday's law of induction							
Rogowski	10 kHz	100 MHz		Fair	-	++	No saturation, very fast
Transformer	10 Hz	10 MHz	I_{DC}	Poor	-	+	Saturation, no conditioning
Interconnect. ind.	1 Mhz	100 MHz	T, EMI	Excellent	-	++	Bias caused by resistance
Magnetic field sensing							
Hall (open)	DC	10 kHz	T, Ext. Field	Good	+	-	Slow, sensitive to ext. fields
Hall (closed)	DC	10 kHz	T	Poor	+	-	Slow, saturation of core
Fluxgate	DC	10 kHz	T, Ext. Field	Good	+	-	Slow, sensitive to ext. fields
(X)MR	DC	1 MHz	T, Ext. Field	Good	++	-	sensitive to ext. fields
Semiconductor-based							
Current Mirror	DC	100 MHz	T	Good	+	++	1 st quad. only, sensitive to T
Desat. detection	DC	10 MHz	T, V_{GE}	Good	-	++	Mainly suited to IGBTs, coarse

→ Hybrid sensors seem necessary, with Rogowski + field sensors most promising.

Temperature Sensing – Discrete sensors



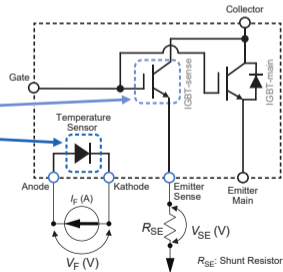
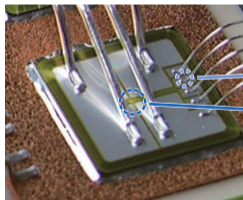
a)

b)

c)

Discrete temperature sensors, with or without electrical isolation [9]

On-chip temperature sensor [11]



Temperature Sensing Summary



Sensor	Time const.	Senses	Integration	Sig. Cond.	Comment
Discrete sensors					
RTDs	1-10 s	T_{case}	Good	Simple	More expensive than thermistors
Thermistors	1-10 s	T_{case}	Good	Simple	Commonly used in IPMs.
Semiconductor sensor	1-10 s	T_{case}	Good	Integrated	Integrated in gate drive
Integrated sensors					
PN junctions	10 μ s	T_j	Excellent	Simple	Used for all current-sensing transistors
RTDs	10 μ s	T_j	Excellent	Simple	Can use metal layer of power chip
Temperature-Sensitive Electrical Parameters					
Miller plateau ampl.	1 ms	T_j	Excellent	Complex	Sensitive to ageing or parameter scattering between chips
Switching timing	1 ms	T_j	Excellent	Complex	
Volt. drop across L_e	1 ms	T_j	Excellent	Complex	

- Integrated sensors required for on-chip current measurement
- TSEP do not seem convenient for temperature measurement outside of lab
 - May be used for condition monitoring?

IC technologies

3 voltage levels required for a gate circuit:

LV: typ. 5 V, for logic circuits

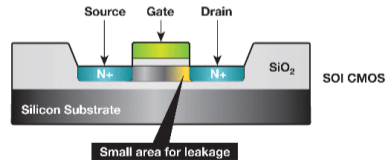
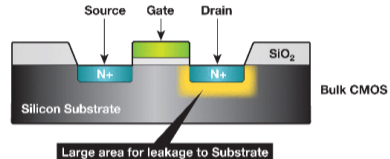
MV: typ. 15-20 V, for gate control

HV: typ. 650 or 1200 V, DC bus voltage

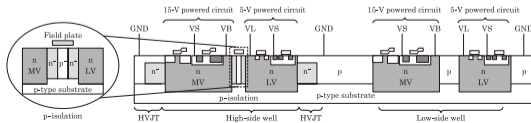
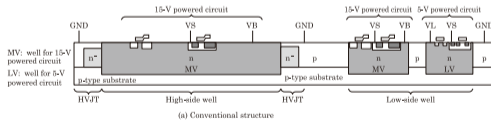
2 technologies

BCD (Bipolar CMOS DMOS), on Si bulk, <150 °C

SOI (Silicon On Insulator), can operate >200 °C



Source: left Jonishi *et al.* [13], top Romanko *et al.* [14]



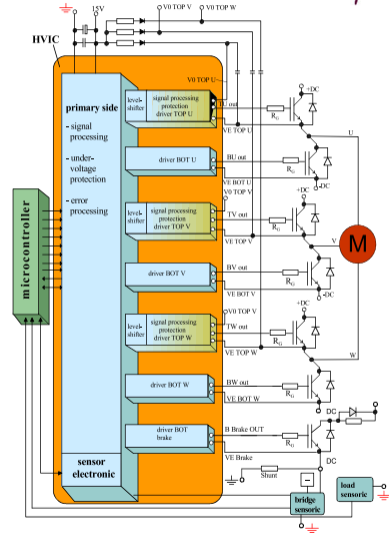
Control features

Gate drive standard features

- Signal isolation
 - level shifter, magnetic isolation, fiber optics
- Power supply
 - only bootstrap, no integrated DC/DC available
- Output buffer
- Protections

Gate drive advanced features

- Advanced control
 - Switching speed control; miller clamp; ...
- Condition monitoring (currently not implemented)



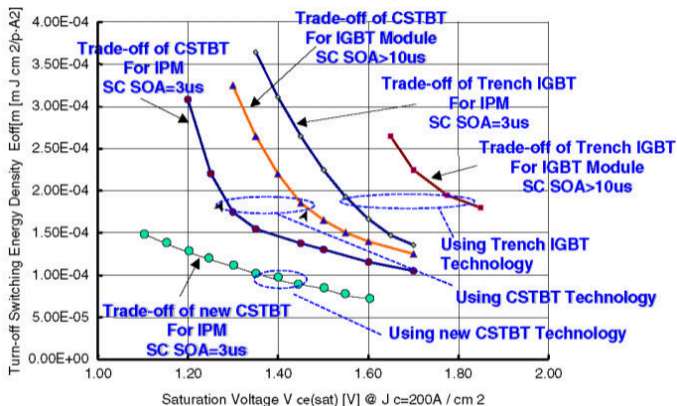
Source: Herzer *et al.* [15]

Matching power device and gate drive circuit



Faster protections thanks to:

- On-chip sensors
- Well defined components
- Known circuit parasitics



Source: Majumdar *et al.* [16] (2007)

Matching power device and gate drive circuit

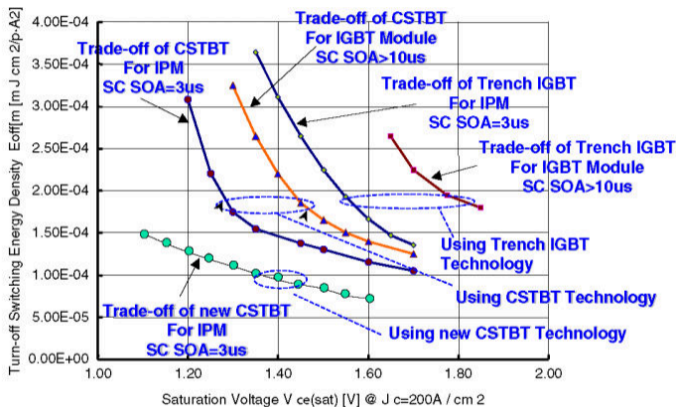


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To use “weaker” devices:

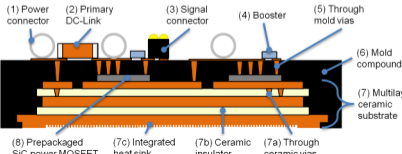
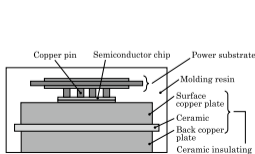
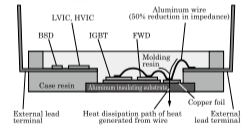
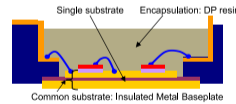
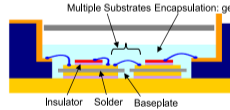
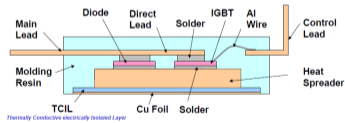
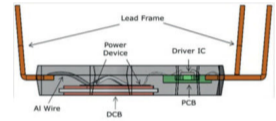
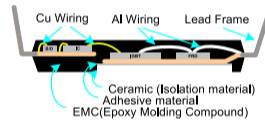
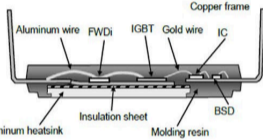
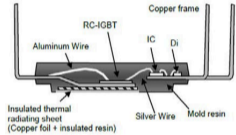
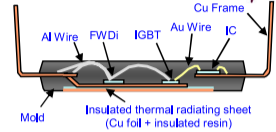
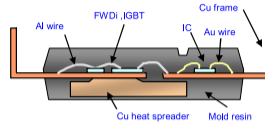
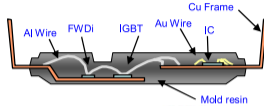
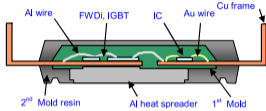
- Less robust to short-circuit
- Lower losses
- Same trade-off for SiC MOSFETs



Source: Majumdar *et al.* [16] (2007)

Packaging Technologies for IPMs

IPM Packaging structures investigated



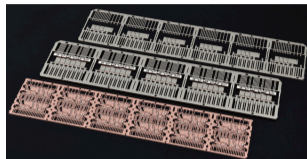
Sources (from left to right, and top to bottom): [17, 17, 17, 17, 18, 18, 19, 20, 21, 22, 22, 23, 24, 25]

Substrates



Lead frame

- Most common for low power IPM
- Thermal performance limited by moulding compound
- Ceramic or metal insert for improved thermal performance

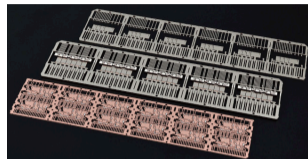


Source: SH Precision Japan,
<https://shpj.co.jp/>

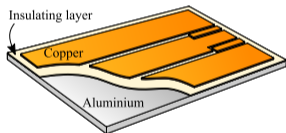
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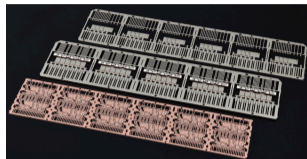
Insulated Metal Substrates & Variants

- Usually poor thermal conductivity
- BN-loaded insulating resin up to $20 \text{ W} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$
- Together with thick ($\approx 1 \text{ mm}$ or more) copper, strong trend.

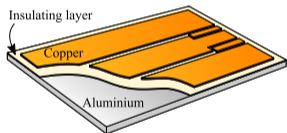
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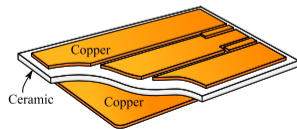


Insulated Metal Substrates & Variants

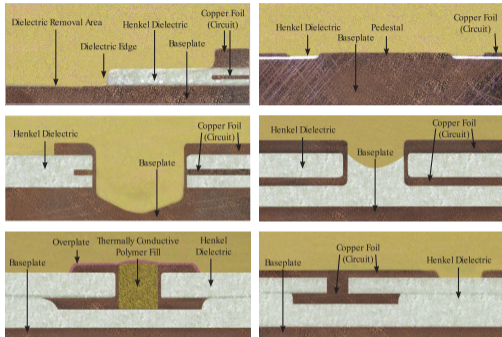
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Ceramic Substrates

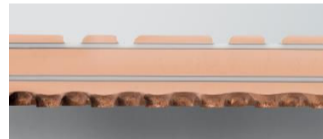
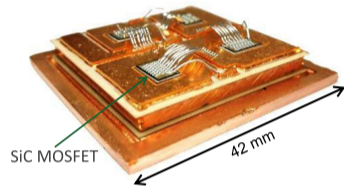
- Orientation toward thin ($2\text{--}300 \mu\text{m}$) ceramics, with thick copper
- $\text{Zr-Al}_2\text{O}_3$, Si_3N_4
- More traditional structures for high voltage only ($>1700 \text{ V}$)



Substrates – Trends



Multi-layer and “3D” IMS features for improved thermal management, low inductance or common mode shielding [26].



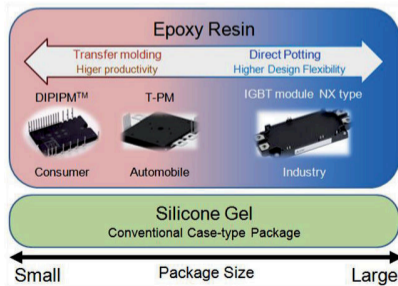
“thin ceramic/thick copper” DBC structure [27]

→ overall CTE of organic or inorganic substrates approaches that of copper (16.5 ppm/K).

Encapsulation

- **Many possible candidates**

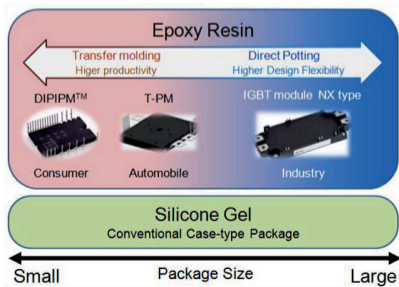
- conformal coatings, volume encapsulants
- Silicone, epoxy, polyimide, parylene, cyanate ester, bismaleimide, inorganic cement. . .



Source: Asada *et al.* [28]

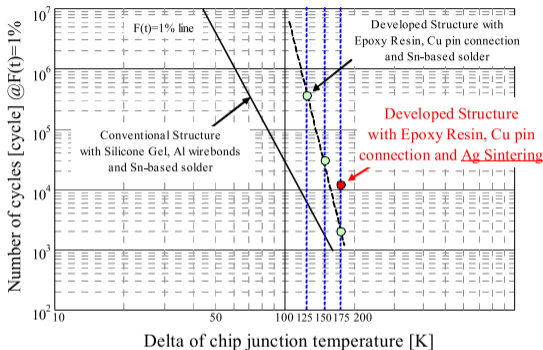
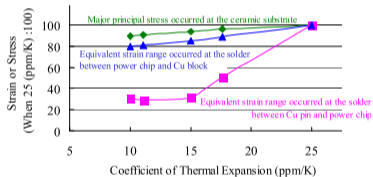
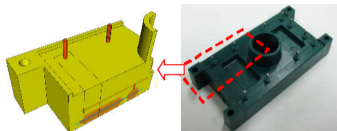
Encapsulation

- **Many possible candidates**
 - conformal coatings, volume encapsulants
 - Silicone, epoxy, polyimide, parylene, cyanate ester, bismaleimide, inorganic cement. . .
- **Epoxy most promising for $\approx 200\text{ }^{\circ}\text{C}$**
 - Coefficient of Thermal Expansion (CTE) matching that of copper
 - Higher breakdown field than silicone
 - Recycling may become an issue



Source: Asada *et al.* [28]

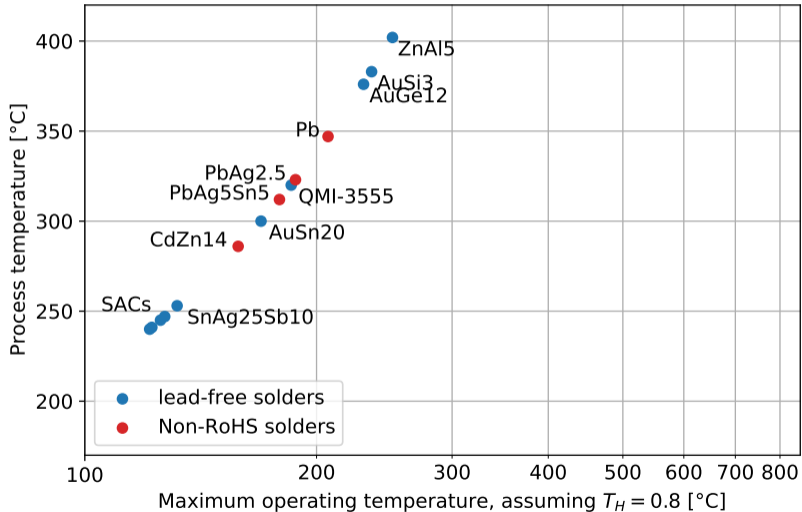
Encapsulation – trends



Source: Horio *et al.* [29]

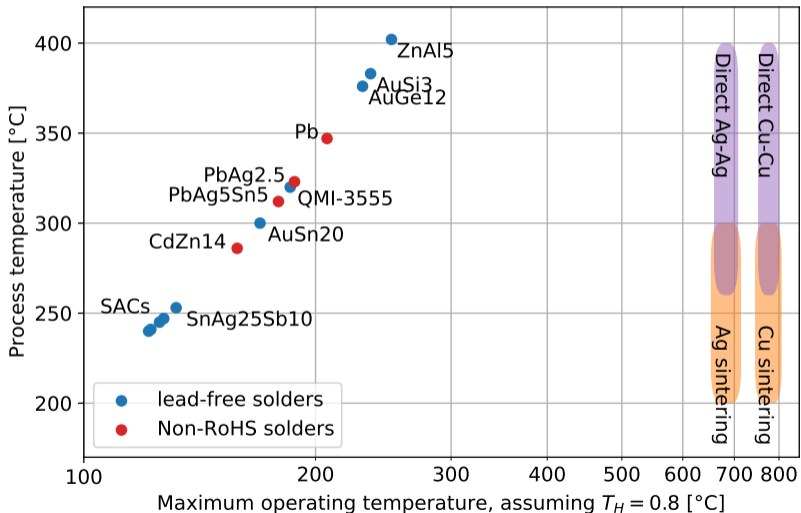
- CTE of encapsulant approaches that of copper
- Better reliability reported by Fuji and Mitsubishi, but no third party analysis
 - Is it true for thin IGBTs only?
 - What about thicker or stiffer (SiC) chips?

Die attach



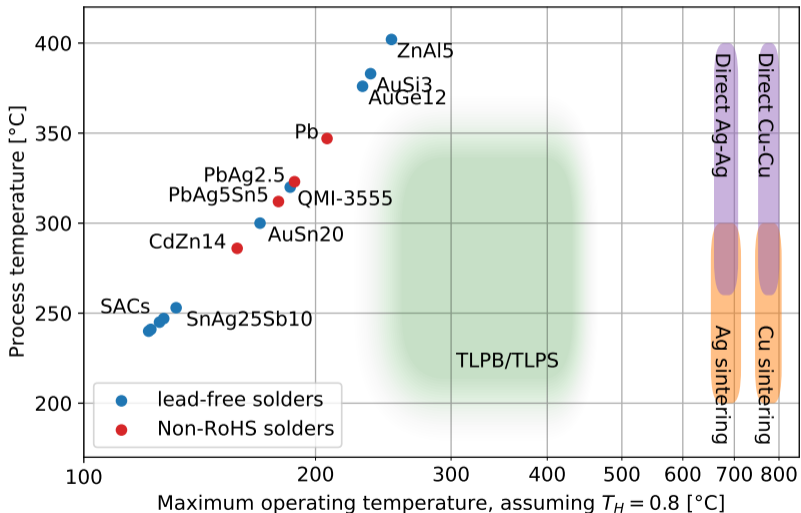
- Few high temp, Pb-free solders

Die attach



- Few high temp, Pb-free solders
- Cu- or Ag-sintering excellent replacements

Die attach

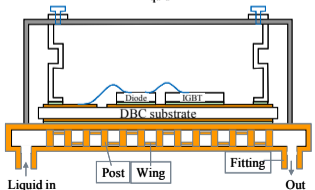
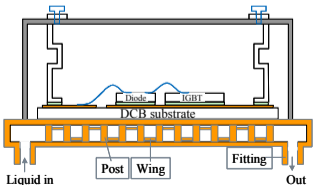
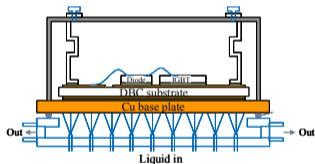
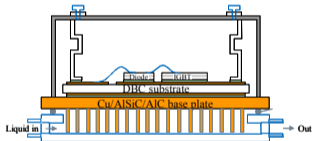
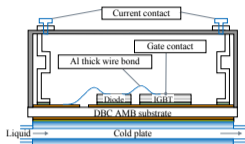
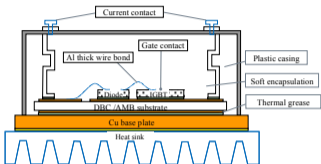


- Few high temp, Pb-free solders
- Cu- or Ag-sintering excellent replacements
- What about Transient Liquid Phase Bonding?

Cooling

← Source: Schulz *et al.* [30]

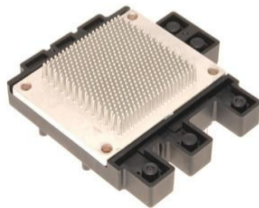
- Many cooling solutions
- IPMs need interface standardisation



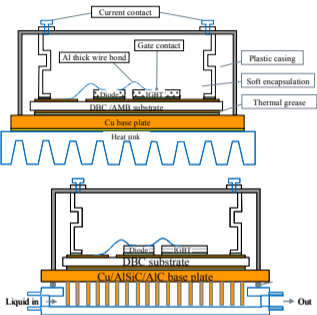
Cooling

← Source: Schulz *et al.* [30]

- Many cooling solutions
- IPMs need interface standardisation
- Only two configurations gained acceptance:
 - flat surface for heatsink
 - pin fins for direct water cooling

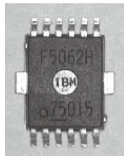
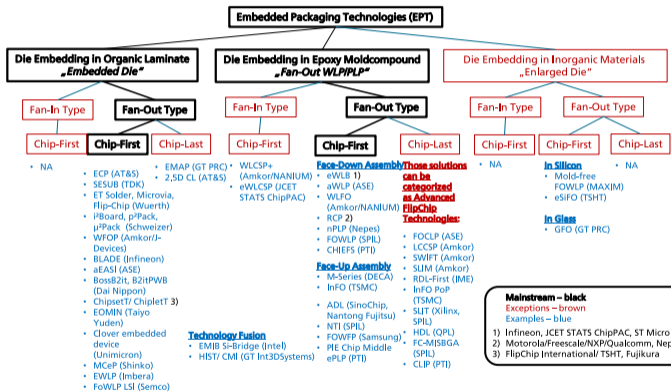


↑ Source: Majumdar *et al.* [31]

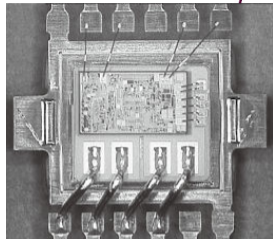


Heterogeneous Integration

Diversity of Fan-Out Packaging

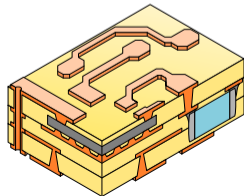


(a) External appearance



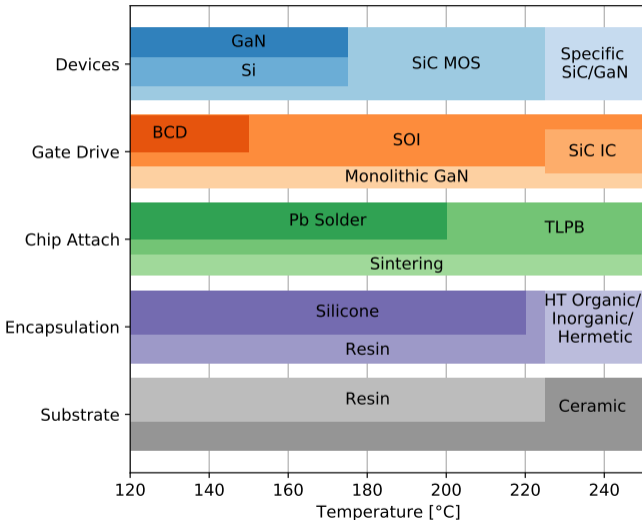
(b) Internal structure

← Fan-out [32], ↑ Chip on chip [33], PCB embedding ↓



Conclusion

Summary on Technologies



Materials

- Incremental changes to reach $T_j = 200-225\text{ °C}$
- Very few SiC IPMs on the market

Structure

- Multi-layer packages
 - Low parasitics
 - Higher integration density
- Thick copper layers
 - Package CTE matching that of Cu.
 - Thin insulation layers

Conclusion



- Most IPMs target mass markets
 - 3-phase inverters for motor control, new topologies may develop, e.g for automotive
- More advanced features (sensors, supplies, etc.) may be required for high-end IPMs
 - High power/voltage, SiC-based
 - IPMs can “mask” exotic devices/exploit “weaker” devices
- Trend towards “organic” packaging:
 - IMS substrates, epoxy encapsulation, even for higher power/voltages
 - IPM technologies may take advantage of other heterogeneous integration technologies
 - Recycling not addressed

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