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Surge Current Capability of IGBT Based Power Electronic Interrupter Modules for Hybrid DC Circuit Breaker Applications

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Abstract—The power electronic interrupter (PEI) is a key component of the dc hybrid circuit breaker (HCB) as it facilitates the arc-less opening of the mechanical switch by taking over the fault current during the interruption process. A modular implementation of the PEI enables design scalability allowing the use of high peak current density discrete IGBTs in a seriesparallel configuration as needed for the maximum transient voltage and peak fault current levels seen by the system. In this paper, surge current turn-off experiments are conducted on discrete IGBTs to determine the limiting factors for fault current interruption. Experimental data are provided to show IGBT performance under two different PEI module configurations and identified failure modes are discussed along with main design tradeoffs.

Keywords—Failure modes, hybrid circuit breaker, IGBT, power electronic interrupter, surge current capability.

I. INTRODUCTION

There is a renewed interest in dc power distribution systems as they offer advantages over conventional ac systems in terms of the power density and efficiency of power distribution while providing the flexibility for easy integration of renewable energy sources and energy storage systems [1]. However, fault protection apparatus such as circuit breakers are required to enable the growth of future medium voltage dc (MVDC) networks. The absence of natural zero crossings and potentially high fault currents bring several challenges to the development of dc circuit breakers [2]. Hybrid circuit breakers (HCB) are a promising solution to this problem offering high efficiency and reliability with reasonable response times ($\sim 500~\mu s$) [3]-[7].

The power electronic interrupter (PEI) of the HCB consists of the power semiconductor device and the voltage clamping circuit used for fault current interruption and inductive energy absorption respectively. The power semiconductor device in the PEI must be able to turn off the fault current without entering desaturation or dynamic avalanche and the device package must be able to handle the thermal load for the duration of the fault event. It has been found that the IGBT can safely conduct (durations up to 5 ms) and turn-off very high surge currents (> 5× rated) making it a suitable candidate for the PEI [8]. Furthermore, the IGBT can be easily controlled (saturation current, on-state voltage) by changing the parameters of its gate driver unit. A typical HCB with an

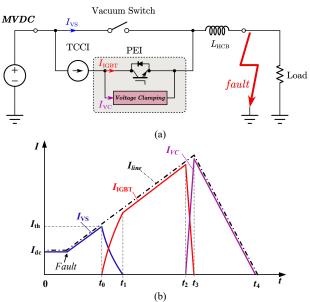


Fig. 1. (a) Typical HCB using an IGBT based PEI; (b) HCB fault current conduction path and commutation sequence.

IGBT based PEI is shown in Fig. 1(a) and idealized waveform of the line current and the commutation sequence is shown in Fig. 1(b). The fault current transfers to the PEI when it reaches the fault threshold value I_{th} at time t_0 . The PEI must be able to conduct the current from time t_0 to t_2 which can be as high as 500 μ s in duration. Further, the PEI should successfully turnoff the peak current at time t_2 to allow the parallel voltage clamping circuit to drive the current to zero by generating a negative voltage across the series line inductance.

In this work, several discrete IGBTs are evaluated for use in the PEI module due to their high surge current specification (datasheet values up to $\sim 7\,\text{x}$ rated) and compact package offering high peak current density with sufficient thermal mass to sustain a surge current durations of $\leqslant 1$ ms. The peak device voltage in the PEI is determined by the voltage clamping circuit. Two commonly used configurations of the PEI module are considered in the surge current experiments as shown in Fig. 2(a); type 1 module – IGBT with MOV and type 2 module – IGBT with RC snubber and MOV. An experimental platform is built to determine the type of voltage

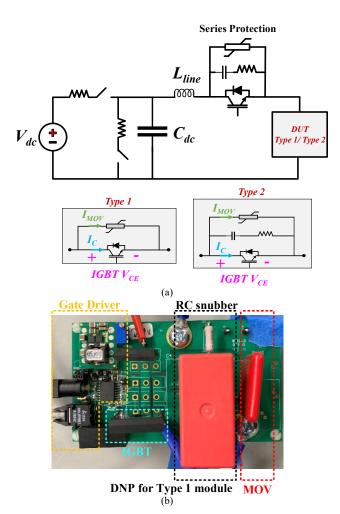


Fig. 2. Surge current test circuit: (a) schematic of both PEI module types; (b) PEI module testbed PCB (DUT).

clamping circuit that will allow the device to achieve the highest surge current value for this application. The failure modes of the two PEI modules are determined and the design trade-offs are established.

II. IGBT SURGE CURRENT TEST BED

Due to the single switching nature of the application, it is desirable to get the maximum utilization out of the power semiconductors in the PEI. Therefore, it is advisable to experimentally determine the peak surge current handling (conduction + turn-off) capability of the IGBT candidates in question. An experimental platform is constructed (see Fig. 2(b)) to conduct a surge current through the DUT IGBTs (beyond its published continuous rating) and subsequently turn off the current to block the clamping voltage as set by the parallel voltage clamping circuit (types 1 and 2). Surge current and clamping voltage values are increased to determine possible failure modes and associated dependencies. The dc bus capacitance is selected to have a near constant bus voltage for the duration of the surge. The inductance and the turn-on pulse width are varied to adjust the peak current value. The device gate-driver is tuned to modulate its transconductance to attain higher peak current levels without desaturation. Due to the limited avalanche capability of the IGBT, the MOV peak clamping voltage is kept below its $V_{\it CE}$ rating.

Typical surge current turn-off transient waveforms for the module types under consideration are provided in Fig. 3. For the type 1 module, as seen in Fig. 3(a), once the IGBT is turned off, the device V_{CE} increases until the MOV reference voltage (V_{ref} : knee point) is reached at t_1 and the current transfers from the IGBT to the MOV branch driving the device voltage to the MOV clamping value (peak value of V_{pk}) until the fault is cleared at t_3 . For the type 2 module, as seen in Fig. 3(b), the IGBT current is transferred to the RC branch after the turn off is initiated. The V_{CE} rises as the snubber capacitor is charged until the voltage reaches V_{ref} (at t_2) when the current transfers to the MOV branch (t_2 to t_3) which then helps absorb the inductive energy and bring the fault current to zero (at t_4) as in the previous case. The IGBT current exhibits a unique phenomenon as the device voltage reaches its peak value (V_{pk}) and will be discussed in detail in the next section. The IGBT internal turn off processes for the two module types are very different leading to two separate failure modes that will also be discussed in the following section. It is important to note that the gate drive parameters have a minor influence on the IGBT turn-off process. The IGBT current decay rate and the turn-off tail current depend on the amount of stored charges and the minority carrier lifetime of the device [9].

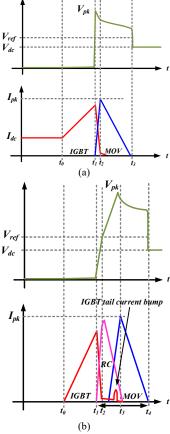


Fig. 3. Typical IGBT surge current turn-off waveforms: (a) Type 1 module turn-off waveforms; (b) Type 2 module turn-off waveforms.

III. EXPERIMENTAL RESULTS AND FAILURE MODES

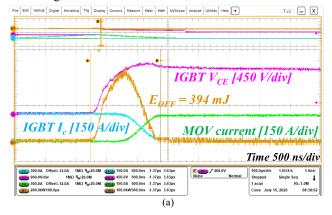
The specification of all the discrete IGBTs tested are provided in Table I. Test results for device 1, with $V_{CErated} = 3$ kV and $I_{C.rated} = 86$ A, is used to illustrate the failure modes. For both the type 1 and type 2 modules, the MOV used in the tests are selected from the UltraMOV 25 S family of 25 mm disc MOVs from Littelfuse and connected in single or series/parallel configuration such that the peak device voltage does not exceed the V_{CE} rating of the DUT. The RC values are varied to change the turn-off dv/dt for comparison and analysis.

TABLE I. SPECIFICATIONS OF THE DISCRETE IGBT CANDIDATES

Device Index	IGBT P/N	Туре	V _{CEmax} (V), I _{C,rated} (A)	I _{c,peak} (A) 1 ms rating
1	IXBF55N300	BiMOSFET	3000 V, 86 A	600 A
2	IXBX55N300	BiMOSFET	3000 V, 120 A	600 A
3	IXBX64N250	BiMOSFET	2500 V, 120 A	600 A
4	IXGX75N250	NPT	2500 V, 160 A	530 A
5	IXGX100N170	NPT	1700 V, 170 A	600 A

A. Type 1 Module

The dc bus voltage is set to be 1 kV and the line inductance is set to 0.45 mH (for parameters in the test circuit in Fig. 2). The turn-on pulse is varied to achieve different peak current values to determine the absolute maximum peak current before device failure. In this configuration, the IGBT operates in a hard switching condition where it is exposed to simultaneous high current and voltage well outside the device SOA [10]. The instantaneous peak power stress seen by the device during the peak current turn-off event can become a concern and lead to failure if the corresponding thermal stress is beyond the device and package capability. Moreover, the peak clamping voltage of the MOV can exceed $V_{CE,max}$ due to the steep front effect without careful MOV circuit design [11]. The experimental results (Fig. 4(b)) show device failure during the turn-off event (surge current about 5x rated value), which poses the biggest threat for this module type. The IGBT is able to turn off 384 A current successfully (Fig. 4(a)), but fails when the peak current is increased to 432 A. The switching loss for the two cases increases from 395 mJ to 460 mJ, which exceeds the device thermal limit and leads to failure. Even if the device is able to survive one such turn-off event (432 A/2.1 kV), the performance and life-time may be degraded over several such events. In general, operation outside the SOA can lead to device degradation and eventual—or direct—failure.



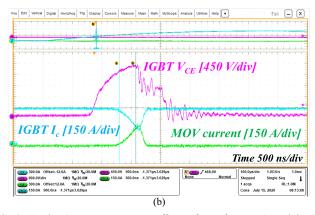


Fig. 4. Device 1 surge current turn-off waveforms for type 1 module: (a) successful turn-off of 384 A at 2000 V Vpk (395 mJ turn-off energy); (a) device failure at 432 A, 2140 V Vpk (460 mJ turn-off energy).

B. Type II Module

The RC snubber in the type 2 module serves two purposes: 1) lower the turn-off power/loss and 2) limit MOV voltage overshoot due to the steep front effect. As seen in Fig. 3(b), the current transfers to the RC branch when the device is gated off. After the current transfer from the IGBT to the snubber capacitor, there remains an amount of free electrons and holes in the drift region of IGBT that are slow to remove due to the near soft-switching operation in this configuration. The charge concentration increases as the turn-off current value is pushed higher. Further increase in device voltage up to the MOV clamping value requires the removal of these free carriers to establish the depletion region. The snubber parameters set the dv/dt across the device during this period reflecting how fast the depletion region expands. This results in a "tail current bump" to facilitate charge removal, whose magnitude depends on the peak voltage V_{pk} and the corresponding dv/dt [12],[13].

Although the energy dissipated in this operating mode may be lower than the critical value for shortcircuit failure, higher "tail bump" magnitudes in the presence of high dv/dt may lead to dynamic avalanche that can create filamentary currents giving rise to a large local increase of temperature and device failure [14]. This phenomenon was observed in the type 2 module experiment for a peak turn-off current of 450 A and a clamping voltage of around 2 kV with $R_{snubber} = 1.2~\Omega$ and $C_{snubber} = 0.44~\mu$ F (see Fig. 5).

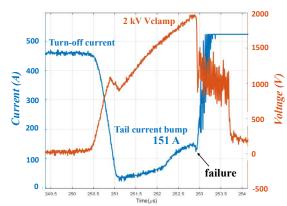


Fig. 5. Test waveforms of device 1 failure under type 2 circuit configuration during IGBT tail current bump stage with a maximum bump value of 151 A.

The failed device was opened for further analysis and the findings (see Fig. 6) matched the hypothesis regarding the current filamentation and localized heating. It should be noted that this failure mode is unique to a (near) soft-switching case where the voltage across the device continues to build after the current has dropped to the hole recombination level, and does not manifest during hard-switching operation. Hence this failure mode is only seen in the type 2 configuration and is not observed with the type 1 circuit which results in a hard switched turn-off event.



Fig. 6. Decapsulated device 1, 3kV IGBT (i4 pak), showing local hotspot failure.

Further tests were performed and it was found that the bump magnitude can be suppressed to acceptable levels to prevent failure by reducing dv/dt and/or reducing the peak clamping voltage level by changing the MOV and RC snubber values (see Fig. 7-Fig. 9). Tail bump magnitude is also affected by changing the snubber resistor or gate resistor values but their influence is not as strong as the MOV and RC snubber values and will be discussed in future publications.

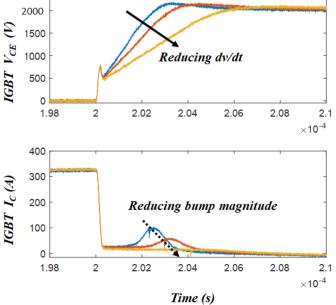


Fig. 7. Reducing "bump" magnitude by increasing snubber capacitance for a slower dy/dt.

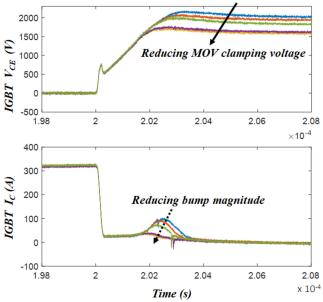


Fig. 8. Reducing "bump" magnitude by reducing MOV clamping voltage.

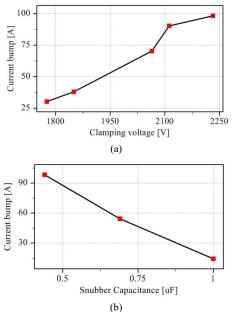


Fig. 9. Current bump magnitudes for (a) different peak clamping voltages; (b) for different snubber capacitor values (dv/dt).

Device 1 was tested in type 2 configuration with a higher value of snubber capacitor $C_{snubber} = 1 \,\mu\text{F}$ with all other parameters unchanged and it was found that the peak surge current can be pushed to 530 A without causing device failure. Although the current bump still exists, its peak magnitude is reduced to < 60 A thus reducing the stress on the device. The waveforms are shown in Fig. 10. Several other discrete commercial IGBTs were tested in type 2 configuration as summarized in Fig. 11. It can be seen that this current bump phenomenon exists across IGBTs of different voltage ratings, physical structure (BiMOSFET, NPT) and package types (i4Pak, PLUS 247) based on the peak turn-off current

magnitude and selection of the clamping voltage value with respect to the device V_{CE} rating along with the applied dv/dt.

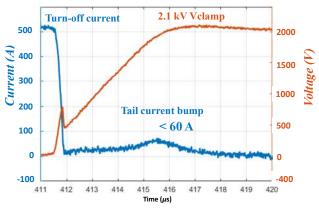


Fig. 10. Device 1 under type 2 circuit with $C_{snubber} = 1 \mu F$ successfully turning off 530 A peak current with peak clamping voltage of 2.1 kV and maximum current bump magnitude of < 60 A.

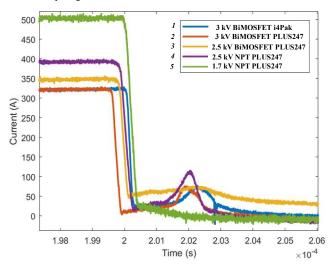


Fig. 11. Tail current bump summary for discrete IGBTs listed in Table I.

C. Discussion

From the device 1 test results presented herein, we can see that the type 1 configuration only allows a peak current of 432 A before device failure due to high peak power stress on the device during the surge current turn off event (simultaneous high current $5 \times I_{rated}$ and voltage). Under type 2 configuration, the tail current bump phenomenon occurs due to the fact that the voltage across the device is still increasing (establish Efield across the depletion region) after the device current has dropped to the hole recombination level due to the near softswitching operation. With the type 2 circuit, the maximum turn-off current for device 1 can be pushed as high as 530 A without device failure by slowing down the device dv/dt as was seen in Fig. 10. Factors influencing the bump phenomenon are IGBT voltage class, the circuit V_{pk} and dv/dt and peak turn-off current value. Based on the experiments and analysis presented in this paper, type 2 circuit is recommended for use in the PEI where the RC snubber and MOV values can be optimized to meet the peak current requirement of the system. Main design

tradeoffs for PEI module selection and design are summarized in Fig. 12.

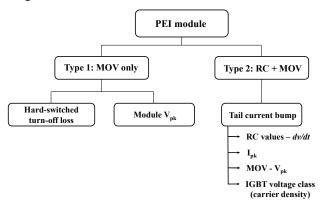


Fig. 12. Trade-off factors for PEI module selection and design..

IV. CONCLUSIONS

In this work, discrete IGBTs are evaluated for an HCB PEI to determine the main failure modes for this application under two separate module configurations. It was found that the highest risk in a snubberless (type 1: IGBT + MOV only) module configuration is failure due to high turn-off power stress, whereas an IGBT+RC+MOV (type 2) module suffers from the tail current bump phenomenon and the corresponding current filamentation failure mode. These findings for a single device can be scaled to parallel device combinations if current, voltage and applied dv/dt are kept the same. It is also found that the current bump phenomenon can be sufficiently suppressed to prevent device failure by lowering the peak clamping voltage value or slowing down the turn-off dv/dt to further increase the safe peak current value of the device. In summary, the type 2 module can help increase the peak turnoff current value of the IGBT device for application in the PEI. Future work will include TCAD simulations to corroborate the experimental findings herein reported.

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