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ABSTRACT: This paper review the research works made so far in associating Ge isoelectronic element to SiC crystals, either by incorporating it inside SiC matrix or for assisting SiC epitaxial growth. The incorporation mechanism and level of incorporation of Ge in SiC during crystal growth with different techniques (sublimation, chemical vapor deposition, vapor-liquid-solid) are compared and discussed. Ge doping level as high as 2-3x10^{20} at.cm^{-3} can be reached without affecting SiC crystalline quality but generating some strain. Higher Ge incorporation levels up to few at% can be reached using farer-to-equilibrium conditions such as ion implantation or molecular beam epitaxy. The former allows retaining 4H-SiC polytype while the latter leads exclusively to defective 3C-SiC polytype. Adding Ge to SiC crystal growth was also used for promoting 3C-SiC heteroepitaxy on Si and on α-SiC substrates, the latter case being more successful. The reported modifications and improvements of SiC crystalline and electronic properties by the incorporation of Ge element are discussed in order to draw or clearer picture of SiC:Ge material. Based on such discussion, some short- and long-term perspectives are proposed

1- Introduction

The development of any semiconductor based technology requires mastering and understanding a high number of fabrication steps which can be very complex. On material aspect, crystalline quality and purity are essential. The former allows reaching the predicted properties of the material while the latter allows working on the intentional doping type and level of the semiconductor. The n and p type doping elements are usually well identified for each semiconductor and their incorporations using different elaboration techniques are widely documented. The incorporation of metallic impurities is also commonly investigated for improving the semiconductor properties such as increasing resistivity (Fe in GaN [1], V in 4H-SiC [2]), tuning optical emission (Er in GaN [3] or Si [4]) or providing magnetic properties (Mn in GaAs [5] or Ge [6]). Isoelectronic (also named isovalent) doping is similarly frequent in the case of binary (III-V or II-VI) semiconductor compounds due to the usual important miscibility between elements of the same column and/or valence. It can lead to bandgap tuning [7, 8], obtaining of new properties [9,10] or crystalline improvement [11,12].

In the particular cases of column IVB semiconductors, the isoelectronic doping concerns only elements of the same column which reduces substantially the possibilities. Important solubility exists

only between Si and Ge elements with the possible formation of $Si_{1-x}Ge_X$ alloys over the full range of composition (see below for a description of the phase diagram). Interestingly, at the extreme compositions of the phase diagram, Ge doping of Si was found to be beneficial to Si properties [13,14] while the reverse (Si doping of Ge) does not seem to be of real technological interest. C doping of these two elements (taken separately) is not only difficult to implement but also ineffective to tune the properties. On the other hand, in the case of SiGe alloys C doping has been long studied for growing $Si_{1-x-y}Ge_xC_y$ alloys for reducing lattice mismatch between Si and $Si_{1-x}Ge_X$ while providing an additional design parameter for manipulating electronic properties [15]. Considering Sn element, despite limited solid solubilities, doping of Ge or SiGe alloys is possible with up to several at% Sn, which leads to new classes of materials with various potential applications [16, 17]. In the case of diamond, which has the smallest lattice constant and widest bandgap of column IVB semiconductors, doping with the almost insoluble isovalent impurities (Si, Ge, Sn or Pb) is recently attracting much interest for quantum photonics [18] due to the formation of color centers with suitable properties.

Coming now to SiC, which is the topic of the present review, it displays higher solubilities than diamond for the other bigger isoelectronic elements Ge, Sn or Pb. But these solubilities do not allow forming real ternary alloys. Note that the boundary between doping and alloying is not clear and it varies significantly from one system to another. We will use in this paper, for the specific case of incorporating a foreign atom into SiC, the term "doping" for impurity concentration < 1 at%. Above this value, the term "alloy" will be used. To the best of our knowledge, no experimental Pb doping of SiC was ever reported though theoretical properties of such material were studied [19]. Only few experimental reports mention Sn doping with incorporation values in the 10^{16} at.cm^{-3} range [20,21]. Ge incorporation into SiC was obviously more studied due to substantially higher incorporation levels even if, as we will see later, SiC-based ternary alloys are rarely obtained, and in most cases the reported results concern doping levels.

The goals for adding Ge into SiC may vary from work to work though one can classify them as follow : i) to increase Ge content into SiC for forming ternary alloys, ii) to improve SiC crystalline quality and/or other intrinsic SiC properties, iii) to stabilize 3C-SiC polytype, or iv) simply to study Ge incorporation mechanism and/or kinetics. Note that objective i) is more or less always superimposed to all other objectives since device engineers would dream of effective SiC-based heterostructures, for instance for bandgap engineering or better metal oxide semiconductor (MOS) properties, which would complement or even compete with actual state of the art SiC device performances. It was even calculated that several at% of Ge (but also Sn or Pb [19]) inside 3C-SiC would lead to direct bandgap material [22] and thus to new potential applications. In a more moderate incorporation level, Ge incorporation into SiC is close to industry application as can be seen from a very recent patent From Cree Inc. on strain compensation effect [23] as will be discussed later.

Addition of germanium element during SiC crystal growth was studied for various polytypes (3C, 4H, 6H) and using different growth techniques. We will separate the cases of hexagonal and cubic polytypes since the latter systematically requires heteroepitaxial growth due to the lack of adequate seed substrate, so that adding Ge for 3C-SiC growth is substantially different. Also, since this review concerns exclusively SiC material, we shall consider only the case of Ge-poor SiGeC alloys (also better noted as $Si_{1-x}Ge_XC$) which problematics are close to SiC material ones. The extreme other case of C-poor SiGeC alloys (noted $Si_{1-x-y}Ge_xC_y$ and already mentioned above will not be addressed further due

to the fact that it deals more with carbon incorporation into $S_{1-x}Ge_x$ alloys, which is a specific topic by itself.

As said earlier, the reasons for adding Ge into SiC or complementing SiC with Ge are rather disperse. This is probably the reason why no review was published yet on this topic. We will show that by comparing these different works, one can better extract the lesson learnt on this system and thus better see some potentialities. But before going further into the experimental results of the literature, the Ge-Si-C chemical system has to be presented for better understanding the related discussions.

2- The Ge-SiC chemical system

There are very limited published data on the Ge-Si-C ternary phase diagram despite early attempts in the late 50's [24,25]. It can be drawn after thermodynamic calculations using the various data which can be found in the related chemical systems. This was performed with Thermocalc software using the data from (i) the review by Durand and Duby [26] for the Si–C binary system; (ii) the experimental work of Scace et al. [27] for Ge–C; (iii) the value given by Olesinski and Abbaschian [28] for the nearly ideal liquid Ge–Si solution; (iv) the assessment of Du and co-worjers [29] for the Gibbs energy of formation for silicon carbide and (v) the classic Dinsdale reference [30] for the Gibbs energy variation for the melting of graphite. Figure 1 shows the resulting isothermal section cut at 1300°C calculated for this Ge-Si-C system. It clearly shows that the only stable carbide is SiC and it can form on the complete compositional range. $Si_{1-x}Ge_x$ alloys are the only other solid compounds which can form in this system (note that they will disappear above Si melting point, see the Si-Ge phase diagram below).

The absence of other carbide(s) is due to the fact that Ge and C atoms are essentially not compatible: Ge-C bonding is thermodynamically unfavorable (the calculated energy of formation of GeC alloy is positive: 0.435 eV/atom [31]) while carbon solubility in liquid Ge is extremely low (~$1x10^{-14}$ at% near Ge melting point (934°C) [27]). The growth of some Ge-rich Ge_xC_{1-x} alloys are sometimes reported but this almost always refer to amorphous material (see for instance [32,33]. As a matter of fact, any Ge-containing carbide with a C concentration above the bulk solubility is thermodynamically metastable.

Concerning the other elemental solubilities in the Ge-Si-C system, carbon has also a relatively low solubility in liquid Si near the melting point (~$3x10^{-4}$ at% at 1414°C [26]) while the experimental values of Ge solubility in SiC are a bit higher, with data ranging from mid-10^{18} at.cm^{-3} at 1500°C [34] to few 10^{20} at.cm^{-3} close to 2300 ˚C [20]. This point will be further discussed later. In conclusion, SiGeC ternary alloys fundamentally thermodynamically unstable. This is confirmed by theoretical studies showing that disordered cubic $Si_{1-x-y}Ge_xC_y$ alloys have positive values of excess energy over the entire concentration range even if some alloy ordering may reduce this excess energy [35] up to allowing thermodynamic stability for $Si_{0.75}Ge_{0.25}C$ composition [36]. But the latter point was never confirmed experimentally.

Another thermodynamic aspect of interest for this review is the Ge-Si binary phase diagram (figure 2) which has to be considered for instance in the implementation of liquid phase growth of SiC from Ge-Si liquid, as discussed later. It displays a spindle shaped evolution over the entire compositional range

in linked with the full solubility of both elements under the solid and liquid states. One can notice also systematic liquid phase formation above Si melting temperature.

Ge reactivity with SiC is very limited or even inexistent below Ge melting point. Under liquid phase, Ge slightly reacts with SiC by dissolving it despite the difference in solubility between Si and C in liquid Ge. This can be better seen in figure 3 representing the Ge-rich corner of figure 1. When pure liquid Ge is in contact with SiC, it will dissolve it for reaching an equilibrium state. Doing this, the liquid composition will first go from point A (pure Ge) to B at which point it will be saturated in C. But since the liquid has not reached its Si solubility limit, it will continue dissolving SiC until it reaches point X (~1 at% Si). This will lead to large C excess in the liquid, much above it solubility limit so that C may precipitate under graphite-like form. Of course, SiC dissolution by liquid Ge is thermally activated and is thus accelerated with increasing temperature. Note that the general shape of figure 3 does not evolve remarkably with temperature but only the position of the X point and of the respective solubilities in liquid Ge varies with temperature.

3- From Ge doping of α-SiC to Ge-poor Si-C:Ge alloys

3.1 Ge incorporation at the equilibrium

Doping of SiC is known to follow the site competition rule saying that the covalent radii of impurities will impose their incorporation site, i.e. either Si or C atomic site into SiC matrix. Ge is a big atom with a covalent radius (120 pm) bigger than both Si (110 pm) and C (76 pm) ones. It should thus incorporate on the bigger site, i.e. Si site, despite the fact it implies the formation of Ge-C bonds which are not very strong. All the simulations performed on the subject agree on the fact that it is more energetically favorable for Ge to site on Si (Ge_{Si}) site than on C site (Ge_C) [38-40]. This is illustrated in Figure 4 which shows that [Ge_{Si}] occurrence in SiC lattice is calculated to be more than five orders of magnitude higher than [Ge_C] one. This graph shows also that thermodynamic Ge_{Si} solid solubility into SiC increases with increasing temperature from few 10^{17} at.cm^{-3} at 700°C to almost $1x10^{21}$ at.cm^{-3} at 2700°C. Experimental results have confirmed that Ge incorporates on Si site [34] even if the obtained evolutions of Ge incorporation with temperature do not follow the theoretical one (see for instance graph 5 shown later). The discrepancies most probably arise from kinetic effects inherent to the growth methods used. In overall, Ge solubility in SiC is rather limited and this should be the combined consequence of the ~10% bigger covalent radius of Ge compared to Si one and the low stability of Ge-C bonding.

3.2 Ge incorporation during SiC epitaxial growth

Using the two most popular techniques for growing crystalline α-SiC material, i.e. PVT and CVD, Ge incorporation was found in the 10^{17} - 10^{18} at.cm^{-3} range using CVD while it raised to few 10^{20} at.cm^{-3} with sublimation at ~2300 ˚C (see figure 5). This has to be compared with SiC atomic concentration of $4.75x10^{22}$ at.cm^{-3} meaning that even the highest Ge doping achieved with PVT is < 1at%. Note that CVD results show a clear decrease of [Ge] with increasing temperature so that one cannot expect to reach the PVT values just by increasing CVD temperature. The CVD trend was explained by enhanced Ge desorption from the growing surface at high temperature. This high desorption/evaporation of Ge led also to fast depletion of this element from the source during PVT growth and thus to Ge

incorporation decrease with time, from $1x10^{20}$ to $2x10^{19}$ at.cm^{-3} at the beginning and the end of the growth respectively [41]. Note that this highest value of $1x10^{20}$ at.cm^{-3} for [Ge] at the beginning of the PVT growth is similar to the one reported by other authors using the same technique [20] and also very close to the calculated Ge solubility limit (on Si site) at the same temperature [39]. This suggests that the material grown by PVT can reach this solubility limit. On the other hand, CVD values of Ge incorporation are one to two orders of magnitude below the theoretical ones probably due to the kinetics limitations discussed earlier. As a consequence, even for the highest reported values, [Ge] concentration into CVD and PVT grown α-SiC crystals is low enough so that such material can still be considered as Ge-doped SiC and not as a ternary alloy.

On the crystal growth conditions point of view, adding Ge element to the system chemistry has some impact on the resulting material. For instance by PVT, for which the amount of incorporated Ge is the highest, Ge seems to lead to 15R-SiC polytype stabilization at the expense of 6H-SiC [41,42]. This effect looks reversible when Ge content in the crystal decreases. Note that 15R stabilization by Ge may not be only the result of its incorporation inside SiC crystal but it could also be the consequence of the changes of physico-chemistry inside the sublimation chamber. Ge presence inside the source SiC powder may change its sublimation rate or modify the relative concentrations of the sublimed species. This can change the local supersaturation, the growth rate and/or the C/Si ratio in the vapor. All these parameters are known to affect polytype stability [43-45]. In particular, 15R polytype transient appearance during PVT was already reported by other researchers but without adding Ge [46,47] so that more statistical studies are required for confirming the real effect of Ge during sublimation growth.

In the case of 4H-SiC homoepitaxy by CVD, no effect of Ge addition on layer polytype was observed, except for the classical fight against 3C-SiC formation due to surface defect and/or too low a deposition temperature [34]. The same study showed that Ge incorporation during CVD is independent on various crystallographic aspects of the substrate (and thus of the grown layer) such as polarity, off-orientation and polytype. Despite incorporating on Si site, [Ge] was also found independent on injected C/Si ratio (Fig. 6a). To have a better insight on Ge incorporation mechanism in 4H-SiC, it is worth comparing with Al impurity case, atom which is also sitting on Si site and which incorporation is more documented [48]. Al and Ge incorporation trends show similarities for temperature (See Figure 6b) and growth rate dependences which probably come from their intrinsic high-desorption/evaporation rate.

But they also differ in other aspects. For instance Al doping during CVD is known to generate memory effect (residual non-intentional incorporation coming from the release of Al atoms from reactor parts) while no memory effect was reported for Ge doping [34]. Another difference concerns the polarity dependence of Al incorporation which is known to be more pronounced on Si face than C face and to increase with C/Si ratio increase (Figure 6a), trends which have not been observed with Ge. This [Al] increase with increasing C/Si ratio was explained by the higher C-coverage of the surface which stabilizes Al atoms sitting on a Si vacancies by forming a fourth Al-C bond on Si face (see Fig. 7). Obviously the experimental results suggest that such mechanism does not seem to stand for Ge. We hypothesize that, due to weaker Ge-C bond as compared to Al-C one (Al_4C_3 compound has negative energy of formation, -0.092 eV/atom [49], while GeC one is largely positive [31]), forming a transient additional Ge-C bond at high C/Si ratio is less probable than in Al case.

When comparing precursor flux dependence, one can see that both impurities display linear increase in incorporation with increasing precursor flux, though with different slopes. (Figure 8). But to have a deeper insight on the incorporation mechanism, one needs to compare the effective incorporation yields. Such comparison can only be done if similar growth conditions (reactor type, geometry, temperature, pressure, C/Si ratio) are used. Using data from ref [34] and [52], which were obtained using exactly the same apparatus, this incorporation yield Y can be calculated as follow:

$$Y_X = \frac{[X]_{SiC}}{F_X \, x \, G_R} \qquad \text{Eq(1)}$$

Where X is the impurity considered, $[X]_{SiC}$ its concentration into SiC after growth (in at%), F_X the gaseous flux of the related X precursor during growth and G_R the SiC growth rate. Due to the fact that the experimental results were obtained for different G_R, i.e. 2.5 and 6 µm/h for Al and Ge impurity respectively, the yield is divided by G_R to mitigate the possible growth rate dependence. The calculated incorporation yields from Eq(1) for Al and Ge as a function of precursor flux are added in figure 8. Firstly, one can see that Y_{Al} is one order of magnitude higher than Y_{Ge}. Secondly, Y_{Al} increases with Trimethylaluminum (TMA) flux increase while Y_{Ge} is constant as a function of GeH_4 flux. Data on vapor pressure of pure Al and Ge elements [53] suggest that Al should be more volatile than Ge at the growth temperature. As a matter of fact, some Ge remaining droplets were often found after Ge doping experiments [34] while this was never observed for Al case. However, yield difference between Ge and Al shown in Fig. 8 cannot be attributed to the vaporization rate of these elements since $Y_{Al} > Y_{Ge}$. It should be thus related to the way these atoms incorporate into SiC. Al and Ge atoms have similar covalent radii (0.18 and 0.22 nm respectively) so that this parameter should not play a major role. More probably, the difference of incorporation yields between these elements should be due to the chemical bonding they form within SiC lattice: Ge forms weak Ge-C bonds while Al forms stronger ones as discussed above. Interestingly Y_{Ge} does not evolve with precursor flux while Y_{Al} display a clear increase with increase TMA flux. This may be related to the fact that each TMA brings three C atoms so that it can modify the local C/Si ratio which is known to lead to higher Al incorporation as shown in Fig. 6. In the case of Ge, the growth chemistry is not modified by GeH_4 precursor so that Y_{Ge} should not evolve with precursor flux.

Another aspect related to the system chemistry is the possible formation of Ge-containing phase. According to the phase diagrams, only Ge-containing liquid phases can form above Si melting point. Indeed, as discussed above Ge segregation at the surface under the form of droplets was often observed after atmospheric pressure CVD [34]. These droplets were pure Ge meaning that they did not dissolve significant Si despite being in contact with SiC and with SiH_4 precursor. The growth kinetics seems to be largely favorable to SiC formation so that all Si atoms are consumed to form Si-C bonds. These Ge droplets did not deteriorate SiC crystalline quality but slightly roughened the surface morphology by forming shallow circular depression after Ge wet etching [54]. We will see later that these Ge droplets can help for the growth of 3C-SiC on α-SiC substrate. One way to get rid of these droplets is to use low pressure conditions during growth in order to enhance Ge evaporation. This is probably the reason why Li et al did not observe such Ge droplets despite rather high GeH_4 flux [55].

3.3 Increasing Ge incorporation

If one wants to go beyond thermodynamic Ge solubility limit and elaborate crystalline Ge-poor α-SiC:Ge ternary alloy, then elaboration techniques limiting the kinetics restrictions discussed above should be used, such as MBE or ion implantation. MBE is rarely used for growing homoepitaxial α-SiC layers [56,57]. This is partly due to temperature limitations but also because it cannot compete with the performances obtained by CVD in terms of e.g. growth rate or purity. The temperature limitation has a direct impact on SiC polytype which can be grown by MBE so that 3C-SiC is most commonly obtained using this technique [58,59]. And this is what is happening when adding Ge to SiC growth by MBE [39,60]. The sticking coefficients and surface reactivities being very different between these elements, the growth procedure is rather complex and requires several cycles of elemental exposures followed or not by some annealing. The resulting material is indeed cubic $Si_{1-x}Ge_xC$ with $x \leq$ few at%. The Ge content was found to decrease with increasing temperature due to excess re-evaporation from the surface [39], like in CVD case. Analogously to the usually grown 3C-SiC on α-SiC, the ternary $Si_{1-x}Ge_xC$ alloys are highly twinned and contain a high density of other extended defects like stacking faults or dislocations. Note that one cannot argue the stabilization of 3C-SiC by adding Ge since the MBE growth conditions (low temperatures) used cannot lead to other polytype growth than 3C-SiC.

Ion implantation can retain the hexagonal polytype while allowing high Ge incorporation into SiC. As a matter of fact, ternary alloys with few at% Ge up to 2.5 at% on lattice site could be obtained in this way without losing the 4H-SiC matrix polytype [61,65]. Various conditions of Ge ions implantation were studied, which are summarized in Table 1. Due to the high atomic number of Ge element, one needs to anticipate the generation of defects up to possible amorphization of implanted SiC matrix. That is why the high-dose implantations are generally performed under sample heating in the 600-1000°C range. According to [62], SiC amorphization can be avoided for sample temperature > 300°C. Note the works of [64,65] reporting no real amorphization but only SiC crystal degradation despite room temperature implantation of very high doses. Unfortunately, no direct observation by TEM was performed so that one can imagine that the implanted material could be partially amorphized.

High temperature annealing of the implanted samples is generally performed in order to heal the material. It allows only partial recovery of the implantation generated defects [61,62]. Ge clusters formation was sometimes reported [66,68] though in most cases the resulting material was strained SiGeC alloy [63]. The strain is generated by the incorporation of big Ge atoms on SiC lattice sites. According to [61], Ge can incorporate on both Si and C site after implantation and annealing despite the fact that C site is energetically less favorable. This is probably the result of the out-of-equilibrium conditions inherent to ion implantation technique while for closer to equilibrium conditions (PVT, CVD) Ge stays on Si site.

In order to study in more details the defects generated by Ge implantation into the 4H-SiC matrix, low dose Ge implantations were performed, corresponding to doping-like incorporations of $1x10^{15}$ to $1x10^{17}$ at.cm^{-3}, see Table 1. By comparing with Ar implanted samples (with implant conditions calculated for producing similar amount of defects), it was found that Ge implantation is much less detrimental than Ar one. For instance, Ar implanted 4H-SiC layers easily turned semi-insulating while Ge implanted ones remained n-type doped at the same doping level as before implantation. Also, Deep level transient spectroscopy (DLTS) measurements on these samples showed the presence of four points defects: the well-known $Z_{1/2}$ center generally attributed to C vacancies (V_C) and three unknown ones, named GID1, 2 and 3 located respectively at 180, 390 and 490K on DLTS spectra [40].

See Table 2 for the energies associated with these defects. Surprisingly, $Z_{1/2}$ defects concentration was found to decrease with increasing Ge implantation while the reverse is usually observed, as seen with the Ar implanted samples trend.

On the other hand, GID defects density were found to increase with Ge dose increase, which suggests that these defects could be Ge-related. It might also suggest a correlation between one of these GID defects and $Z_{1/2}$ centers. Ge_{Si}-V_C complex (Ge located on Si site and associated with a V_C) was proposed as possible candidate for GID2 and its electronic structure and abundance were calculated by hybrid density functional theory (DFT) [40]. However, Ge_{Si}-V_C theoretical equilibrium concentration was found several orders of magnitude lower than that of V_C so that interaction between these point defects was suggested to be unlikely even if one can argue that ion implantation is by essence far from thermodynamic equilibrium. It was thus proposed that the observed reduction of $Z_{1/2}$ defects with increasing Ge dose could be linked to kinetic mechanisms and more specifically to the kinetics of Ge in 4H-SiC. Interestingly, these simulations show also that Ge sitting on Si site (Ge_{Si}) does not introduce any level in SiC bandgap while Ge sitting on C site (Ge_C) does. Note that implantation of another isoelectronic element (Sn) led to more or less identical results as for Ge which supports the idea that these effects could be specific to isoelectronic ions implantation.

4- Ge mediated 3C-SiC heteroepitaxial growth

As discussed previously, Ge addition to CVD or PVT growth systems does not lead to significant improvement of the crystalline quality of the homoepitaxial α-SiC material, which is already very high. This could be different in the case of 3C-SiC which is still looking for adequate substrate and/or growth process in order to attain sufficient quality for acceptable electronic device operation. In addition, 3C-SiC epitaxy requires lower growth temperatures than the hexagonal counterparts so that lower desorption of Ge atoms from the growing surface is expected and thus more impacts on growth.

Among the various substrates used for growing 3C-SiC, the most commonly studied are silicon and α-SiC. More details on the growth aspects and status of the 3C-SiC material grown on these substrates can be found in Refs [70-73]. However, germanium addition to these heteroepitaxial growth systems is only briefly mentioned in these papers despite several attempts. This will be done here by separating these two most used substrates.

4.1 Ge addition to 3C-SiC growth on Silicon

Most of the works dealing with Ge-mediated 3C-SiC growth on Si substrate concerns the modification of the SiC/Si interface by this bigger atom (Ge addition before growth) while those reporting on Ge addition during 3C-SiC growth are rather few. It is important to remind that 3C-SiC heteroepitaxial growth on Si is usually performed using a two-step process, i.e. Si surface conversion into SiC by carbonization (thermal treatment under a C source) followed by the SiC growth itself with the simultaneous supply of Si and C elements.

Let us first discuss the case of interface modification which was almost exclusively studied using MBE chambers. This could be performed either by doing the carbonization at the same time Ge is added or by pre-depositing few Ge monolayers on Si substrate before starting the carbonization process.

The former option was carried out using a single-source precursor for both Ge and C atoms, namely dimethylgermane (DMGe - $(CH_3)_2GeH_2$) [74,75]. In this way, the carbonization temperature could be reduced down to 650°C while keeping a smooth and monocrystalline SiC layer. Note that the proposed mechanism did not imply any effect of Ge atoms but only the low temperature delivering of CH_3 radicals by DMGe precursor. Since only the carbonization step was studied, it is thus difficult to estimate the gain of such approach in terms of crystalline quality or stress reduction. The reports on Ge pre-deposition before carbonization are more numerous. It is shown that Ge remains at the SiC/Si interface and/or in-diffuses inside the Si substrate [76,77]. It modifies SiC nucleation mechanism [78,79] and, for optimal Ge amount, leads to reduced residual stress inside the thin 3C-SiC layer, lower Si out-diffusion from the substrate and also reduction of other polytypes inclusions [80]. When CVD is used for thickening of such Ge-modified buffer layer, the stress evolves towards compressive while surface roughness increases [81]. Recently, Zimbone et al performed the 3C-SiC deposition by CVD on $Si_{1-x}Ge_x$ ($0 < x < 0.15$) epitaxial layers with well-defined composition instead of just Ge monolayers deposition [82]. This led to significant modifications of the growth procedure (lowering of the carbonization and CVD growth temperatures) in order to adapt for the new pseudo-substrate. The layers were found to easily switch to polycrystal except for a rather narrow operating window allowing slightly improved quality.

Some research groups have studied the addition of Ge (GeH_4 addition to CVD system) only during 3C-SiC growth (not before or during carbonization step). None of them obtained any ternary SiGeC alloy though some $Si_{1-x}Ge_x$ phase separation was detected together with 3C-SiC [83]. Some Ge was incorporated inside SiC at the dopant level but the exact concentration was not given [84]. In most cases, adding GeH_4 to the CVD growth recipe did not allow improving 3C-SiC material quality though it permitted obtaining epitaxial films down to 1000°C [85].

Altogether, the improvements brought by adding Ge to the 3C-SiC/Si heteroepitaxial system are rather limited and did not lead to any significant breakthrough in terms of 3C-SiC material quality so that this approach remained relatively marginal on such abundant research topic.

4.2 Ge addition to 3C-SiC growth on α-SiC

3C-SiC spontaneously forms on α-SiC substrate if conditions for replicating the polytype of the substrate are not fulfilled. It generally happens for too low growth temperature (usually < 1400°C) and/or low off-orientation of the substrate [73]. That is why the above discussed works about growth of $Si_{1-x}Ge_xC$ ternary alloys led to cubic polytype even on hexagonal SiC substrate. This was a side effect and not a target. But Ge was also used for stabilizing and/or improving 3C-SiC growth on α-SiC, and not for growing a ternary alloy. This was performed either using vapour-liquid-solid (VLS) mechanism or CVD. Both cases are described below.

VLS mechanism was implemented by melting Si and Ge pieces on top of a α-SiC substrate and then feeding it with propane [86]. By tuning melt composition and temperature, twin-free 3C-SiC thin layers can be reproducibly grown on a cm^2 scale [87] as illustrated in Fig. 9. The proposed mechanism involves a transient dissolution/precipitation process, occurring during the heating ramp and driven by the difference in C solubility inside Ge-varying Si-Ge melts [88]. This can be summarized in Fig. 3 by following the evolution of [C] inside Ge-rich liquid phase from point A to B then X. Upon passing the equilibrium line from *Liq = Liq + C* to *Liq = Liq + SiC*, the large C excess in the liquid will precipitate under the form of SiC. Such precipitation being very fast, it leads to the formation of 3C-SiC islands

even on α-SiC substrate, islands which are further enlarged upon feeding with propane. Note that Ge is not the only element, when added to Si, allowing such precipitation since Sn or Ga element were also shown to lead to similar twin-free 3C-SiC layers [87].

Ge atoms are obviously incorporated inside the 3C-SiC layers grown by VLS mechanism but the corresponding experimental data shows that Ge concentration is about one order of magnitude higher than with CVD. However, these data cannot be directly compared considering the fact they were grown with very different techniques. Indeed, the phase in direct contact with the growing surface is much Ge-richer using VLS than CVD so that incorporating more Ge with VLS is a rather logical result. Note that by extrapolating the CVD incorporation trend to lower temperatures (VLS growth range), one could expect incorporating similar Ge as with VLS technique. Interestingly, according to VLS results reported in Fig. 10, Ge-richer melts allows increasing Ge content inside the grown 3C-SiC layer.

This trend is better displayed in Fig. 11 which shows that incorporation as high as ~$1x10^{20}$ at.cm^{-3} (equivalent to PVT results) can be reached for 90 at% Ge inside the melt. Atomic location by channeling enhanced microanalysis (ALCHEMI) demonstrated that some of the Ge atoms in these VLS layers were occupying interstitial sites [89]. This was confirmed by careful investigations using transmission electron microscopy (TEM) which revealed that nanoscale interstitial clusters containing Ge atoms were present inside the 3C-SiC layers [90]. As a matter of fact, though VLS technique is leading to similar [Ge] as PVT but at much lower temperature, these incorporations cannot be compared since Ge atoms are not incorporated in the same manner.

Germanium was also used for eliminating the twin boundaries inside the 3C-SiC layers grown on α-SiC by CVD. This improvement was not obtained by adding GeH_4 during the growth [55] but before it, during the in-situ surface preparation step [91]. By proper tuning of this pre-treatment (temperature, GeH_4 flux and time), 3C-SiC nucleation and islands enlargement is modified, favoring one in-plane orientation of 3C-SiC among the two possible ones. The proposed mechanism implies an initial transient homoepitaxial growth mediated by the presence of Ge droplets on the surface. Such hoemoepitaxy provokes local enlargement of the steps by faceting and thus preferential 3C-SiC nucleation in these areas. In this way, self-selection of the 3C in-plane orientation is achieved by this step faceting induced nucleation. To some extent, this approach is comparable to the Ge pre-deposition before MBE heteroepitaxial growth of 3C-SiC on Si substrate discussed above: it essentially modifies SiC nucleation.

5- Improving SiC properties

Adding germanium inside SiC was always performed with the aim of improving the properties of the grown material and/or growing a new class of material (such as ternary compounds) with original properties. We will now see what are the added values of such Ge insertion into SiC.

5.1- Crystalline quality

Adding Ge inside α-SiC during homoepitaxial growth by CVD was not shown to significantly improve or degrade the crystalline quality of the material, probably because of the relative low amount of Ge incorporated. Using PVT, which allows higher Ge incorporation, some structural changes are reported such as 15R polytype stabilization, increase of the lattice constants or of the dislocations

density (see Table 3). Lower basal plane component in mixed type dislocations was also found for highly Ge-doped crystals [41]. As a matter of fact adding too much germanium can be detrimental to the crystalline quality.

But one can try turning into an advantage such lattice expansion, for instance towards bandgap and strain engineered SiC electronic devices [92] or as strain compensation in the case of compressed material. Indeed, it is known that highly N- or B- doped α-SiC has a smaller unit cell volume than undoped counterpart [93,94]. In the case of N, lattice shrinkage due to too high N incorporation is accompanied by stacking faults generation, either after growth [95] or after thermal annealing [96]. Co-doping of high N-doped 4H-SiC with Al atoms (known to increase SiC lattice) allows reduction of this crystalline degradation. But this gain in crystallinity is the positive aspect of a trade-off, the negative aspect being that the resulting material is highly compensated despite being still n type. As a matter of fact, replacing Al by Ge for the co-doping of highly N doped 4H-SiC should lead to the same crystallinity improvement without any electrical compensation since Ge is isoelectronic to SiC [23]. The final objective is to maintain a high crystalline quality even for highly doped materials in order to reduce the resistivity of the substrates which is requested for reducing the on-resistance of metal-oxide-semiconductor field-effect transistors (MOSFETs) made of 4H-SiC.

Adding Ge to liquid-based growth techniques leads also to some structural changes. Using VLS mechanism, it allows eliminating the twin defects commonly found in 3C-SiC layers grown on α-SiC, as discussed above. On the other hand, with the more commonly used top seeded solution growth (TSSG) technique and Si-Ge melt, some crystal improvements were also demonstrated such as micropipe filling [97] or surface roughness reduction [98]. However, the growth rates were low due to low C solubility in the Ge-based melts and high Ge evaporation at too high temperatures.

5.2 Electronic and optical properties

Theoretical calculations suggest that a high doping (in the few at% range) with isovalent impurity (Ge, Sn, Pb) can significantly modify both optical and electronic properties of 3C-SiC [19,22]. Both studies agree for the band gap becoming direct while its value would be marginally affected by Ge (Sn, Pb) incorporation. However, opposite trends are anticipated with either an increase [22] or a decrease [19] in optical absorption in the UV-visible spectral range. Unfortunately, there is no experimental data confirming one of these conclusions. The few experimental information on optical properties of Ge-doped 4H- or 3C-SiC material do not evidence any change as compared to undoped SiC. For instance, the Raman spectroscopy and low temperature photoluminescence spectra of Ge-doped 4H-SiC layer do not display any additional Ge-related peak [34]. Ge-related features were detected in the case of VLS-grown 3C-SiC layers but they were attributed to unwanted Si-Ge(-C) clusters forming inside the layers [90,99]. Such clustering was also present in some similarly grown Sn-doped 3C-SiC layers but they did not modify also the Raman spectra of the layers [21].

Concerning the electronic properties of Ge-doped SiC, it is predicted that numerous other direct and indirect transitions would appear close to the fundamental band gap, possibly resulting in greater efficiency of SiC:Ge devices over pure SiC ones [22]. But the experimental data suggest that modifying SiC electronic properties with Ge incorporation does not look as straightforward as for the crystalline properties. For instance, for highly doped crystals (~2 at% Ge in 4H-SiC using ion implantation), the resulting SiC/SiC:Ge devices displayed lowering of the forward drop, the contact resistance and the built in voltage [100,101]. With 0.34 at% Ge implantation into 4H-SiC, the

heterostructure bipolar transistors (HBT) displayed ~33% increase of gain (β) and of early voltage [64,102] as compared to homojunction bipolar junction transistors (BJT) fabricated without Ge. However, for similar highly Ge-doped crystals grown by PVT, ~15% reduction of the electron mobility was found [41]. Of course, it is tricky to compare results from differently obtained Ge-doped materials, since both elaboration approaches (PVT and ion implantation) is affecting differently the crystal structure either by generating point and extended defects and/or by expanding the crystal lattice.

In the case of lower Ge-doped SiC material obtained by CVD, inconsistent results about electronic properties can also be found in the literature. On one hand, more than 50% increase in electron mobility and conductivity was measured for a Ge-doped layer as compared to an undoped one [103]. This Ge doping did not seem to affect the quality of the SiO_2/SiC interface of MOS device [94]. On the other hand, these positive results were counterbalanced by a later study which did not detect significant difference on merged PiN-Schottky diodes and Trench MOSFETs performance with or without Ge-doping in the active layer [104]. Note that, even if all these studies refer to CVD grown materials, they were not grown using exactly the same conditions. For instance, the positive results were obtained from 4H-SiC layers grown using vertical cold-wall reactor under atmospheric pressure while the negative ones were from layers grown using horizontal hot-wall reactor under reduced pressure. These technical differences are known to impact the layer properties, and especially point defects generation such as $Z_{1/2}$ centers.

From ion implantation studies, the relation between $Z_{1/2}$ centers and Ge content was evidenced [40-67]. But the Ge-doped CVD layers with increased mobility discussed in ref [103] did not display any of these point defects due to the high C/Si ratio use for the epitaxy. In addition, concerning the PiN-Schottky diodes and Trench MOSFETs showing no improvement, no information was given about the $Z_{1/2}$ centers concentration inside the Ge-doped epitaxial layers [105] so that it is difficult to go further with the present interpretation. Wang et al suggested that, since Ge is sitting on Si site, the Ge-C bonds thus created are weak and easy to break under an applied electric field [106]. They suggest that this could generate free electrons and thus enhance the electronic properties. However, such bond breaking would mean that Ge sitting on Si-site provides a charge-transition level close to the conduction band but this is in contradiction with their own results reported in the same study and with the ones reported in [40]. As a matter of fact, the question of Ge doping benefit for electronic properties of SiC is still open.

6- Conclusion and Perspectives

Within the last three decades, germanium mediated growth and/or doping of SiC was regularly investigated using various techniques and for different polytypes. Both theoretical and experimental results agree that Ge atoms incorporate naturally on Si atomic sites and form thus thermodynamically weak Ge-C bonds. This probably limits the maximum amount of Ge that one can introduce inside SiC while performing in situ doping during crystal growth. There exists also kinetics limitation, the most effective being probably the relative high vaporization rate of this element at the temperatures used for PVT. Despite this, doping values as high as $2\text{-}3\text{x}10^{20}$ at.cm^{-3} were reported and which can be considered as the thermodynamic solid solubility limit of Ge inside SiC.

The experimental data of the literature, which refer to Ge doping of the most stable polytypes of SiC (3C, 4H and 6H), do not show any clear relation between Ge incorporation and SiC polytype, such as

Ge incorporation level dependent on SiC polytype or stabilization of a certain polytype with Ge. The only reported effect concerns a trend toward 15R-SiC transient stabilization with Ge doping during PVT growth but more experimental results are required for confirming it since such transient polytype switching was also reported without Ge doping. A number of results presented in this review suggest a link between Ge and 3C-SiC but the formation of 3C polytype is always related to the elaboration conditions and kinetic limitations (low temperature, silicon substrate or out-of-equilibrium nucleation) rather than Ge incorporation effect.

The massive incorporating of Ge atoms inside SiC lattice leads to lattice parameters increase because Ge atoms is bigger than Si one. This lattice increase seems to start for [Ge] > ~10^{19} at.cm^{-3}. By fighting against thermodynamics, it is possible to go beyond solid solubility limit and to form hexagonal $Si_{1-x}Ge_xC$ ternary alloys with [Ge] up to 2-3 at% by ion implantation in 4H-SiC. Of course, such massive implantation damages the SiC crystal and generates high amounts of defects which can be only partly healed by post-implantation annealing. Despite these defects, some improvements of the electrical properties were reported as compared to pure 4H-SiC. Lower Ge doped 4H-SiC layers, grown by CVD, were also found to display better electrical conductivity. However, contradictory results can also be found in the literature so that the enhancement of the electrical performances of Ge doped SiC-based devices is still questionable. At least it can be said that Ge incorporation inside SiC does not degrade the electronic properties of the material if gently incorporated below solid solubility. There seems to exist some links between G and point defects such as $Z_{1/2}$ centers but it requires more systematic study preferably on CVD grown samples rather than implanted ones to avoid generation of other defects which can shadow the real Ge effect. In overall, more work remains to be done for clarifying the real effect, if any, of Ge doping on the electronic properties of 4H-SiC.

The most directly useable effect of Ge doping is probably the possibility of strain compensation for highly N-doped material in order to improve crystalline quality of such material and reach higher conductivities. It essentially concerns bulk growth techniques since the first obvious application is to reduce electric losses occurring through current passing across the substrates. PVT technique, which is the present industry standard, needs to be adapted in order to avoid Ge impoverishment with time. One can thus imagine implementing an independent and stable Ge source inside the growth cavity, for instance in a similar manner as for Al or P doping during PVT [107-108]. Adding Ge to the Si-based melt for SiC growth by TSSG technique is an interesting alternative which looks simpler in a first glance but which would probably generate other difficulties linked to low C solubility or evaporation at high temperature. Note that any improvement of the bulk growth techniques toward massive and controlled Ge incorporation could also allow going beyond the actual Ge solubility limits into SiC, in closer to equilibrium conditions than when using ion implantation ones. This could lead to bulk-like high quality $Si_{1-x-y}Ge_xC_y$ alloys with possibly new and interesting properties for electronic applications.

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Figures

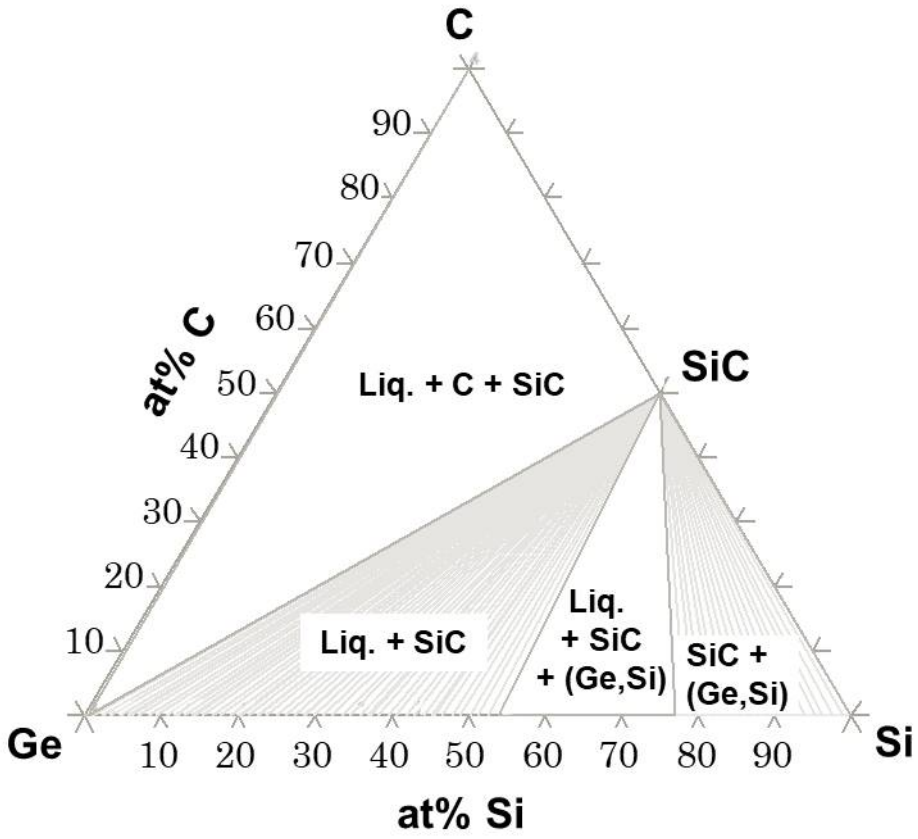

Figure 1: Isothermal section cut of the Ge-Si-C ternary phase diagram calculated for 1300°C and at atmospheric pressure

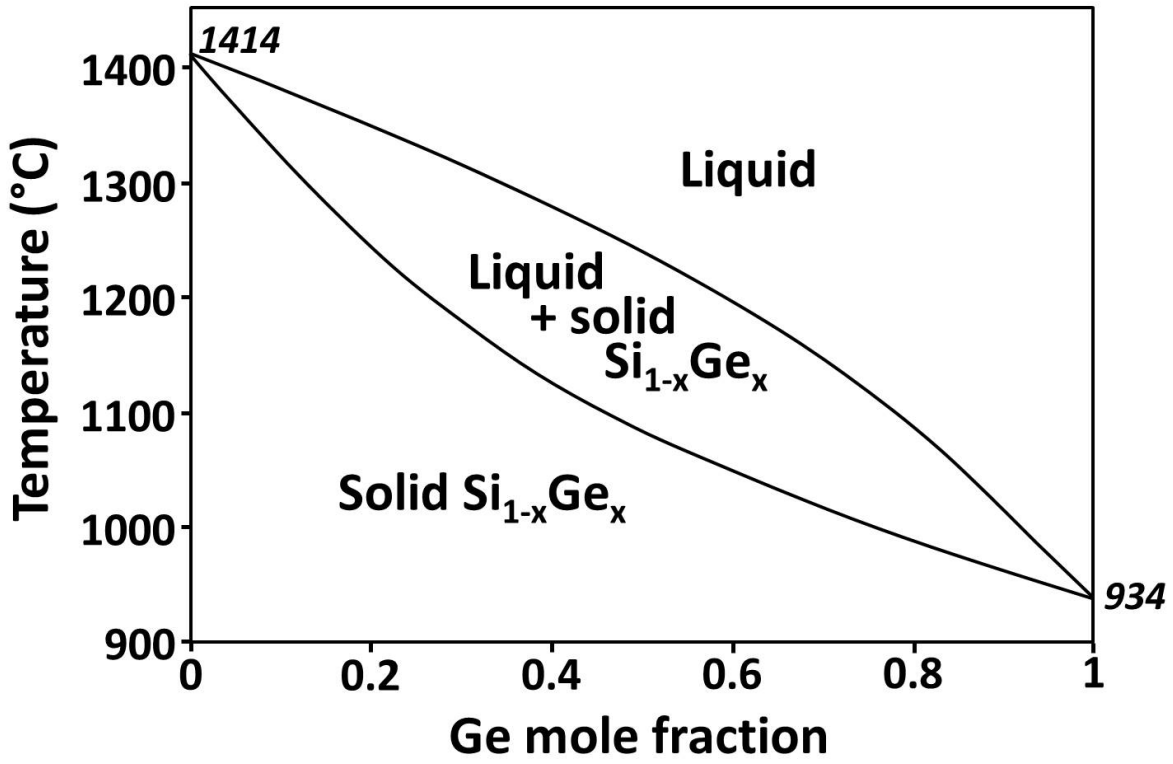

Figure 2 : Binary phase diagram of the Ge-Si system, redrawn from ref [37].

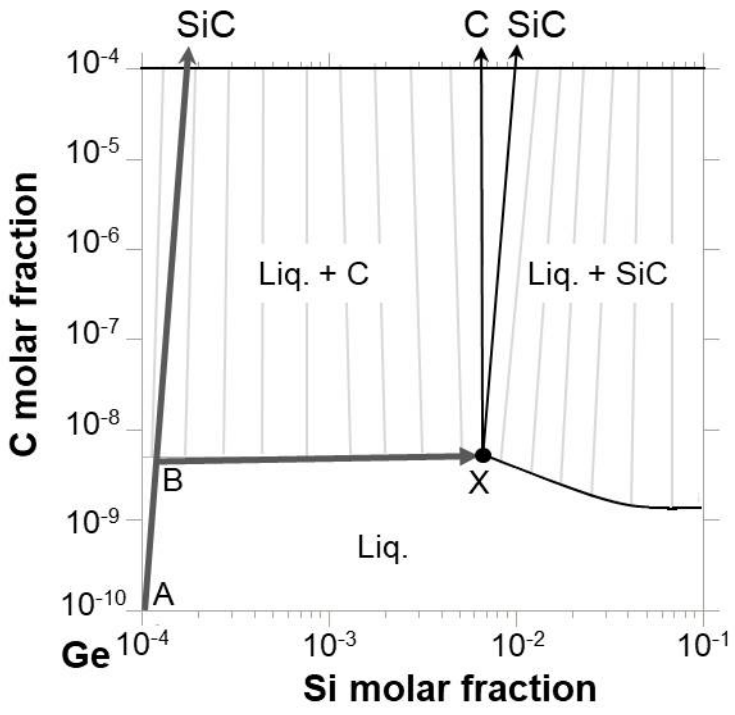

Figure 3: Representation (in log-log scale) of the Ge-rich corner of the isothermal cut shown in Fig. 1. Axes are drawn perpendicular for clarity reasons. Note the difference in magnitudes between the scales.

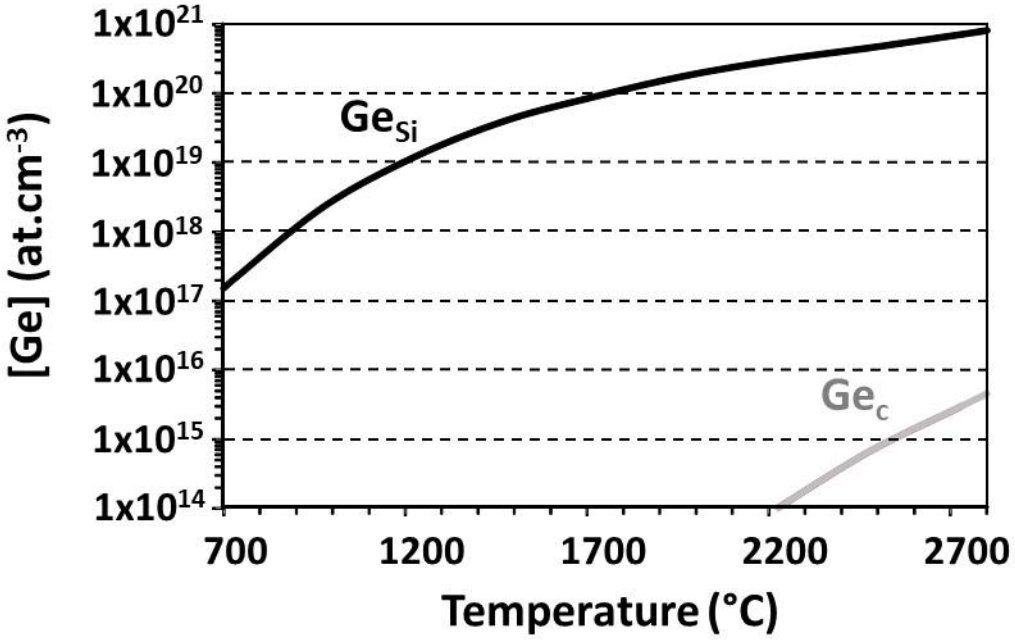

Figure 4: Calculated equilibrium solid solubility of Ge into SiC as a function of temperature for both Ge_{Si} and Ge_C incorporation cases, redrawn from ref [39].

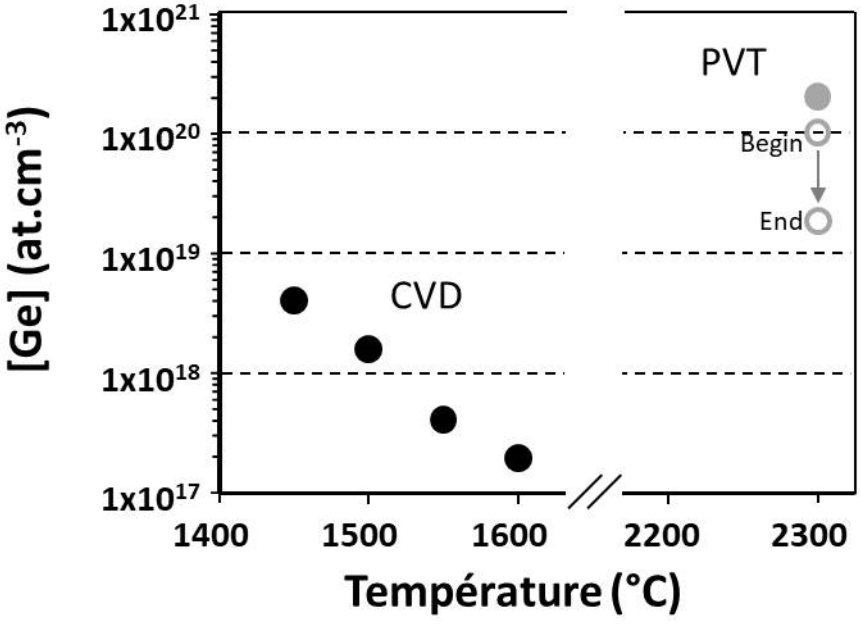

Figure 5: Evolution of Ge incorporation as a function SiC growth temperature. ● refers to CVD samples grown using a fixed GeH_4 flux of 0.02 sccm [34]. ● and ○ refer to PVT grown samples from [20] and [41] respectively

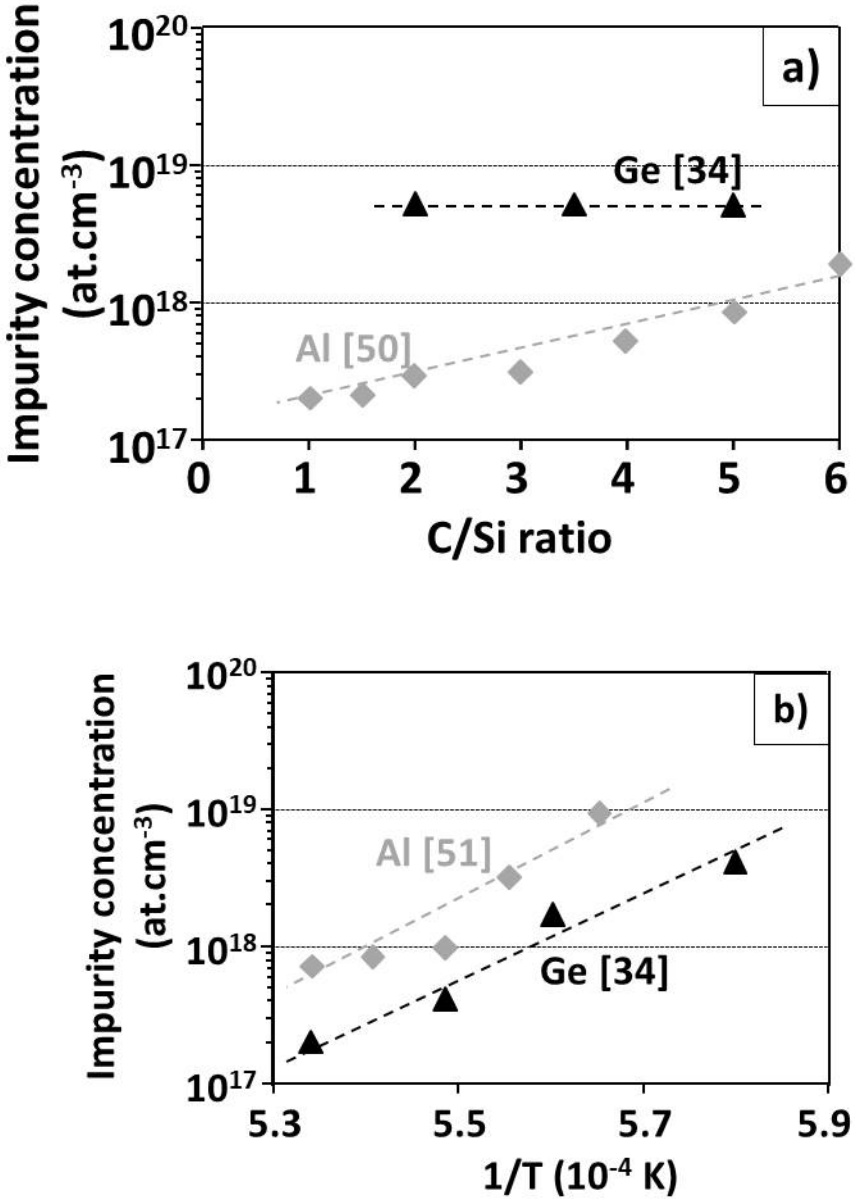

Figure 6: Comparison of Al and Ge incorporation trends inside 4H-SiC during CVD as function of a) C/Si ratio and b) temperature.

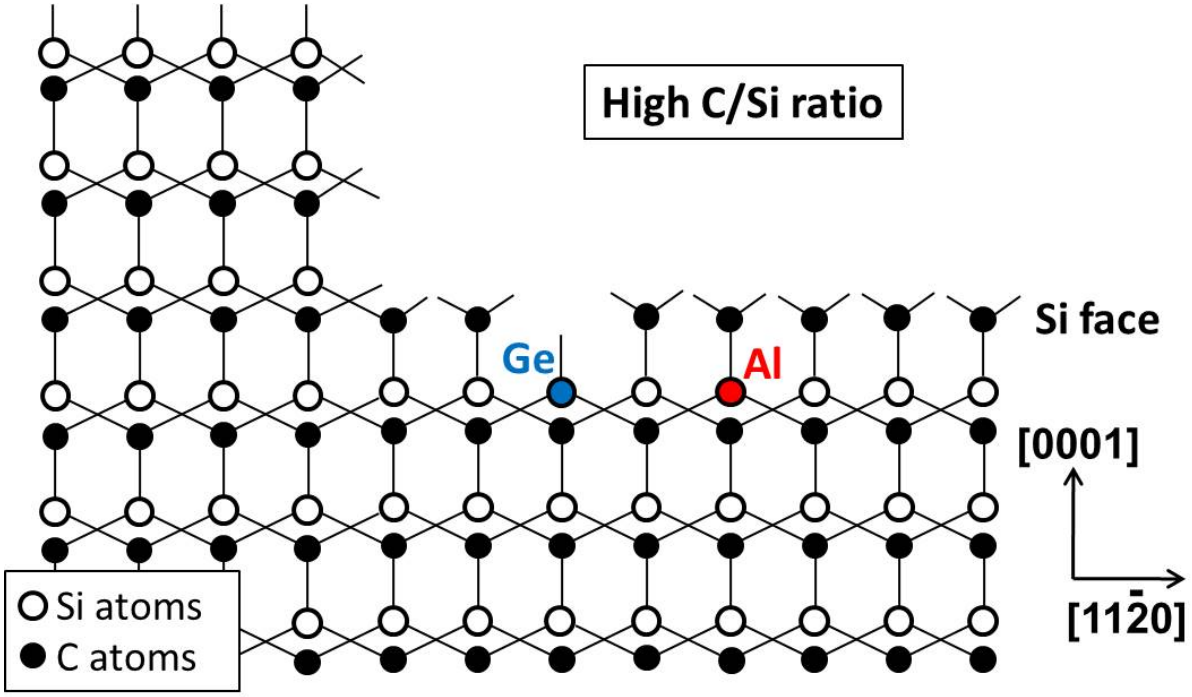

Figure 7 : Schematic representation of Al and Ge incorporation on Si-face 4H-SiC surface during CVD with high C/Si ratio.

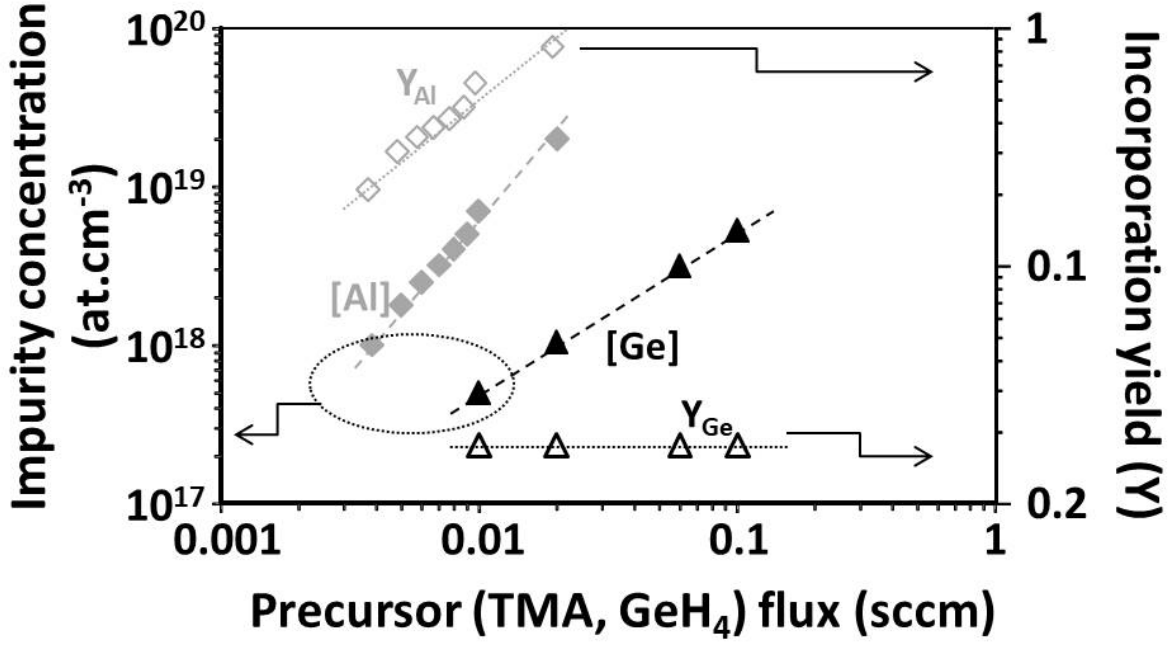

Figure 8: Evolution of Al and Ge impurity incorporation into 4H-SiC as a function of related precursor (TMA for Al and GeH_4 for Ge) during CVD. The growths were performed at 1500°C under atmospheric pressure.

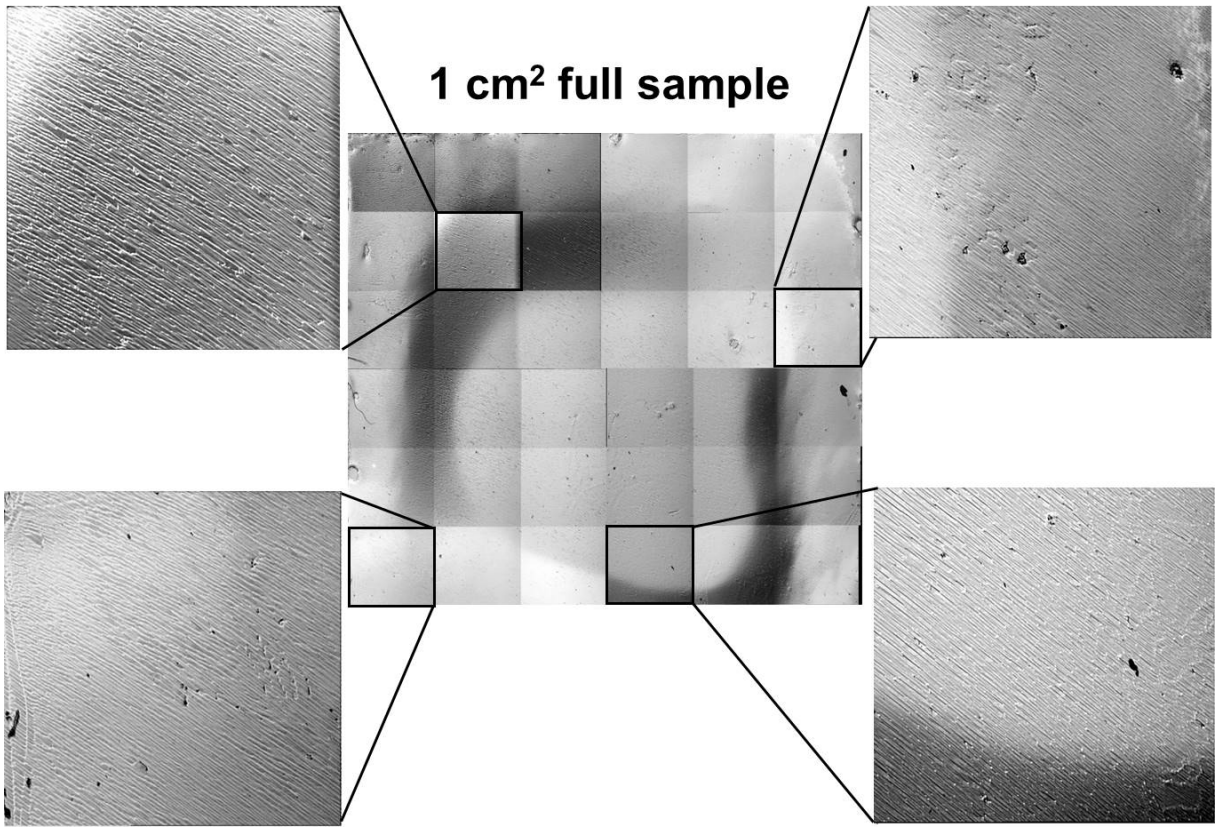

Figure 9: Surface morphology of a 1 cm x 1 cm sample fully covered by a VLS grown twin-free heteroepitaxial 3C-SiC layer on 6H-SiC(0001) on-axis substrate ($Ge_{50}Si_{50}$ melt composition, T = 1250°C). The central image was built from 36 images taken by optical microscopy at higher magnification The four lateral images are zooms of some areas showing that similar morphology is obtained on the entire wafer.

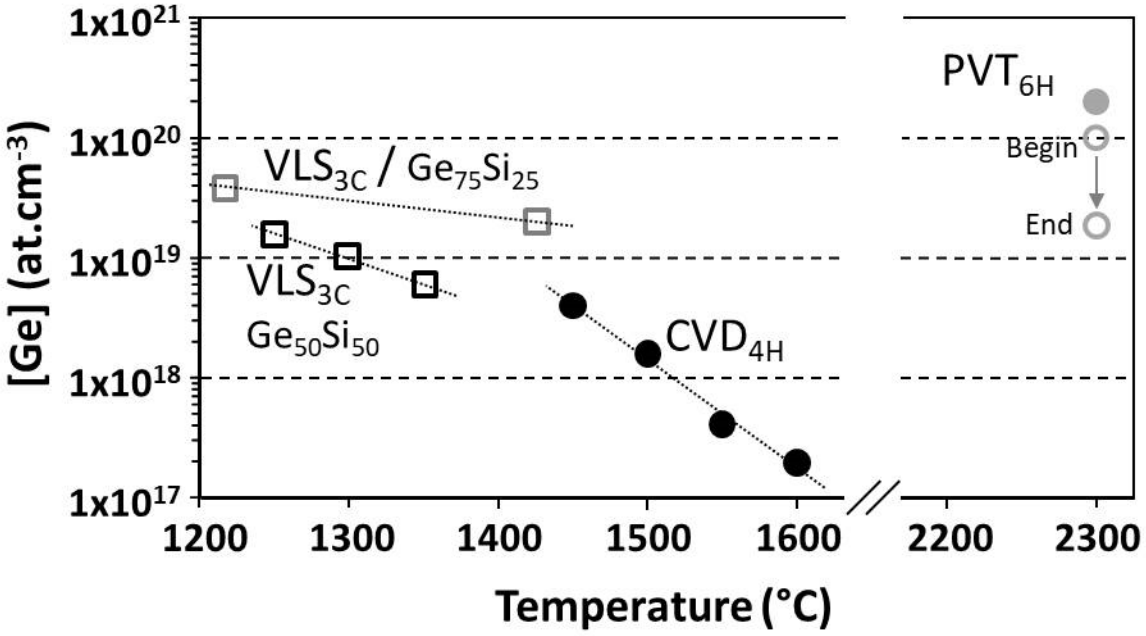

Figure 10: Same figure as Fig. 5 but with the addition Ge incorporation trends versus temperature for 3C-SiC VLS grown samples using 50 and 75 at% Ge inside the melt.

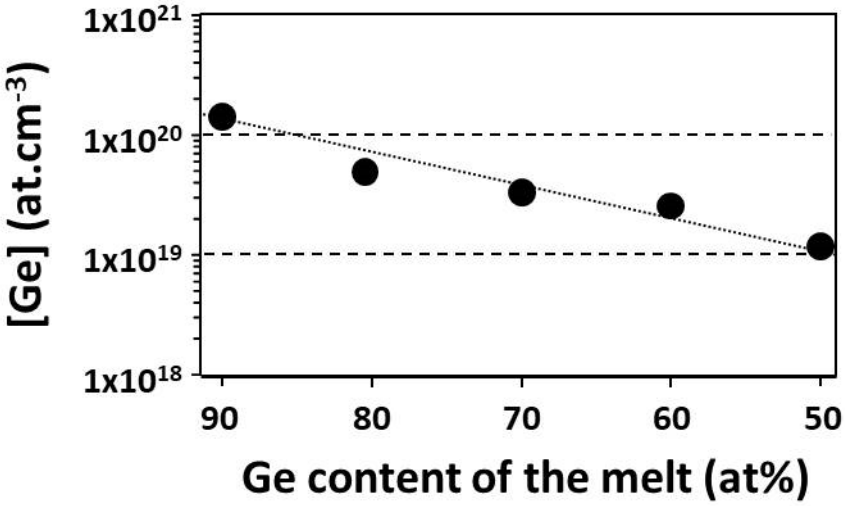

Figure 11: Effect of Ge content of the Ge-Si melt on [Ge] incorporated inside the 3C-SiC layers grown by VLS mechanism at 1300°C on 6H-SiC on-axis substrate.

Tables

Ge Implantation dose (cm^{-2})	Ge ion energy (keV)	Implantation temperature (°C)	[Ge]	Amorphisation	Annealing (°C)	Reference
$1x10^{16}$ $1x10^{14}$	500-800 500-800	700 RT	1 at% -	No Yes	1400-1600	[62]
$1x10^{16}$	250	RT – 700	1 at%	Yes at RT	1400-1600	[66]
1 to $6x10^{15}$ /	30-200	600	0.7-2.5 at%	No	1300	[61]
$2x10^{10}$ to $2x10^{12}$	-	RT	$1x10^{15}$ to $1x10^{17}$ $at.cm^{-3}$	No	1700	[67] [40]
0.3 to $5x10^{15}$	50-140	1000	0.074-1.25 at%	No	1250-1650	[63]
$1x10^{16}$	750	RT	0.34 at%	no	1050-1600	[64]
$2x10^{16}$	300	RT	1.2 at%	no	1000	[65]

Table 1: Experimental conditions used for Ge implantation into α-SiC.

	$Z_{1/2}$ (V_c) [69]	GID_1	GID_2	GID_3	Ge_{Si} (calc)	Ge_C (calc)	Ge_{Si}-V_c (calc)
Charge state	-2/0	?	?	?	-	+1/0	+2/+1 +1/+0 0/-1 -1/-2
Energy level (eV)	Ec – 0.59	Ec – 0.36	Ec – 0.79	Ec – 0.9	-	Ev + 0.45	Ev + 1.49 Ec – 1.56 Ec – 0.57 Ec – 0.31

Table 2: Energy levels of Ge-related defects in 4H-SiC; calc = calculated by DFT [40]

Lattice parameter	a (nm)	c (nm)	Dislocation density (cm^{-2})
Undoped 6H-SiC	0.3080469	1.51193	$2.9x10^4$
Ge-doped 6H-SiC	0.3080842 [41]	1.51317 [42]	$6x10^4$ [42]

Table3. Evolution of 6H-SiC crystal parameters with Ge doping.