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Redefining High-k Dielectric Materials Vision at Nanoscale for Energy Storage: A New Electrochemically Active Protection Barrier.

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Abstract

Dielectric materials have been used for decades for energy applications where their insulation and polarizability properties are critical. In the energy storage field, most material scientists envision high-k dielectric layers in contact with an active material only as an insulating passivation layer. In microelectronics, this concept has been modified with the study of dielectrics at nanoscale level revealing interesting properties scarcely known by other fields. We propose to reconsider the vision of high-k dielectric materials for energy at nanoscale specifically. Based on microelectronic measurement techniques and nanometric control of dielectric thickness by Atomic Layer Deposition (ALD), an ultra-thin pinhole-free alumina (Al_2O_3) layer on a silicon nanowire (Si NW) is shown to display thickness dependent tunneling electrical conduction. This result brings a new light on this material class in the energy field and allows original approaches toward achieving scientific leaps. As an illustrative application, a silicon based micro-supercapacitor (MSC) protected by 3 nm of alumina dielectric layer exhibits Electrical Double Layer Capacitance (EDLC) by means of tunneling current in aqueous electrolyte, an unprecedented result for this material, with outstanding lifetime capacity retaining 99% of its initial capacitance after 2 million cycles. Extended to multiple energy materials, such method could lead to notable progress.

Keywords: Energy Materials, Nanoscale Effects, High-k dielectrics, Tunneling Conduction, Electrochemical Energy Storage.

Abbreviations: (footnote first page)

ALD : Atomic layer deposition

Si NWs : silicon nanowires

Si NTs : silicon nanotrees

Al@SiNWs : alumina coated silicon nanowires

Al@SiNTs: alumina coated silicon nanotrees

3 nm Al@SiNWs : 3 nm alumina coated silicon nanowires

1. Introduction

Over the past few years the rise of the study and synthesis of well-known materials at the nanometric scale has opened a new world of possibilities for material scientists to be explored.^[1] Material properties, such as melting point, mechanical properties, chemical reactivity, electrical conductivity and biocompatibility can be tuned as a function of size to fit the scale of study.^[2-4] Specifically, nanoscopic phenomenon in which nano-sized objects do not follow principles of classical mechanics, have revealed interesting new features.^[5] For example, in metal science, a revolution is underway with the development of affordable additive manufacturing which has now become a viable option for mass production.^[6,7] This approach has naturally been applied to the energy storage field with nano-induced effects on ion absorption inside nanopores,^[8] nanostructuring of advanced electrodes for battery applications,^[9] and design of self-assembled nanocomposites for electrochemical energy storage.^[10]

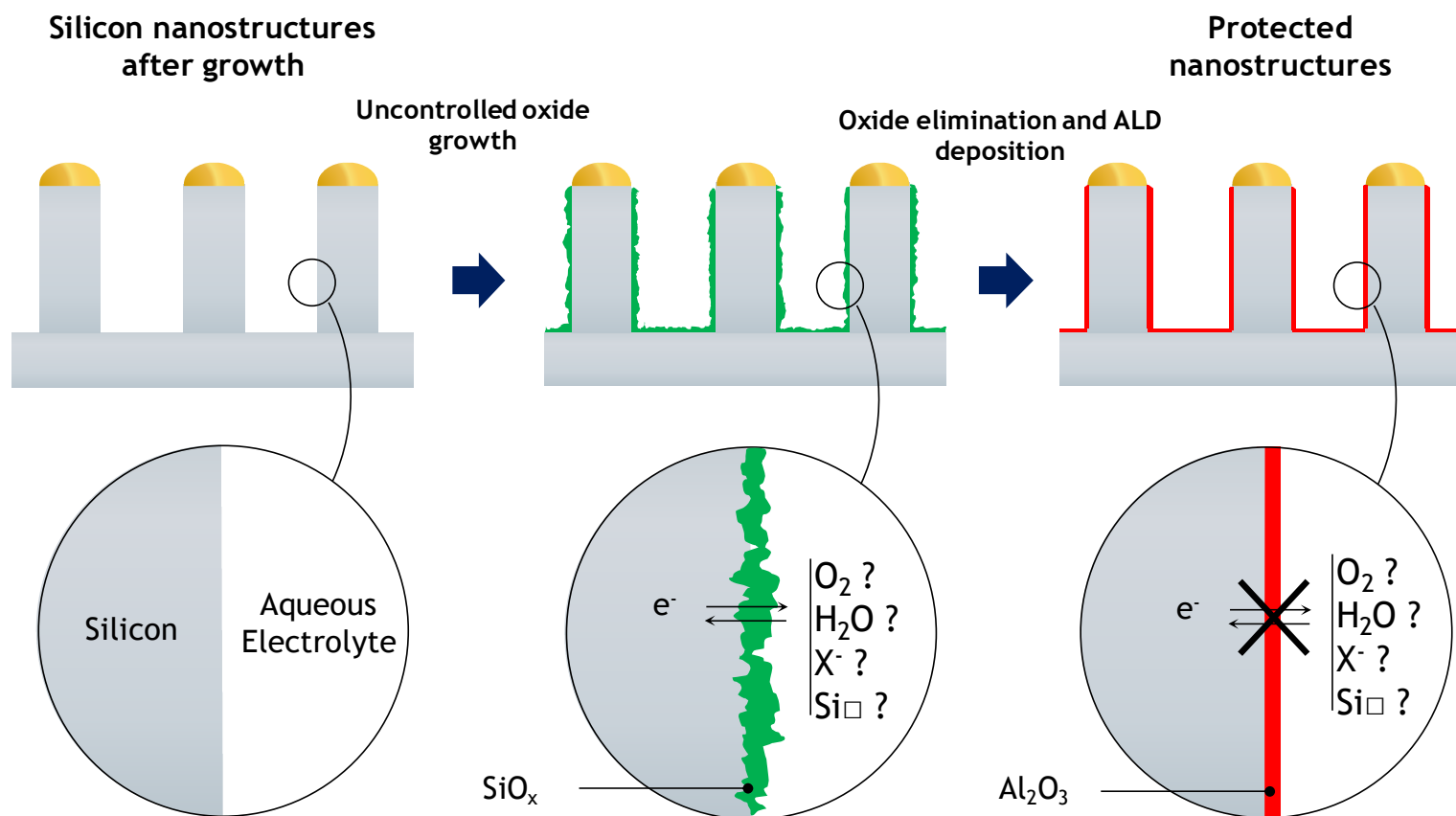
However, dielectric material vision in energy has not benefited from this shift. Even though multiple studies on dielectrics have been performed in the micro and nanoelectronics^[11] where the understanding of interface influence is critical for transistor applications,^[12] this knowledge has not been transferred and applied to the energy storage field. The microelectronic industry has developed expertise and processes which energy storage could highly benefit from but, still remain sparsely used. One of the reasons for the lack of

transition is the complexity of the solid/electrolyte interface requiring specific electrochemical expertise to adapt the existing tools.

High-k dielectrics have been widely used in energy storage as electrode separation layers in well-known electrolytic capacitors, ensuring an electrical insulation between them and thus creating the capacitance.^[13] This application has influenced the vision of scientists in the energy storage field to apprehend dielectrics only as insulating layers. In microelectronics however, while high-k dielectrics have also been used as an insulator between the gate and channel of transistors, tunneling electron conduction through dielectrics is well-known and even used for some applications. To mitigate the issue of gate leakage through thin dielectrics, oxides such as alumina are selected to maintain a high degree of electrostatic control on the channel while ensuring small levels of controlled gate current leakage.^[14] In this paper, we look to reframe this work for energy applications at the nanoscopic scale where thin high-k dielectric materials are able to exhibit specific features of high interest: A pin-hole free nanometric layer of alumina dielectric deposited by ALD, a rising tool for material scientists,^[15-17] protecting a silicon electrode material from oxidative media is shown to not be consistently insulating but rather have thickness dependent conduction properties via tunneling electron conduction.

Based on this result, a micro-supercapacitive application using the conduction phenomenon through a passivation dielectric layer is presented. Microsupercapacitors (MSCs) made of silicon nanostructures suffer from detrimental growth of native silicon oxide on electrode surfaces in aqueous media, a major weakness narrowing their potential applications. This uncontrolled oxidation does not allow them to operate using common aqueous electrolytes widely utilized with carbon or pseudocapacitive materials.^[18] Hence, for this supercapacitor material to be viable for many applications, it needs to be modified to be used with the environmentally harmless and inexpensive, yet so far unusable, aqueous electrolytes. The

coverage of the electrode nanostructures by an ultra-thin nanometric layer of dielectric alumina by ALD, as shown in **Scheme 1**, is investigated to overcome this problem.



Scheme 1. Substitution of the SiO_2 native oxide of silicon nanostructure by a nanometric layer of high-k dielectric alumina. The surface state of the supercapacitor electrode material is controlled to avoid parasite electrochemical reactions with the electrolyte detrimental to the capacitive performance.

This approach can easily be adapted to already existing electrode materials to diversify their application field. In this regard, amending the vision of dielectric materials at nanometric scale in the energy storage field, to be a protective but also conductive passivation layer instead of only an insulator layer for capacitor applications, is a way of progress towards advanced energy storage units.

2. Materials and Methods

2.1. Silicon Nanowires growth

Highly doped Si NWs were grown in an hot wall Chemical Vapor Deposition (CVD) reactor as growth chamber (EasyTube 3000 first Nano, CVD Equipment Corporation) based on the vapor-liquid-solid method (VLS) using silane precursor gas reactions with gold catalyst as defined by our co-workers.^[19,20] In operando donor doping of the nanostructure was performed by adding phosphine doping gas during material growth.

2.2. Fabrication of electrical contacts on a single isolated silicon nanowire:

The Al₂O₃ coating of highly n-doped Si NWs was carried out using trimethylaluminum (TMA) and H₂O as precursors in an Atomic Layer Deposition reactor (Fiji200). The deoxidized samples were placed in the deposition chamber under 250 °C, 10⁻² Torr, argon purge gas, and an automated thermal deposition recipe alternating 4 steps (0.06 s TMA, 8 s purge, 0.06 s H₂O, and 8 s purge) was performed until the desired thickness was reached. Samples were then sonicated in isopropanol and NWs were drop-casted onto a silicon substrate. Prior to the drop-cast, the substrate was prepared with a thermal SiO₂ layer and contact metal pads on top together with alignment markers made via a first level of e-beam lithography, metal deposition and lift off.

A first set of electrodes (10 nm Cr and 100 nm Au) was deposited on the Al₂O₃/Si NW via electron beam (e-beam) alignment using UV5 resist and lift off. A second set of electrodes was aligned and deposited nearby the first one via a second e-beam alignment step using ZEP 520A resist. This time, a slight exposure to hydrofluoric acid (HF) vapors was done prior to the metallization step (10 nm Cr and 100 nm Au) during approximately 20 seconds in order to remove the Al₂O₃ layer at the bottom of the resist trenches. Lift off of the metal deposited on the resist was performed consecutively.

The structure of the final microelectronic electrical characterization device can be found in **Figure 1.**

2.3. Electrical measurement method

Two probe I-V measurements are conducted by connecting one prober tip to a deoxidized contact and one to an Al₂O₃ contact, allowing probing one barrier at a time. Connected NWs are typically approximately 50 nm in diameter and 20 μm long. The width of the electrodes is 500 nm, and each gap between two neighboring electrodes is 1 μm. **Figure 1.** shows SEM inclined views of a series of contacts on a 5 nm alumina capped Si NW.

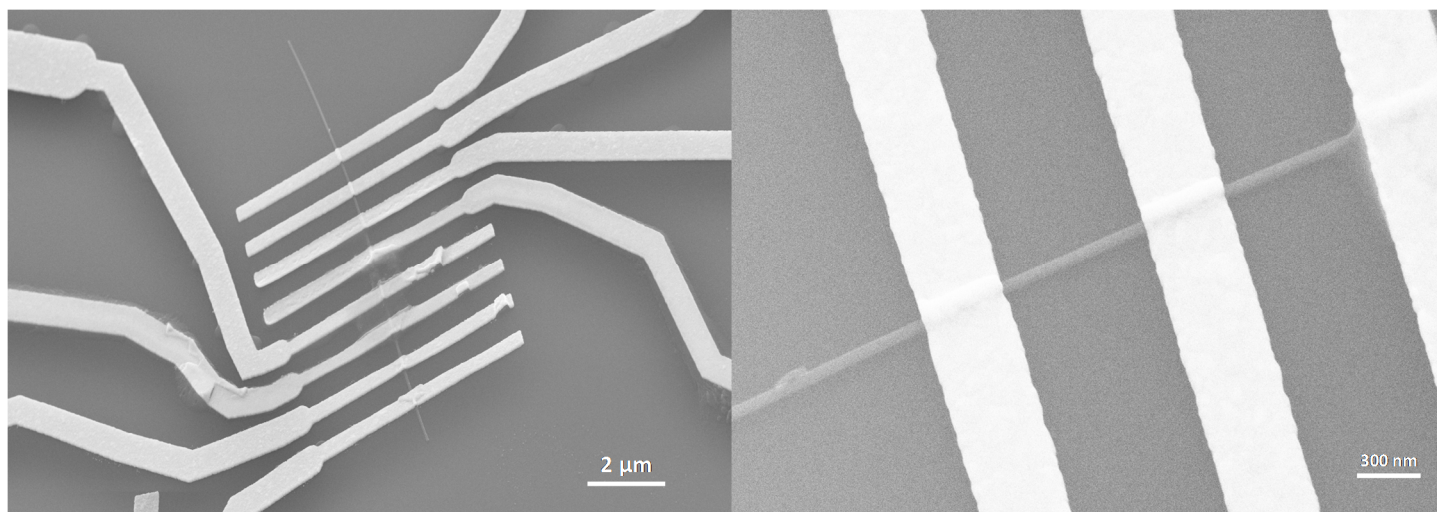


Figure 1. SEM Imaging of electrical contacts on a 5 nm alumina capped Si NW. Pictures acquired at an acceleration tension of 20kV.

2.4. Electrochemical measurements

All electrochemical measurements were carried out in an aqueous electrolyte of Na₂SO₄ 0.2 M electrolyte at room temperature. The electrochemical characterization tests were conducted with a potentiostat/galvanostat (VMP3, Biologic, France) equipped with a low current module for electrochemical impedance measurements.

The investigation of the microsupercapacitors coated with the nanometric alumina layer was performed in a commercial electrochemical cell (ECC cell, EL-CELL, Hamburg, Germany) in both three electrode and two electrode cell configuration. Three electrodes cell characterization was conducted using the silicon based sample (active area 1 cm²) as the working electrode, a 20 mm diameter circular YP50 black carbon counter electrode and a

platinum wire as pseudo-reference electrode. In order to ensure the reproducibility of the experiments, the platinum is washed using a 10% HNO₃ solution prior to measurements. Prior to any experiment, the platinum pseudo-reference electrode is calibrated using the voltammetric response of ferrocene redox couples in Na₂SO₄ 0.2 M using a Ag/AgCl reference electrode.

Two electrodes cell devices were assembled by sandwiching an Na₂SO₄ soaked Whatman n°41 paper separator between two symmetric silicon samples connected to a plunger made of 316L stainless steel.

The electrolyte is initially purified from oxygen using argon bubbling then injected inside each cell with a 1 mL syringe under the consistent basis of 300 μL for each test..

Cyclic voltammetry tests were conducted with various potential windows ranging from -0.7 to 0.2 V vs Ag/AgCl reference electrode at different scan rates (ranging from 50 mV.s⁻¹ to 1 V.s⁻¹). Thereafter, galvanostatic charge-discharge measurements were conducted at multiple current densities (ranging from 0.05 mA.cm⁻² to 1 mA.cm⁻², at a cell voltage of 0.7 V). Areal capacitance, energy and power densities were derived from the slope of the galvanostatic measurement taking into account the footprint of the MSC device (1 cm²).

Capacitance retention of the supercapacitor configuration was investigated through long-term galvanostatic charge-discharge tests at a current density of 0.5 mA.cm⁻².

All electrochemical characterizations were performed several times with samples from separate CVD and ALD batches using the same conditions, displaying a good reproducibility.

2.5. Electrochemical Impedance spectroscopy

2.5.1. Impedance measurements

Electrochemical Impedance spectroscopy measurements (EIS) were performed at open circuit voltage using 70 mV amplitude signals at frequencies ranging from 20 mHz to 200 kHz using a three electrode configuration.

Resistance (ESR) was estimated from the real part of the impedance at maximum frequency in EIS measurements. From the impedance spectra in three electrode cells, the time constant is easily derived by plotting the imaginary part of the impedance for the Si NTs depending on the Alumina thickness and determining the frequency of the impedance maxima for each specimen.

2.5.2. Impedance modelling

Impedance Modelling of electrical behaviour of the 3 nm alumina protected Si NTs is performed using a commercial impedance software (EC-Lab, Z-fit tool with Randomize + simplex method). An equivalent circuit modelling the electronic behaviour of the 3 nm alumina protected SiNTs given in **Figure 2**. was used. The impedance arrangement consists of a single vertical ladder network in series with an RC parallel network. The detailed description of the model are given in supporting information of this paper.

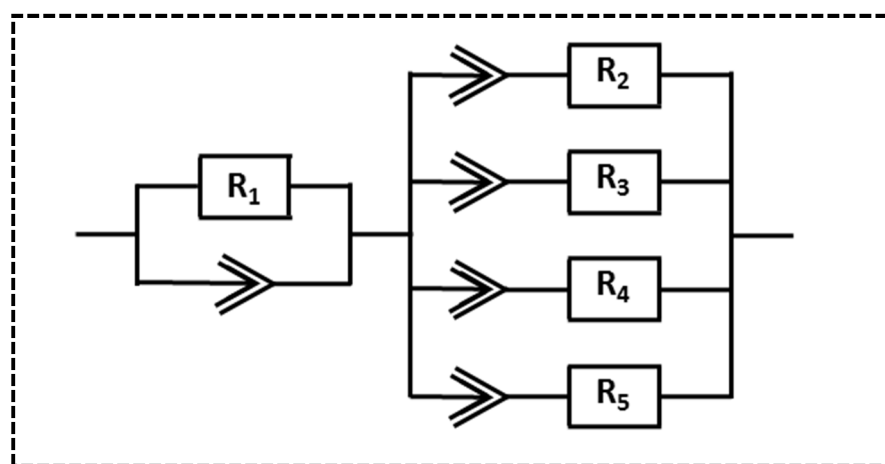


Figure 2. Equivalent circuit modelling the electronic behaviour of the 3nm protected Al@SiNTs micro-supercapacitor electrode. Fitting parameters and equivalent circuit constants are given in supporting information of this paper.

3. Results and Discussion

3.1. Dielectric electrical conductivity measurement

An electrical conductivity study was performed on a single silicon nanowire from a nanostructured micro-supercapacitor electrode to understand the behavior of the nanometric dielectric layer at different thicknesses. Highly doped Si NWs from a silicon “nanoforest”^[21] are randomly selected as representative samples to investigate their electrical behavior by electrical two probe I-V measurements following the work of our coworkers.^[22] One of the two contacts is deoxidized prior metallization making the I-V representative of the electrical probing of a single Al₂O₃ barrier. More information about electrical contact and fabrication process can be found in **Figure 3. b)** and supplementary information of this paper.

The **Figure 3. a)** shows the electric response of 1, 3 and 5 nm thick alumina layers. The 1 nm thick layer has a straight I-V (in the linear-linear scale), characteristic of ohmic behaviour. A similar behavior is observed with pristine nanowire having two deoxidized contacts in **Figure S1** of supplementary information with current values in the same range. Thus, the 1 nm dielectric barrier deposited by ALD is not conform, as expected foremost, but rather contains holes. This allows direct contact between the deposited metal and the highly doped Si NW, giving rise to the ohmic character of the electrical conduction observed in this sample. These defects can be explained by looking at the principle of the alumina deposition itself. The most common process used to deposit alumina by ALD is based on Trimethylaluminum and water precursors.^[23] The growth mode of alumina with this process on hydrogen-terminated silicon nanostructures surface after growth has been demonstrated to be of the island type until a continuous layer is formed.^[24] In island-growth, new material units are preferentially deposited on already ALD-grown material until the layer is completed, explaining the inhomogeneities of the surface coverage at the first growth stages. The alumina deposited by this process is porous until a thickness of roughly 1nm (where the growth mode becomes two dimensional) explaining the observed electrical behavior.

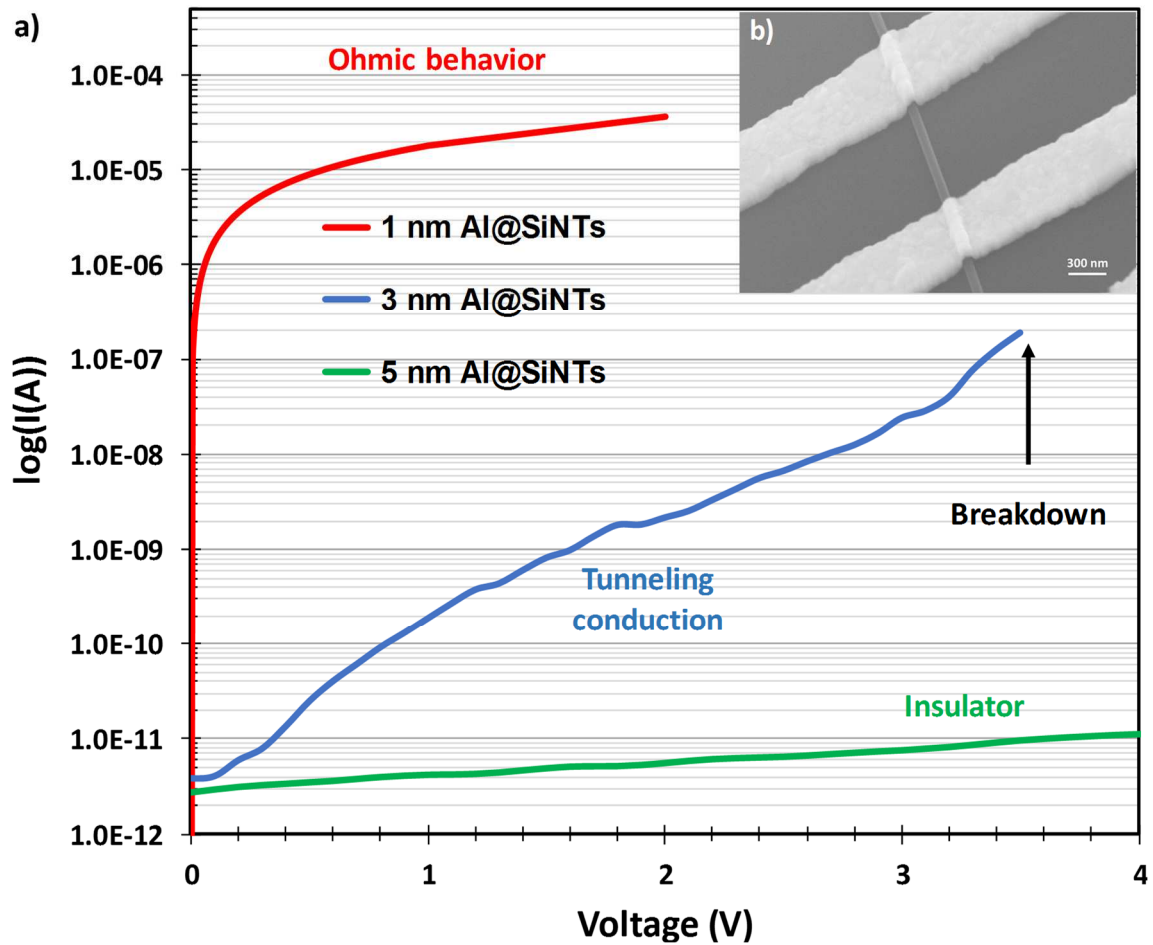


Figure 3. a) Electrical characterization of the alumina/silicon interface by I-V technique on a single isolated Si NW covered by different alumina dielectric thicknesses. b) The inset shows SEM Imaging of electrical contacts on a 5 nm alumina capped Si NW.

In contrast, the 5 nm thick alumina barrier displays the electrical behavior of a classical dielectric material being an insulator over the whole potential window. The measured current values are in the order of the pA, the typical noise level of the measurement apparatus, with a 5 V stability of the barrier. In such condition, the ALD deposited dielectric layer is indeed fully pin-hole free and can be considered electrically-wise as an insulator. Finally, a 3 nm thick layer of alumina on a Si NW exhibits a remarkable behavior. The electrical measurement shows an exponential-like dependence of the current vs the applied voltage, shown to be typical of tunneling transport of electrons through an electronic

barrier.^[25-27] The 3 nm thick alumina is again pin-hole free but still allows the conduction of electrons. Thus, at particular nanometric thickness, a conformal layer of alumina does not electrically behaves as a common dielectric material but rather undergoes tunneling electron conduction with a breakdown voltage measured at 3.5 V, a value in agreement with microelectronic literature.^[28,29]

This behavior has already been investigated in studies for gate oxides development in microelectronics;^[30-32] but is seldomly known in the energy storage field and has never been demonstrated on an electrode material to be immersed in an electrolyte and used for storage application. Still, for energy storage this behavior is remarkable for an alumina layer, previously seen as a fully insulating thus detrimental for energy storage properties, to combine both the protection given by its conformity with electron conduction properties. In the energy storage field, this new way of seeing a whole class of materials, the dielectrics when controlled at nanometric scales, could lead to major improvements in the stability of already existing advanced technologies.

3.2. Electrochemical characterization

A practical application of this effect is studied below with micro-supercapacitor devices made of silicon nanotrees (SiNTs) electrodes, with ultra thin alumina layers, operating in aqueous electrolyte. The benefit of the addition of the nanometric dielectric layer on the energy storage performances is investigated by standard electrochemical measurements (**Figure 4**). The impact of the thickness is highlighted by benchmarking performances of SiNTs electrodes covered with 1, 3 and 5 nm of Alumina (Al@SiNTs).

As previously mentioned, a major weakness of silicon nanostructure and of silicon itself, is the growth of silica under oxidative atmosphere at its surface.^[33] Herein in the **Figure 4**. a), the electrochemical response of a 3nm coated Al@SiNTs in aqueous media is typical of an electrical double layer supercapacitor with a near perfect rectangular shape stable over the whole potential window. Despite the increase of the scan rate, the behavior is kept up to 1

$V.s^{-1}$ indicating the good stability of the system. By contrast, the resistive behavior of pristine SiNTs in aqueous electrolyte can be found in **Figure 4. b)** below. The resistivity of the silicon based electrode material without the alumina nanometric layer is significant over the whole electrochemical window. Moreover, the electrochemical storage performances are diminished. The intake brought by the addition of the dielectric layer is unequivocal, the electrode resistivity is greatly decreased compared to the pristine one while the electrochemical stability of the material at the extrema of the potential window is ensured. Thus, the alumina layer protects the silicon nanostructure from oxidation enabling silicon nanostructures to electrochemically behave as an active storage material in aqueous electrolytes reaching high performances.

A thickness of 3nm of the alumina dielectric is the best compromise to increase the stability of silicon micro-supercapacitors in ionic liquid as shown in our previous work, ^[34] while retaining high capacitance. This observation might not still be valid in aqueous electrolytes, hence a study of the impact of the thickness is conducted. The **Figure 4. c)** displays the galvanostatic behavior of two-electrode cells in aqueous electrolyte varying the thickness of the ALD layer. When increasing current densities in two-electrode cell studies, nanostructures protected only by 1 nm of alumina show their resistive hindrance to the capacitive behavior while 3 nm and 5 nm of alumina maintain a near perfect triangular shape typical from a capacitive galvanostatic response. The derived capacitance value of each devices are then reported in **Figure 4. d)** along with a Ragone plot in **Figure 4. e)**. Both areal capacitance and specific energy decrease steeply when increasing current densities above 0.2 mA.cm^{-2} . In contrast, Al@SiNTs covered by 3 and 5 nm of alumina are able to maintain similar storage performances at current densities up to 2 mA.cm^{-2} .

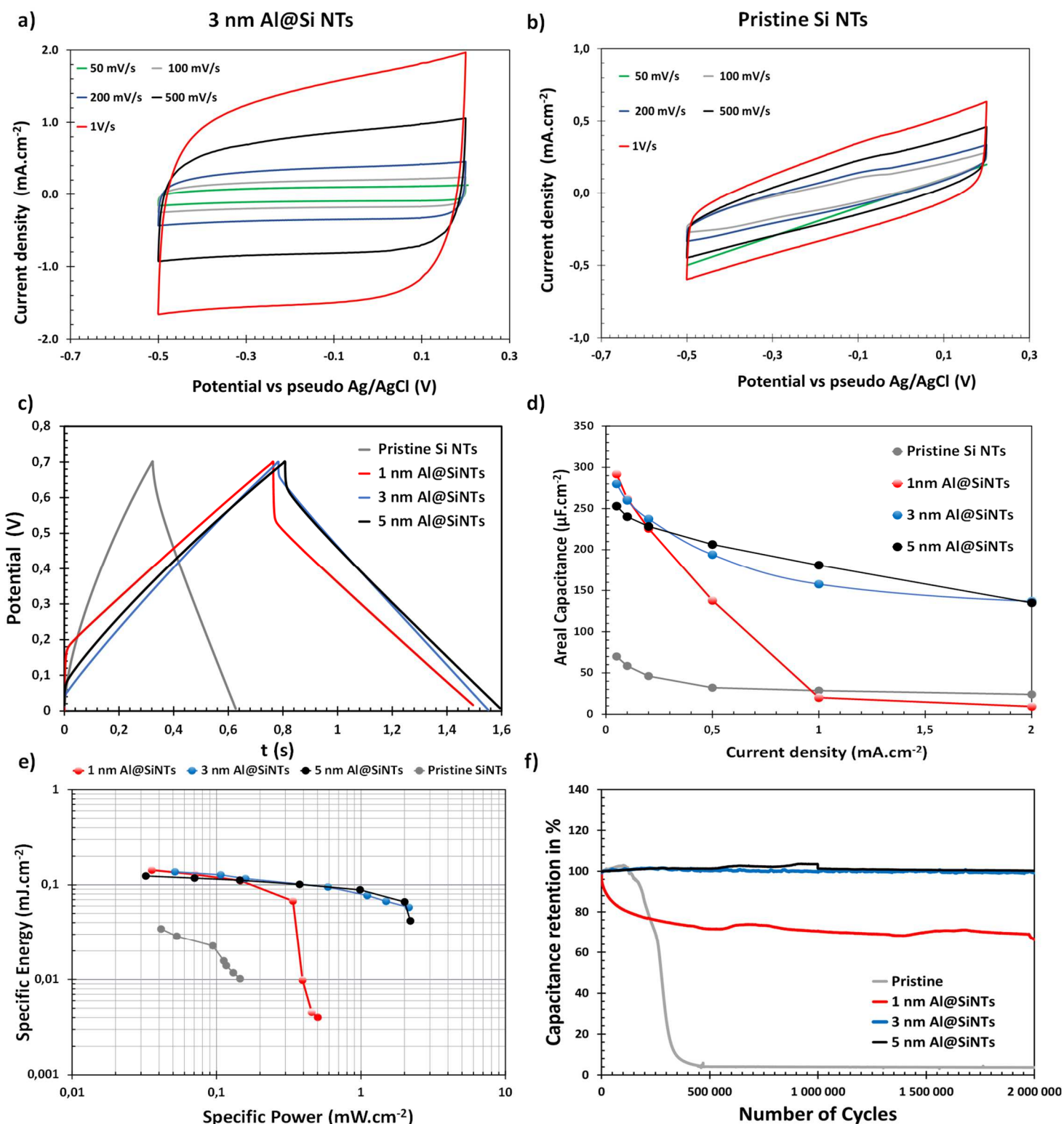


Figure 4. Al@SiNTs electrochemical characterization in Na₂SO₄ 0.2M electrolyte a) Voltammograms of 3 nm Al@SiNTs at different scan rates . b) Voltammograms of pristine Al@SiNTs in the same conditions. The high resistivity of the nanostructure, due to the oxidative environment, is highlighted. c) Two-electrode cell galvanostatic charge/ discharge plot of Al@SiNTs at a current density of 0,1 mA·cm⁻². d) Areal capacitance of Al@SiNTs at different current densities varying the dielectric thickness. e) Ragone plots comparing Al@SiNTs covered with different alumina thicknesses. f) Stability stress test of Si NTs microsupercapacitor devices at 0.5 mA·cm⁻².

Lastly, a core and unmatched feature of silicon nanostructures as electrode material for micro-supercapacitor applications is their outstanding stability in devices which are able to withstand more than 5 million galvanostatic cycles in ionic liquid.^[34] For the Al@SiNTs of this study, a stability stress test at $0.5 \text{ mA}\cdot\text{cm}^{-2}$ is performed in full cell while varying dielectric thicknesses as shown in **Figure 4. f)**. Compared to pristine material, which drastically degrades after 50 000 charge/discharge cycles, the 3 and 5 nm protected Al@SiNTs are able to withstand 2 million galvanostatic cycles with almost 100 % capacitance retention. To the writer's knowledge, this result is one highest reported results for silicon-based micro-supercapacitor using aqueous media. Their application field can now be expanded to aqueous electrolytes paving the way to safer and lower natural impact applications. In addition, a large number of pseudocapacitive materials, displaying higher capacitive performances compared to silicon nanostructures, are electrochemically active and usually deposited in aqueous media.^[35-37] Thus, a whole range of new additive materials is available to reach advanced energy storage performances.

For 1nm Al@SiNTs, the capacitance retention reaches 72% after 2 million cycles highlighting again the imperfection of the dielectric barrier. Part of the silicon nanostructure is not totally covered and gets in contact with the aqueous media. Over the cycling test, the silicon is oxidized in unstable silica increasing the resistivity of the device and degrading its capacitance performances.

Once again, these experiments highlight the defects of the 1 nm ALD deposited alumina layer and the limitation of the ALD process at sub-nanometric thicknesses. Going towards 3 nm or 5 nm thick dielectric, which do not require much more time to be deposited, ensure a total protection of the nanostructure.

In order to further investigate the electrochemical behaviour of the alumina/SiNTs interface in aqueous oxidative media, impedance spectroscopy including Mott Schottky measurements are used (**Figure 5**). Here the impact of the thickness of the dielectric layer

remains critical as the resistivity of the material depends on the alumina thickness. As previously observed, pristine silicon nanostructures display high resistivity overall with a wide impedance semi-circle thus high resistance to the charge transfer (**Figure 5. a**)).

The 3 nm protected SiNTs seems to be the better compromise in terms of charge transfer ability due to its low impedance semi-circle diameter. The inset of the measurements at higher frequencies given in **Figure 5. b**) confirm this behavior : At each frequency the value of the $\text{Re}(Z)$ for the 3 nm protected SiNTs ($18 \Omega \cdot \text{cm}^{-2}$) is lowered by approximately a factor 3 and 5 compared to the 5 nm and 1 nm dielectric protected SiNTs respectively (40 and $90 \Omega \cdot \text{cm}^{-2}$ respectively). These results are attributed to the presence of surface defects in the 1 nm dielectric layer due to the limitations of the ALD technique at thicknesses lower than 1 nm and to the thicker dielectric layer for the 5 nm one.

The procedure, depicted in materials and methods, to obtain the time constant of the material is summarized in **Figure 5. c**). From the frequencies of the impedance maxima, the Micro-supercapacitor time constants are compared in **Figure 5. d**). For supercapacitor applications the lower the time constant, the more efficient the charge/discharge of the device will be.^[38]

In this regards 3 nm Al@SiNTs represents the optimum solution having a lower time constant value of 51 ms compared to 156 and 59 ms for 1 and 5 nm protected SiNTs respectively, **Figure 5. d**). Thus, for further impedance spectroscopy investigation, 3 nm Al@SiNTs is preferentially selected for being the optimal compromise.

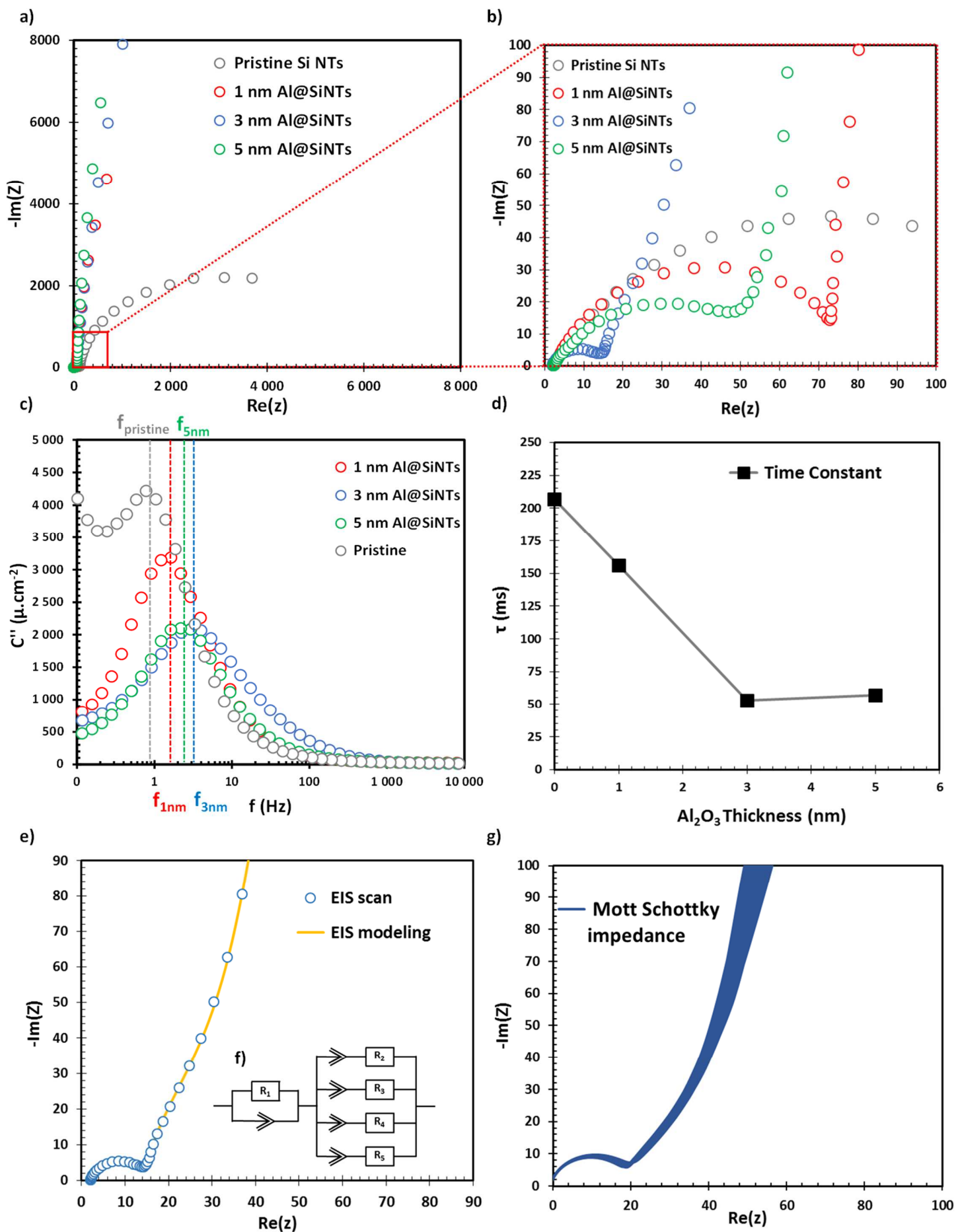


Figure 5. Al@SiNTs EIS characterization a) Nyquist plot of the Si NTs depending on the Alumina dielectric thickness at open circuit voltage highlighting the impedance behaviour at low frequencies. b) The inset shows a magnified version of the the Nyquist plot within the frequency range of 20 mHz to 1 Hz at open circuit voltage highlighting the impedance behaviour at high frequencies. c) Imaginary part of the impedance for the Si NTs depending on the Alumina thickness. The time constant of the MSCs is derived from the frequency of the maxima. d). Micro-supercapacitor time constant comparison with the ALD alumina layer thickness. e) Nyquist plot of 3 nm protected Al@SiNTs at open circuit voltage with fitting impedance model (yellow curve) by EC-Lab software and Equivalent circuit of the material based on impedance software modelling (inset f)). g) Mott-Schottky impedance spectroscopy of 3nm protected Si NTs between -0.5 V and 0.2 V vs Ag/AgCl.

Using an impedance modelling software, an equivalent circuit modelling the electrical behaviour of the 3 nm alumina protected SiNTs is given in **Figure 5. e)** and **Figure 5. f)**. The model is based on the work of Fletcher and al. which have designed a model for EDLC supercapacitors commonly used with carbonaceous electrode materials.^[39] (more information about the fitting process in **Figure S2** of the supporting information). Thus, by impedance spectroscopy measurement, the energy storage mechanism of dielectric protected SiNTs is decisively confirmed to be of the Electrical Double Layer type. Finally, a Mott Schottky study of the material, **Figure 5. g)**, is performed with impedance measurements over the whole potential window with a 5 mV step. The low dispersion of the spectrum demonstrates the stability of the capacitive response over the potential window which is again typical of an EDLC storage mechanism and confirm the validity of the model selected based on the work of Fletcher and al.^[40]

Overall, in the case of the alumina dielectric with nanoscale thickness, a 3 nm protection layer is the best compromise combining lower resistivity, electrochemical stability, tunnelling conduction and EDLC behaviour.

From a nanostructural point of view, the stability of the 3 nm alumina protected NTs under electrochemical working condition is investigated via electron microscopy techniques. The evolution of the composition and the morphology of the pristine and the 3 nm protected

SiNT electrodes after 2 million charge/discharge cycles are observed by SEM and EDX measurements, **Figure 6**. After a 2-month stress cycling test, the morphological aspect of SiNTs covered by the nanometric alumina dielectric shows no visible changes compared to nanotrees before cycling (see **Figure S3**), which confirms the stability of the nanostructures in aqueous electrolyte. Moreover, by EDX elemental mapping scan, the integrity of the nanomaterial is retained with the absence of chemical modification induced by the oxidative electrolyte media. In contrast, bare SiNTs composition is modified by the long-term cycling in Na_2SO_4 electrolyte with the occurrence of sodium and sulfur peaks at 1.1 and 2.32 eV respectively.

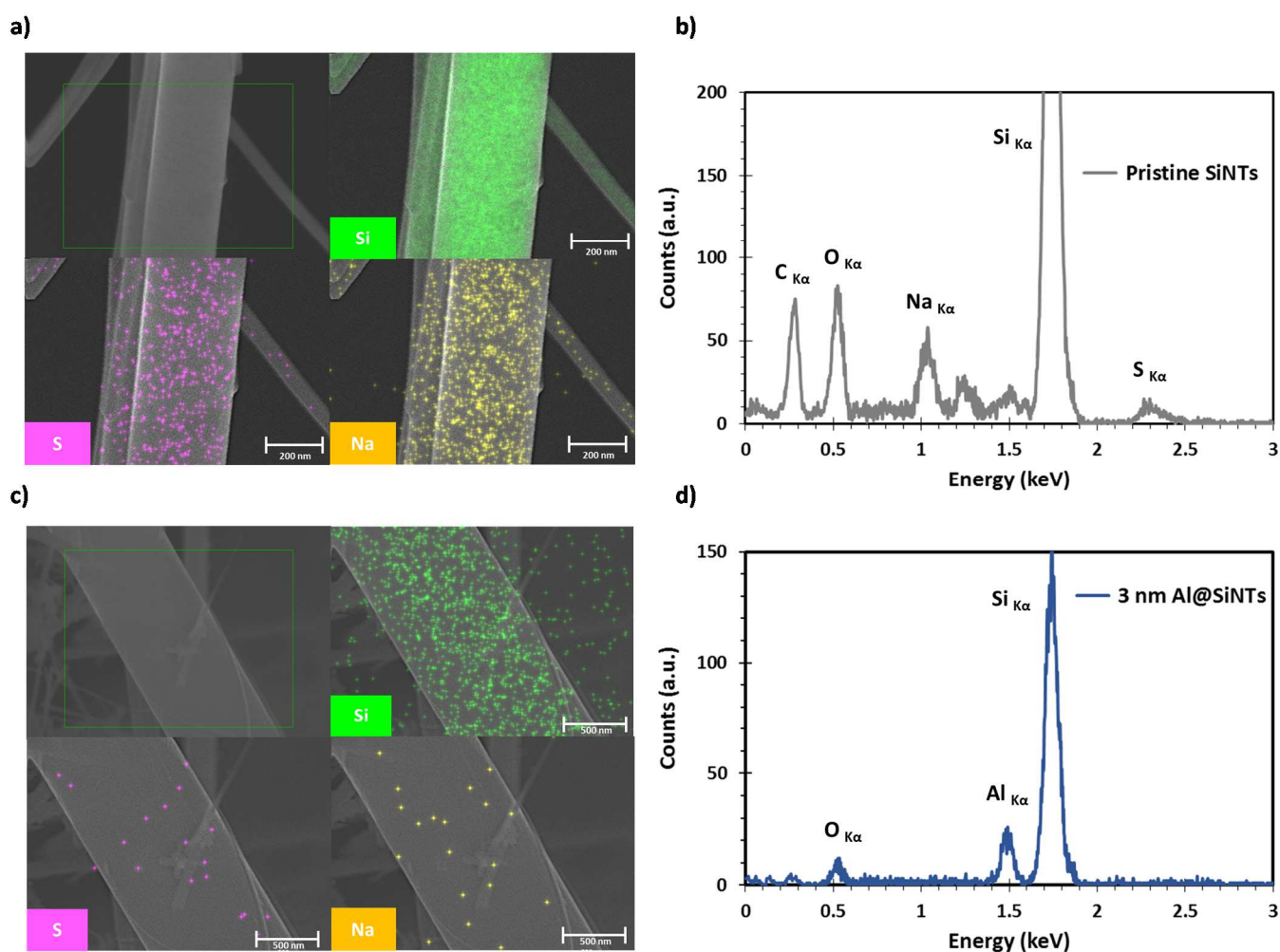


Figure 6. EDX scans and EDX composition spectra of pristine Si NTs after 2 million charge/discharge cycles in aqueous electrolyte. (picture a) and b) respectively). EDX scans

and EDX composition spectra of 3 nm alumina protected SiNTs after 2 million charge/discharge cycles in aqueous electrolyte. (picture c) and d) respectively.).

4. Conclusions

This work presents a reconsideration of the vision in energy storage of a well-known material class, high-k dielectric materials. Through tailoring nanoscale properties and using microelectronic measurement techniques, a pin-hole free nanometric layer of alumina on a silicon nanowire was shown to display an electronic tunnel conduction. An application of this result in the energy storage field is then detailed with silicon based micro-supercapacitor. The protection provided by a 3 nm thick layer of alumina dielectric allows this supercapacitive electrode material to operate with a whole new range of electrolytes. The cycling stability of such device in aqueous electrolyte is shown to reach more than 2 million cycles at $0.5 \text{ A}\cdot\text{cm}^{-2}$ exceeding by far the stability of any silicon based MSCs using aqueous electrolyte previously reported in the literature.

By modifying the vision of a long term used material class, dielectrics, based on a nano-centered approach using growing tools such as ALD, new advanced features for an electrode material were achieved. Such a method is easily adaptable to various energy storage materials and could lead to notable progress.

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