# Self-Timed Ring Oscillator Based Time-to-Digital Converter: a 0.35$\mu$m CMOS Proof-of-Concept Prototype

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# Self-Timed Ring Oscillator based Time-to-Digital Converter: A 0.35$\mu$m CMOS Proof-of-Concept Prototype

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***Abstract*—This paper presents an ASIC test chip designed and fabricated in 0.35 µm CMOS process to further confirm and evaluate the advantages of the time-to-digital converter (TDC) based on a self-timed ring oscillator (STRO). Three TDCs with different number of STRO stages have been included in this test chip. Most of the measurements are perfectly in accordance with our theoretical claims. The fabricated circuits prove the ability of the proposed TDC architecture to enhance the time resolution by increasing the number of stages. Indeed, three TDCs with $L = 9, 23$ and $61$ have been integrated in the same chip. A 10-bit counter was used to cover a dynamic range of 1.7 µs. The smallest TDC, with $L = 9$, samples the time intervals with a time resolution of 72.5 ps, while a time resolution of 13.9 ps is obtained with the TDC of $L = 61$.**

***Index Terms*—Time-to-digital converter, self-timed ring oscillator, time resolution, time measurement, CMOS AMS350 technology, on-the-fly measurement .**

## I. Introduction

In many application fields incorporating high precision time measurements, such as high-energy physics, metrology, telecommunications and satellite positioning [1]–[4], the time-to-digital converters (TDCs) are highly deployed. They are used to measure time intervals in the picosecond range. The most known analog TDC architecture is based on the time stretching technique, which allows benefiting from a fine time resolution [4]–[6]. However, there is an increased demand for fully digital approaches to benefit from low-power and small circuit area. Thus, the digital TDCs, for which the technology shrink can be easily adopted, are offering simple architectures and sub-gate resolution [7]–[10]. Thanks to the digital circuits, on-the-fly measurements is ensured with simply using the delay lines [2]. In accordance with a wide dynamic range, the delay-line can be looped to make an oscillator and to re-use the delay gates many times. Unfortunately, the resolution of these TDCs is limited by the gate delay. One possible solution to get sub-gate time resolution is to employ the Vernier technique [8], [11]. Despite the simple and fully digital architectures of these TDCs, they cannot combine a sub-gate resolution for on-the-fly measurements and wide time intervals. Advanced techniques trying to combine the advantages of each kind of the above architectures in order to reach better performances have been proposed [8], [9], [12]. They are mainly adopted for dedicated applications. However, their principles often target a time resolution improvement. Even for advanced TDCs [10], [13], most of the structures are not able to combine all the desired performances : sub-gate resolution, wide dynamic range, and good linearity. Unfortunately, this is not perfect, especially for the on-the-fly measurements. In our previous works [14]–[16], we proposed a proof-of concept of a new TDC architecture based on a self-timed ring oscillator (STRO), which gives some trends for solving this issue.

The proposed TDC is able to provide a very high resolution without averaging. Indeed, it virtually achieves a time resolution as fine as desired by simply increasing the STRO number of stages. In fact, the STRO is a multi-phase oscillator, which is able to provide one phase per stage output. The TDC exploits these different STRO phases, which are evenly-spaced thanks to the unique analog STRO properties. Thus, a regular time base can be extracted from this STRO and applied for time measurement. This paper demonstrates the advantages of such a TDC in terms of precision, calibration, low-cost and for on-the-fly measurements. It also states the TDC limits due to the STRO jitter. An ASIC prototype has been designed, fabricated and tested for validating this new class of TDC using 0.35 µm CMOS process.

The paper is structured as follows: Section II describes briefly the STRO principles. Section III details the STRO-based TDC architecture and its working principle. Section IV reports the main TDC blocks implementation in 0.35 µm CMOS process. The experimental results are presented in Section V. Finally, Section VI states the paper conclusions.

## II. Self-Timed Rings and Operation Principles

The self-timed ring oscillator (STRO) is basically a control circuit of micropipelines that is looped back to form a ring, as proposed by [17]. Based on simple asynchronous digital gates, called C-element, the architecture of the STRO is simple to design [14], [16], as depicted in Fig. 1. Each STRO stage has a forward (resp. backward) static propagation delay $D_{\text{ff}}$ (resp.

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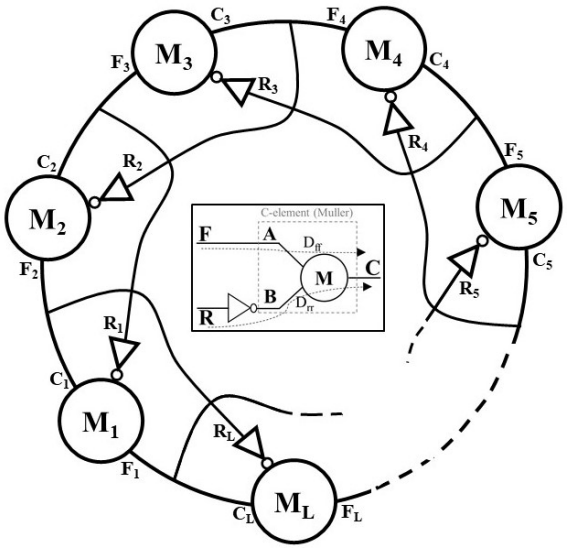


Figure 1. Global architecture of a L-stage STRO.

reverse static propagation delay $D_{\mathrm{rr}}$). This oscillator allows propagating several events (electrical transitions) simultaneously without colliding thanks to the request/acknowledgment handshake protocol. The number of these events stays invariant. The ring is modeled with a token game by which the events are initialized in the ring (tokens and bubbles) [18]. A ring stage $i$ contains a token if its output $C_i$ differs from the output of the next stage $C_{i+1}$ ($C_i \neq C_{i+1}$), and it contains a bubble if these two outputs are the same ($C_i = C_{i+1}$). A token propagates to the next stage if and only if it contains a bubble. In this case, the bubble propagates in the opposite direction and replaces the token, which had freed its place. By this process, the events push away in time from each other as they propagate in the ring due to the presence of the analog phenomena, namely the Charlie's effect and the Drafting effect [19]. The Charlie's effect can be expressed by: *the closer are events at the inputs of a Muller gate, the longer is its propagation delay* [18]. Whereas, *the shorter is the time between two successive commutations of the output C of the C-element, the shorter is its propagation delay* (Drafting effect). As a result, two steady state modes are possible: the evenly-spaced mode and the burst mode.

One important features of the STROs is that their frequency does not directly depend on the number of stages $L$ but rather on its occupancy ratio (as function of token's number $N_T$ or bubble's number $N_B$). Moreover, this frequency can be adjustable for the same STRO. Furthermore, the main consequence of the STRO evenly-spaced mode is that STROs can produce a uniform phase distribution. As a result, a regular time base is generated by these equidistant phases with a sub-gate time resolution $\Delta\varphi = T_{\mathrm{STR}}/2L$, where $T_{\mathrm{STR}}$ is the STRO oscillation period [14] (assuming that the number of tokens is co-prime with the number of stages). Thus, the time resolution between these phases can be accurately tuned as fine as needed by simply increasing the number of ring stages. The resulted equidistant phases is able to achieve sub-gate delay resolutions and can be exploited for on-the-fly time measurement on fast non-periodic signals. The Charlie's effect provides a unique feature to the STRO. This is the strength of our approach because the electrical transitions propagating into the ring become evenly-spaced after the ring was initialized. Therefore, the phase distances are particularly accurate and stable with STROs. This is comparable to an automatic calibration of the distance between the phases. No calibration is required at this level.

Table I
POSSIBLE STATES FOR THE N-BIT VECTORS $B_k = M$ AND $B_k = M + 1$.

| State | $M$ $(b_{i,n-1}, b_{i,n-2}, ..., b_{i,1}, b_{i,0})$ | $M+1$ $(b_{j,n-1}, b_{j,n-2}, ..., b_{j,1}, b_{j,0})$ |
|---|---|---|
| 1 | X...X00 | X...X01 |
| 2 | X...X10 | X...X11 |
| 3 | X...X01 | X...X10 |
| 4 | X...X11 | X...X00 |

## III. TDC ARCHITECTURE

The proposed STRO-based TDC exploits the features of the STRO previously presented in [14], [16]. In fact, an $L$-stage STRO, with a number of tokens $N_T$ co-prime with the number of stages $L$, provides $L$ signals evenly distributed over its half oscillation period $T_{\mathrm{STR}}/2$. By exploiting the L-stage STRO phases, the time interval $T$ to be measured can be quantified considering both edges. If all outputs are connected to n-bit counters, each counter would count either $M$ or $M+1$ events. Let $k$ be the number of counters having the value $M+1$ (while $L-k$ counters have the value $M$). The quantification of $T$ can be expressed by:

$$T_m = M\frac{T_{\mathrm{STR}}}{2} + k\Delta\varphi = (ML + k)\Delta\varphi \qquad (1)$$

Let $B_k = (b_{k,0}, b_{k,1}, ..., b_{k,n-1})$, where $k \in [1, L]$, be the bit vector presenting the output of the $k^{th}$ n-bit counter connected to the STRO output $C_k$. The difference between the binary vector of $M$ and $M+1$ is globally detected for the two least significant bits as presented in Table I (unless the state 4 which can affect sequentially the MSB). We propose to represent $M$ with the vector $B_i$, and $M+1$ with the vector $B_j$. The parity of $M$ can be evaluated using the bits $b_{k,1}$ ($k \in [1, L]$). $B_i$ is even when: $b_{i,1} = b_{j,1}$ (state 1 and 2). Oppositely, $B_i$ is odd when the two bits are different (state 3 and 4). Therefore, if at least one bit of $LSB_1 = (b_{1,1}, b_{2,1}, ..., b_{L,1})$ is different, then $M$ is odd, and if they are all equal, then $M$ is even. The parity of $M$ is noted with a Boolean $P$, which is set to '1' if all bits of $LSB_1$ are identical and to '0' otherwise.

On the other hand, if the LSB of $B_i$ is equal to '0' (in case $M$ is even), the number $k$ of counters having the value $B_j$ is the number of the bits of the vector $LSB_0 = (b_{1,0}, b_{2,0}, ..., b_{L,0})$ equal to '1'. Otherwise, in case $B_i$ is odd, $k$ corresponds to the number of bits of $LSB_0$ equal to '0'. Hence, the hamming weight of the vector $LSB_0$ is used

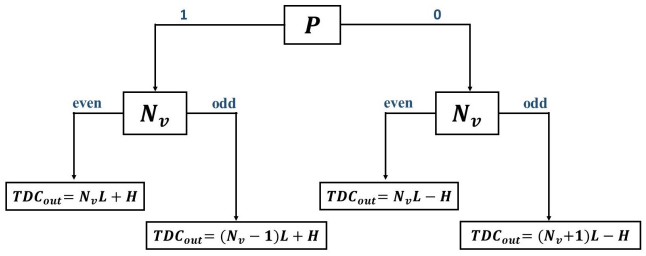


Figure 2. Computation algorithm applied to the STRO-based TDC according to the values provided by the computing unit $H$, $P$, and $N_v$.

to define the value of the variable $k$. More explicitly, the hamming weight of $LSB_0$, denoted with $H$, is equal to $k$ when $M$ is even and $L - k$ when $M$ is odd.

According to the above analysis, equation (1) can be resolved by using a simple algorithm (instead of using n-bit counters for all the phases). Let $N_v$ be the number of transitions counted by an arbitrary n-bit counter during the time interval $T$. To determine if the value $N_v$ corresponds to $M$ or $M + 1$, we evaluate the parity of $M$ using $LSB_1$. Then we compare the result with the parity of the value $N_v$. The value of $k$ is determined by $H$. The diagram given by Fig. 2 summarizes the computation algorithm of $M$ and $k$ as a function of $N_v$, $P$ and $H$. Thus, the TDC output $\mathrm{TDC}_{out}$ ($T_m = \mathrm{TDC}_{out}.\Delta\varphi$) can be expressed according to the parity of $N_v$.

The global architecture of our proposed TDC is depicted in Fig. 3. In this structure, an $L$-stage STRO is used. The coarse conversion is carried out by an n-bit counter connected to a single STRO output, presenting the value $N_v$. Then, for the other $L - 1$ STRO outputs, only 2-bit counters are required in order to determine both $M$ and $k$. The value $P$ is obtained by the $M$ Parity block. The Hamming block uses the LSBs of the counters to compute the hamming weight $H$.

## IV. Hardware Implementation

An ASIC test chip has been designed and fabricated in 0.35 µm CMOS process. Indeed, to cover several time resolution, TDCs with different numbers of stages ($L = 9$, $L = 23$, and $L = 61$) have been implemented in the same chip. Each TDC operates independently. According to the selected TDC, the measurement results are presented in the common outputs of the chip. The global architecture used to implement these TDCs, generalized to L-stage STRO-based TDC, is illustrated in Fig. 4.

### A. STRO with analog C-element

The *analog C-element* topology has been chosen for the STRO-stage implementation to benefit from the symmetric topology and to simplify the connection between the stages. Thus, the same values of $D_{\mathrm{ff}}$ and $D_{\mathrm{rr}}$ are obtained. The estimated values of these propagation delays using the 0.35 µm CMOS technology are $D_{\mathrm{ff}} = D_{\mathrm{rr}} = 350ps$. Thanks to this, the maximal frequency, with maximal Charlie's effect amplitude, is obtained for equal number of tokens and bubbles

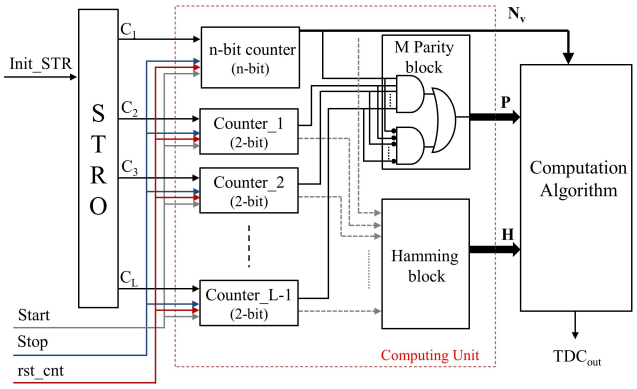


Figure 3. Proposed TDC architecture using an L-stage STRO.

($N_T = N_B \pm 1$). Therefore, for a maximal frequency, a $L$-stage STRO is initialized with $L/2$ events. In this case, the same frequency is obtained for each STRO of any number of stages as long as the occupancy ratio is surely equal to 1/2. Therefore, duplicating the number of STRO stages by $N$ allows to reduce the time resolution by this factor.

The *analog C-element* has symmetric inputs and outputs. Its connectivity is displayed in Fig. 5. It shows the direct connection of the stage $i$ with its adjacent stages (stage $i - 1$ and stage $i + 1$). In the same figure, an example of the initialization process was described. It details how to assign signal values to the inputs $Rb_i$ and $S_i$ in order to initialize the stage with a token or a bubble. For a fast distribution of events over the STRO, it is recommended to initialize the ring as follows: {TBTBTB..} (*e. g.*, it can correspond to an STRO output vector of {0110011..}). The inputs $Rb_i$ and $S_i$ allow initializing the stages. In fact, the input signals $Rb_i$ and $S_i$ are active low, which allows to reset (resp. to set) the stage output $C_i$. Only one signal *init* can be used to assign values to the initialization inputs. It can be initialized with a value "0" in order to active the inputs $Rb_i$ and $S_i$, and then goes high to make stages in a free mode. An illustration is displayed in Fig. 5 in which the output $C_{i-1}$ is set to "1" while $C_i$ and $C_{i+1}$ are set to "0". According to this, the stage $i - 1$ is initialized with a token and the stage $i$ initialized with a bubble. In order to make the design simple, the STRO stages have been designed with a fixed initialization. The design can easily be implemented using standard cells.

The signal *ena*, which triggers the tri-state inverters of the *analog C-element*, freezes the inverter outputs during the initialization. Thus, it is only set high once the initialization is finished. Notice that the signal *init* has the same shape as the signal *ena*, as shown in Fig. 6. The signal *init* can only be used as input signal, as depicted in Fig. 4. Thus, the signal *ena* must be sufficiently delayed to guarantee a correct initialization.

### B. Counting unit implementation

A 10-bit counter is implemented to cover a dynamic range of 1.7 $\mu$ s. A double-edge counter made by two 9-bit counters is required: the first one is clocked with $C_i$ and the second

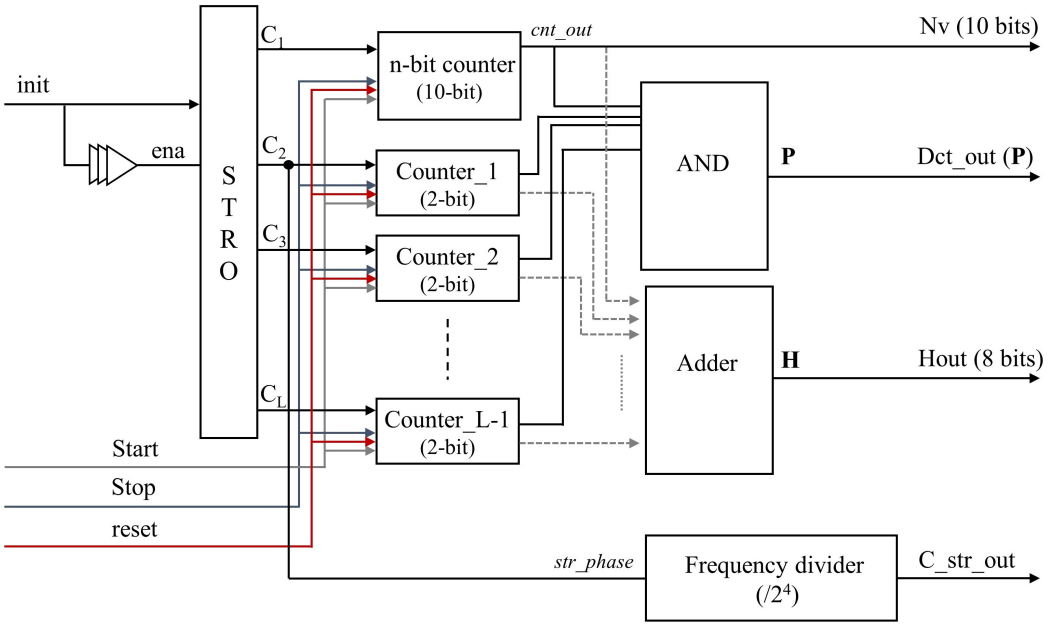


Figure 4. The global architecture of L-stage TDC for 0.35 µm CMOS technology implementation.

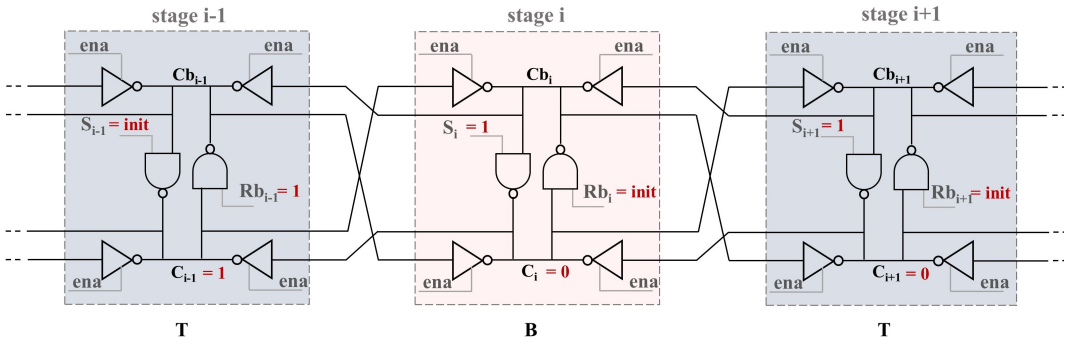


Figure 5. Three stages example from a self-timed ring oscillator with *Analog C-element* implementation given with an initialization example.

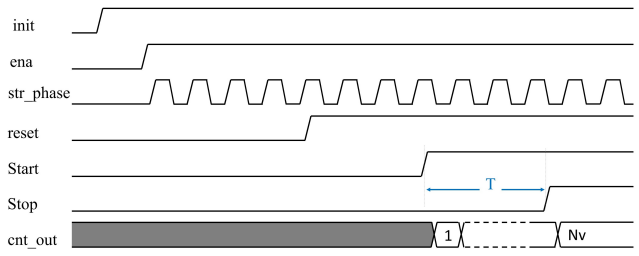


Figure 6. The chip input signals timing diagram.

with $Cb_i$. The sum of the outputs is represented on 10 bits. The counters include Mutex circuits making a decision in case of metastability. The *Enable* signal brings the start and stop times of the interval $T$, which needs to be measured.

Otherwise, each TDC includes its own Hamming and $M$ Parity blocks needed to compute the value of $H$ and $P$ for each measurement. They are simply made by adders and AND gates. The Hamming block output requires 7 bits to fit with the results for all these TDCs.

### C. Input/Output interfaces

The finite-state-machine (FSM) has been implemented off-chip (on an FPGA). It allows generating the input signals as presented in Fig. 6. The *init* signal is generated by the FSM. On its arrival, *init* is delayed in order to produce the signal *ena*. The *reset* signal, generated by the FSM, allows resetting the flip-flop outputs of the counters before starting a measurement on the *Start* event. Then, the measurement is stopped by the *Stop* signal, which triggers the TDC outputs. Another *reset* signal is used to initialize the FSM, which is independent from the counter *reset* signal. *Sel*, a 2-bit signal, allows selecting the TDC we want to use.

Fig. 7 shows a block diagram for connecting the FSM with the chip for the test. Indeed, the use of the FSM is optional and can be replaced by other sources able to create signals such as generators.

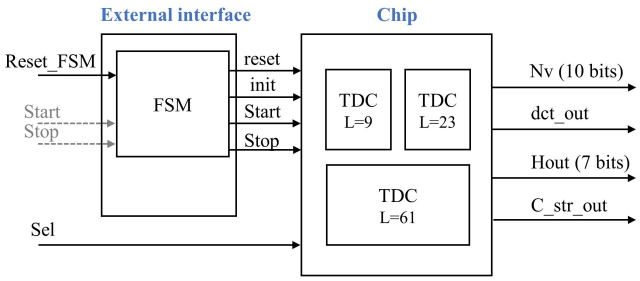


Figure 7. Block diagram of the experimental setup.

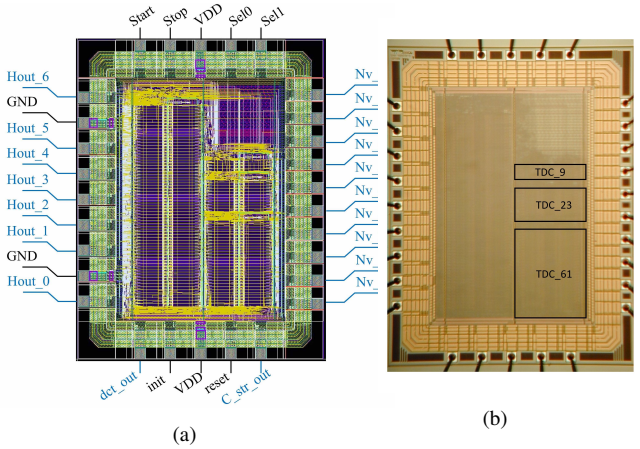


Figure 8. (a) the circuit layout with pads and input/output, (b) Microphotograph of the three STRO-based TDC chip.

Practically, for the 0.35 µm CMOS technology, the maximal input frequency allocated to the input of the pads is limited to 100.0 MHz. Unfortunately, the STRO frequency exceeds this bandwidth limitation and can further reach 850.0 MHz, as it has been shown by simulations. Therefore, the *C_str_out* signal has to go through a frequency divider to be externally measured. A division ratio of $2^4 = 16$ has been implemented into the frequency divider. A total number of 25 pads have been included in the circuit to interface the TDCs with the measurement tools, as schematically shown in Fig. 8a.

## V. Experiment Results

The proposed STRO-based TDC was fabricated in the 4-metal layers CMOS 0.35 µm AMS technology. The supply voltage is 3.3 V. A microphotograph of the four STRO-based TDC fabricated in CMOS 0.35 µm AMS technology is shown in Fig. 8b. Each TDC placement is mentioned in the figure. The size of the whole layout including the input/output pads is 2.88 mm×2.21 mm. The actual core area is 3.29 $\mathrm{mm}^2$ (2.18 mm × 1.51 mm). The 9-stage STRO-based TDC occupies an area of 0.181 mm×0.67 mm, which presents 3.7% of the core area. The 23-stage STRO-based TDC area is 0.380 mm × 0.67 mm, which presents 7.7% of the core area. The 61-stage STRO-based TDC occupies 17.9% of the core area (0.880 mm × 0.67 mm).

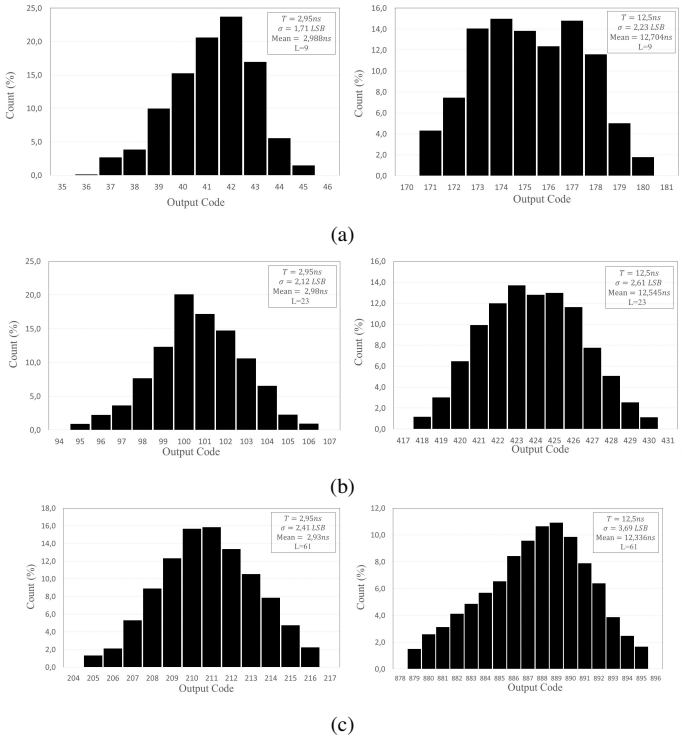


Figure 9. Measured single-shot precision of the: (a) 9-STRO based TDC (b) 23-STRO based TDC (c) 61-STRO based TDC, when input time intervals are respectively 2.95 ns and 12.5 ns.

As shown in Fig. 7, the test setup consists of using an external interface, employed as a signal generator, and an oscilloscope. An Intel Cyclone IV FPGA was used to generate the input signals (*reset*, *Sel*, *init*, and *Start* signals). In fact, the *Start* signal was split into two pulses. The direct pulse is injected into the TDC as the *Start* signal. The second pulse is delayed by a coaxial cable and, then, injected into the TDC as the *Stop* signal. Therefore, the time made by the signal to propagate into the cable, which is related to the length of the cable, presents the time interval to be measured by the TDC. The oscilloscope allows measuring the frequency of the STRO presented by the output *C_str_out*.

### A. 9-stage STRO-based TDC

The first TDC of 9 stages (with an initialization of 4 tokens) shows an estimated time resolution of 74.0 ps. This latter is enough larger than the jitter standard deviation of the STRO. The jitter value is estimated to be between the 10.0 ps and 15.0 ps. This TDC consumes 88.9 mW at room temperature (25°). As a result, a theoretical time resolution of 72.5 ps is obtained.

A large number of measurements have been made in order to characterize the single-shot measurements. Thus, many hits, carried out using several coaxial cables, were analyzed in order to characterize the TDC performances. Fig. 9a plotted the histogram of the resulted digital TDC outputs for two different time delays: 2.95 ns and 12.5 ns. The TDC shows a mean value of 2.988 ns with a standard deviation of $\sigma = 1.71$ LSB for

the time input $T = 2.95\,\mathrm{ns}$ representing an error of 38.0 ps. When the input time is $T = 12.5\,\mathrm{ns}$, the measurement error is 204.0 ps for a mean value of 12.704 ns and a standard deviation of $\sigma = 2.23\,\mathrm{LSB}$.

### B. 23-stage STRO-based TDC

On the other hand, the same measurements from the 23-stage STRO-based TDC have been processed. This TDC was adopted to enhance the time resolution around the jitter variations including 12 tokens. The achieved time resolutions is 29.6 ps. This TDC presented a power consumption of 164.6 mW for a frequency of 734.43 MHz corresponding to $\Delta\varphi = 29.6\,\mathrm{ps}$. As displayed in Fig. 9b, the TDC shows a measurement error of 30.0 ps (resp. 45.0 ps) with a mean value of 2.98 ns (resp. 12.545 ns), and a standard deviation of $\sigma = 2.12\,\mathrm{LSB}$ (resp. $\sigma = 2.61\,\mathrm{LSB}$) for $T = 2.95\,\mathrm{ns}$ (resp. $T = 2.95\,\mathrm{ns}$).

### C. 61-stage STRO based TDC

The time resolution of the 61-stage STRO-based TDC initialized with 30 tokens is equivalent to $\Delta\varphi = 13.9\,\mathrm{ps}$ with a measured frequency of 589.69 MHz and a power consumption of 365.5 mW. The resolution of this TDC is about the jitter level of the circuits. The time measurement of the first hit shows a mean value of 2.93 ns with an error of 20.0 ps and $\sigma = 2.41\,\mathrm{LSB}$. However, the measurement of $T = 12.5\,\mathrm{ns}$ presents an important quantification error regarding the time resolution of 164.0 ps (the mean value is 12.336 ns). The measurements are highly affected by the jitter, which is obvious with the higher standard deviation (noise $\sigma = 3.69\,\mathrm{LSB}$).

## VI. Conclusions

The hardware implementation of the proposed TDC architecture using 0.35 µm CMOS technology allows us to further evaluate the performance and confirm the advantages of the proposed approach. Most of the measurements are perfectly in accordance with our theoretical claims. They prove the ability of the proposed TDC architecture to enhance the time resolution by increasing the number of stages. In fact, the proposed TDC achieves a mean standard deviation of measurement of 1.8 LSB for a total number of stages of 9. For this TDC, the achieved time resolution is 72.5 ps. Compared to the proposed TDCs in literature, according to the same equivalent number of stages, our TDC presents a fine time resolution [10]. The measurement results of the TDCs with 23 and 61 stages prove the time resolution enhancement by increasing the number of stages. Despite the impact of the jitter, we have been able to exploit some measurements. According to these results, we are convinced that integrating a simple calibration of the frequency will help to improve the measurements. In our case, it is important to notice that the so-called analog Charlie's effect avoid the phase calibration, which is a strong advantage compared to TDCs requiring delay calibration. Furthermore, they can be further improved by using averaging. All these points can be considered for the future works.

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