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# On the Limitations of Concatenating Boolean Operations in Memristive-Based Logic-In-Memory Solutions

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**Abstract** — *Emerging non-volatile memories are widely studied today as means to maximize energy efficiency and because they enable the so-called Computation-In-Memory. The Logic-in-Memory (LIM) paradigm is a subset of the Computation-in-Memory and it focuses on the execution of Boolean operations inside the memory. Among the most popular solutions, MAGIC and FELIX promise non-input destructive operations, as classical computation paradigms, allowing therefore to re-use the set of input data for several operations. In this paper we have analyzed the electrical behavior of some significant LIM implementations (MAGIC NOR and FELIX NAND) under various operation conditions. Our results show that it is not trivial to guarantee non-input destructive operations (in the case of FELIX NAND) and there is a real difficulty in concatenating several operations due to non-ideal intermediate results.*

**Keywords** — *Emerging technologies, Logic-In-Memory, Memristors, Non-Volatile memories*

## I. INTRODUCTION

Emerging non-volatile memories are widely studied today as means to maximize energy efficiency by eliminating the static power and reducing the data movement between memories and processors. One of the solutions to reduce the data movement is to perform operations within the memory itself (Computation-in-Memory).

The Logic-in-Memory (LIM) paradigm is a subset of the Computation-in-Memory (CIM) techniques and it focuses on the execution of Boolean operations inside the memory. There are three categories of LIM: (i) *Stateful Logic in Array*, where the logic value is encoded as resistive state and operations are performed within the memory array; (ii) *Stateful Logic in Array and its Periphery*, where operations are performed in the memory array and with modified logic in the memory periphery (i.e., sense amplifiers, address decoder, write drivers); (iii) *Non-Stateful Logic in Array and its Periphery*, where the logic values are encoded as resistive states and voltage levels [1]. Among these three classes of solutions, the first is gaining interest in the research community because it requires the least amount of modifications in the memory architecture.

*Stateful Logic in Array* solutions include *IMPLY* ([2]–[4]) having the Boolean implication as primitive operation, the *Stateful Three-Input Logic* [5] with the primitive operation *ORNOR3* (i.e., input1 OR (input2 NOR input3)), *Memristor-Aided Logic - MAGIC* [6], [7], whose primitive operations are NOT and NOR, and *FELIX* ([8], [9]) whose primitive operations are OR, NAND and XOR.

Some of the existing LIM solutions do not preserve the content of the input memristors after executing the operation (i.e., *input-destructive* operations). On the other hand, MAGIC and FELIX promise *non-input destructive* operations, as classical computation paradigms, allowing therefore to re-use the set of input data for several operations. This characteristic has been demonstrated in the state-of-the-art by assuming ideal operation conditions.

In this paper we have analyzed the electrical behavior of some significant LIM implementations (MAGIC NOR and FELIX NAND) under various operating conditions. Our results show that it is not trivial to guarantee non-input destructive operations (in the case of FELIX NAND) and there is a real difficulty in concatenating several operations due to non-ideal intermediate results. We have chosen MAGIC NOR and FELIX NAND functions since they are functionally complete, i.e., each one of them can be used to implement all logic functions in one or more steps.

The contributions of this work are:

- The in-depth analysis of the operation conditions of MAGIC NOR and FELIX NAND, with the identification of the ranges in which the operations are performed correctly, highlighting the values of control signals which lead to input-destructive operations.
- The demonstration that, while the operation is performed correctly, the resistance of the output memristor does not always reach its ideal value (either low or high).
- The demonstration that concatenating operations (i.e., using the output of one operation as input of the next operation) starting from non-ideal resistive values can lead to wrong results.

The remainder of this paper is organized as follows. Section II presents the background and the motivation of the work. Section III explains the simulation environment, and the analysis of the operation conditions for the MAGIC NOR and FELIX NAND. Section IV analyses the concatenation of operations of these two operations. Finally, Section V concludes the paper.

## II. BACKGROUND AND MOTIVATION

This chapter briefly explains the basic functioning of the targeted MAGIC NOR and FELIX NAND operations. The reader can refer to [2] and [4] for more details.

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A memristor is a two terminal device that switches between resistive states: the high resistance state (HRS or  $R_{OFF}$ ) and the low resistance state (LRS or  $R_{ON}$ ). When used as a non-volatile memory, HRS and LRS are associated with the logic values '0' and '1' respectively. Write operations are performed by applying the right amount of electrical current to allow the device to switch from one state to the other. Read operations are performed by comparing the current flowing through the device against a reference current, which is usually the mean value between the current flowing through the device in HRS and in LRS.

When memristors are used in LIM architectures, a compute operation is enabled, besides read and write operations. To perform the computation, one or several memristors (on the same word line) are electrically connected and proper control signals are applied, so that one of the memristors will reflect the output of the Boolean function.

In the case of MAGIC NOR and FELIX NAND operations, three memristors are used: 2 for the inputs and one for the output. The output memristor is initialized to the logic value '1' (LRS) before executing the logic operation. The operation is executed by applying a voltage  $V_0$  to the bit lines of the two input memristors, while the bit line of the output memristor is connected to ground. Based on the amplitude and the duration of  $V_0$ , the output memristor will contain the result of the NOR or the NAND operation.

The equations defining the amplitude of the control voltage  $V_0$  are reported below, where:

- $V_{T,OFF}$  is the memristive threshold voltage to switch from LRS to HRS
- $V_{T,ON}$  is the memristive threshold voltage to switch from HRS to LRS
- $\parallel$  represents the parallel configuration of resistances.

For the MAGIC NOR the equation is:

$$2V_{T,OFF} < V_0 < \min \left[ \frac{R_{HRS}}{2R_{LRS}} V_{T,OFF}, |V_{T,ON}| \right] \quad (1)$$

while for the FELIX NAND:

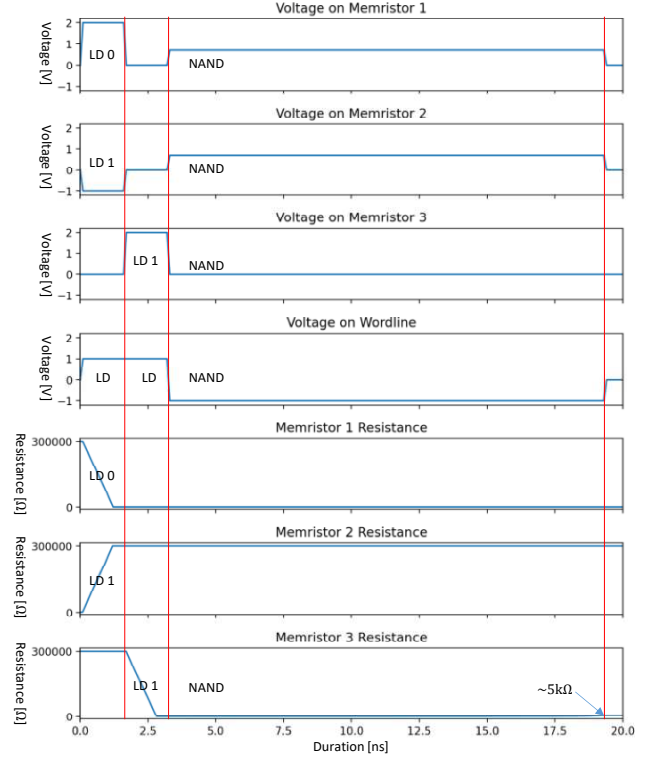
$$\frac{V_{OFF}}{R_{LRS}} \left\{ R_{LRS} + \left( R_{HRS} \parallel \frac{R_{LRS}}{3} \right) \right\} < V_0 \quad (2)$$

$$< \frac{V_{OFF}}{R_{LRS}} \left\{ R_{LRS} + \left( R_{HRS} \parallel \frac{R_{LRS}}{2} \right) \right\}$$

While these equations give a range of theoretical values for the control voltage amplitude, the duration of the control voltage strongly depends on the dynamics of the memristor, but it is difficult to derive its analytical expression. Therefore, to identify the combinations of control voltage amplitude and duration for which the operation is performed successfully, we have resorted to electrical simulations.

While performing the electrical simulations, we have identified 4 scenarios: (1) the operation has been performed correctly without any effect on the input; (2) the operation has been performed correctly but the information on the input was lost; (3) the operation has been performed correctly but the resistive state of the output memristor did not reach the nominal HRS or LRS, as shown in Figure 1; (4) the operation has failed.

The third scenario has led us to the assumption that concatenating operations where the output of the first operation (which did not reach the nominal HRS or LRS) is used as input for the next operation, might lead to a wrong result. We proved this assumption right as thoroughly explained in Section IV.



**Figure 1** – Waveform of a FELIX NAND operation, where the final resistive state does not reach the nominal LRS. LD is the load operation on a memristor (set if LD 1, reset if LD 0). At the end of the NAND operation, the final resistive value of the output memristor (memristor 3) is not 1kΩ as expected, but 5kΩ. The vertical red lines indicate the start of the next operation.

## I. SIMULATION ENVIRONMENT AND ANALYSIS

MAGIC NOR and FELIX NAND operations have been simulated in Cadence Spectre using the VTEAM memristor model [10], with the internal parameters suggested for MAGIC (see Table 1 – VTEAM model parameters). Memristors have been set up to have nominal HRS equal to 300kΩ (logic value '0') and nominal LRS equal to 1kΩ (logic value '1'),  $V_{T,OFF} = 0.3V$  and  $V_{T,ON} = -1.5V$ .

Name	Description	Value
model	Memristor model - VTEAM	4
window_type	window function - no window	0
dt [s]	numeric simulation time step (for Cadence Virtuoso)	1E-12
init_state [0:1]	The initial state of the state variable	0
Roff [Ω]	Memristor's maximum resistance	300000
Ron [Ω]	Memristor's minimum resistance	1000
D [m]	Physica width of the memristor	3E-09
w_multiplied	A normalization for the state variable (for Cadence Virtuoso)	1E+08
p_coeff	The value of p in the window functions	2
p_window_noise	A small noise to avoid boundary problems in window functions (for Cadence Virtuoso)	1E-18
x_c [m]	Normalized length for Simmons tunnel barrier	1.07E-10
a_on [m]	Upper bound of undoped region (Simmons tunnel barrier)	2E-09
a_off [m]	Lower bound of undoped region (Simmons tunnel barrier)	1.2E-09
K_on [m/s]	kon in TEAM	-216.2
K_off [m/s]	koff in TEAM	0.091
Alpha_on	Nonlinearity power coefficient for TEAM	4
Alpha_off	Nonlinearity power coefficient for TEAM	4
v_on [V]	Threshold voltage in VTEAM	Von
v_off [V]	Threshold voltage in VTEAM	Voff
x_on [m]	Lower bound of undoped region (TEAM)	0
x_off [m]	Upper bound of undoped region (TEAM)	3E-09

**Table 1** – VTEAM model parameters

Theoretical values for  $V_0$  (calculated with Eq. (1)) range between 0.60V and 1.50V for the NOR operation, and between 0.40 and 0.45V for the NAND operation (calculated

with Eq. (2)). To perform the in-depth analysis, the input voltage has been swept from 0.20V to 2V with a step of 0.1V. Based on published results about the duration, we considered all durations ranging from 0.25ns to 20ns with a step of 0.25ns.

For each control voltage setup (i.e., couple of amplitude and duration) we have simulated the execution of MAGIC NOR and FELIX NAND functions applying all input combinations (i.e., 00, 01, 10, 11) and the final state of the three memristors (the two inputs and the output) have been stored and analyzed.

The results for the MAGIC NOR are shown in Figure 2. For each combination of voltage amplitude and duration, we have plotted the outcome of the operation by using the following color scheme:

1. Dark green, when the operation has been performed correctly for all 4 input combinations, and the input memristor did not lose their state (non-input-destructive operation).
2. Light green, when the operation has been performed correctly for all 4 input combinations, but at least one of the input memristor lost its state for at least one input combination (input-destructive operation).
3. White: the output is wrong for at least one input combination.

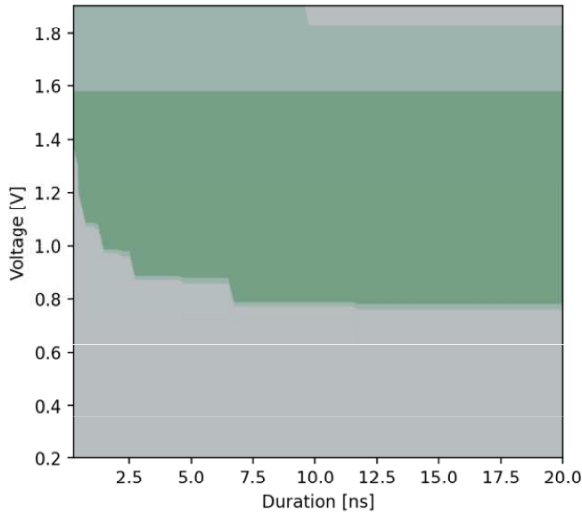


Figure 2 – NOR Operation

Results in Figure 2 – NOR Operation are in agreement with the theoretical analysis. Indeed, we observed correct operations when the voltage amplitude ranges between 0.7V and 1.55V. The slight difference is due to the parameters of the memristive model we used.

For the FELIX NAND, no combinations of amplitude and duration have generated correct results. This can be due to the fact that the theoretical voltage range for correct operation is very narrow, and to a non-optimal setup of the memristive model.

## II. ANALYSIS OF WORKING RANGES

In the previous section, we have considered as correct result only the cases where the output memristor reaches exactly the nominal values of HRS or the LRS. This explains why all NAND operations were considered flawed and the range of control voltages for correct NOR operations is narrower than the theoretical one. Nevertheless, on a closer analysis, we have observed that combinations of amplitude

and duration exist for which the output memristor reaches resistive values close to the nominal HRS or LRS (close enough so they can be read as correct logic values). We have defined these states as *weak HRS* and *weak LRS*.

Due to this observation, we updated the conditions for an operation to be considered correct, i.e., an operation is correct if the resistive value of the updated memristor is between *weak HRS* and nominal HRS when a logic 0 is expected and between nominal LRS and *weak LRS* when a logic 1 is expected. Figures Figure 3 and Figure 4 show the color-coded space of control voltages for the FELIX NAND operation, under 2 different groups of weak values: in Figure 3 *weak LRS*=1.3k $\Omega$  and *weak HRS*=290k $\Omega$ , while in Figure 4 *weak LRS*=50k $\Omega$  and *weak HRS*=150k $\Omega$ .

It is worth noticing that the higher the distance between nominal and weak state, the larger the control voltage range where the LIM operation is considered correct. This knowledge can lessen the restrictions on the voltage regulators (to generate the control voltages).

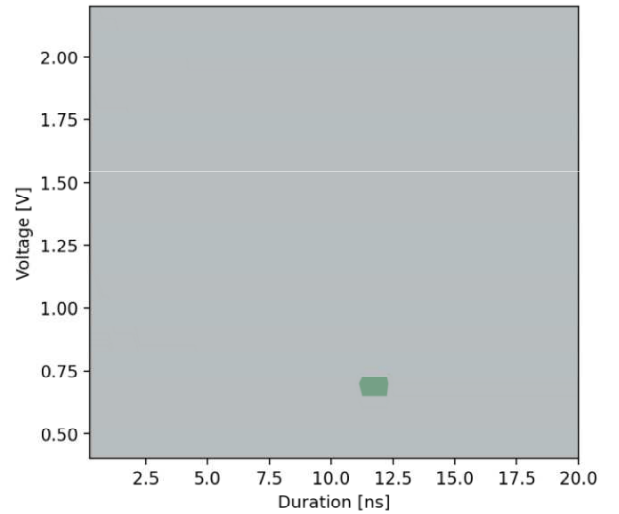


Figure 3 – NAND operation with *weak LRS*=1.3k $\Omega$  and *weak HRS*=290k $\Omega$  for reading the output value

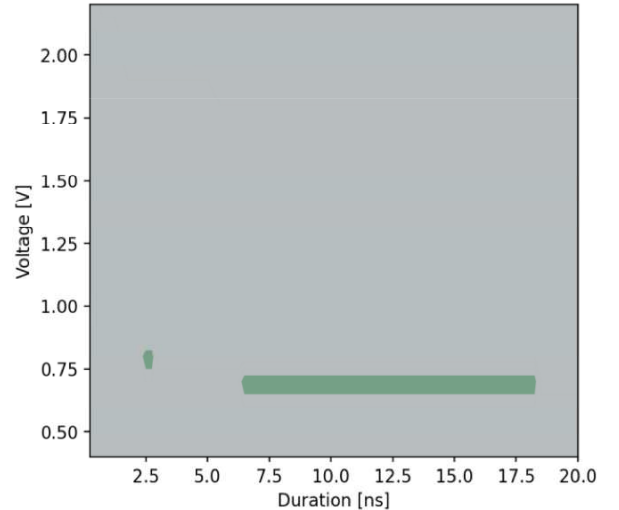


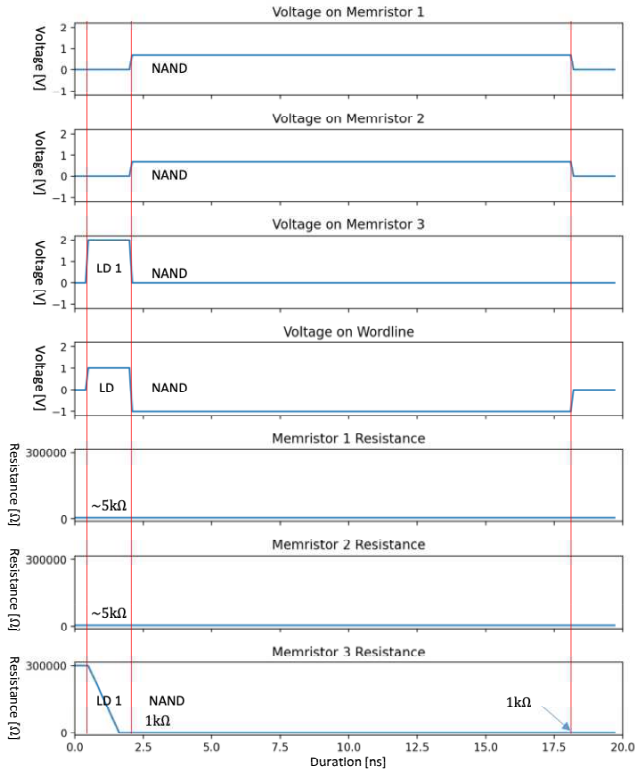
Figure 4 – NAND operation with *weak LRS*=50k $\Omega$  and *weak HRS*=150k $\Omega$  for reading the output value

## III. CONCATENATION OF OPERATIONS

One of the interesting aspects of LIM solutions such as MAGIC and FELIX is that the entire operation is done

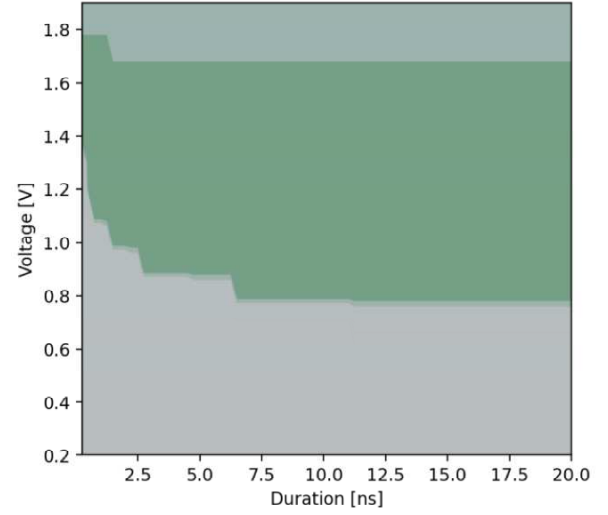
without the need to take the data outside of the memory. As a consequence, doing consecutive operations can enable a significant performance speed-up. But if one or both inputs are the result of a previous operations, the operation itself might not behave correctly.

We analyzed the effect of a weak state as input in both NOR and NAND operations. We repeated the simulations done to study the operations, but considering weak states in the input memristors. We have considered two cases: (i) weak states have been chosen from the output resistive values obtained during the NAND operation shown in figure 3; (ii) the weak LRS has been chosen from the output resistive values obtained during the NAND operation shown in Figure 4, while the HRS has been kept in the nominal value. In the first case, weak HRS is equal to  $297.5k\Omega$  and weak LRS is equal to  $1225\Omega$ . In the second case, weak LRS is equal to  $5K\Omega$ .

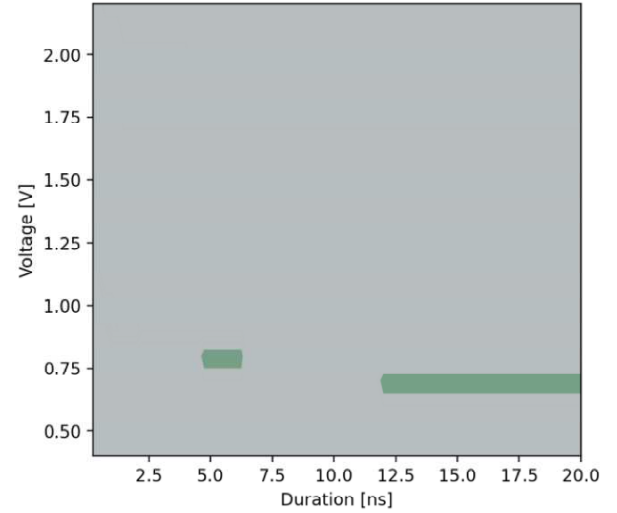


**Figure 5** – Waveform of a FELIX NAND operation having the input memristors with *weak LRS*= $5k\Omega$ . As it can be seen, instead of the expected logic 1 ( $300k\Omega$ ), it is obtained as a result a logic 0 ( $1k\Omega$ ): the memristor cannot change its resistive value due to the too high resistive value of the inputs. The NAND operation is therefore failed.

For the first case, simulations have been performed with weak states in both input memristors and have shown that the operations still work. The NOR and the NAND operations can be seen in figures Figure 6 and Figure 7 respectively. While for the NOR operation there are no remarkable differences, in the case of the NAND operation the working conditions are different from the case where both inputs are initialized with the nominal values. More in particular, the dark green regions in Figure 4 and Figure 7 only partially overlap. This knowledge hardens the restrictions on the voltage regulators (to generate the control voltages), since it reduces the range of voltages for which the operations are correctly executed when considering concatenation.

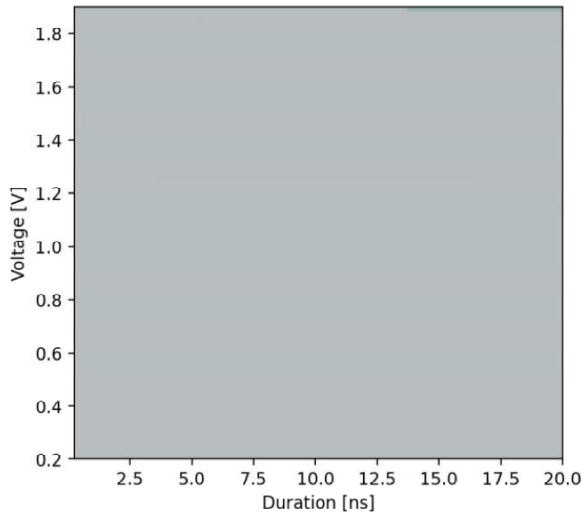


**Figure 6** – NOR operation with weak state inputs ( $1225\Omega$ ,  $297.5k\Omega$ ), and with *weak LRS*= $1.3k\Omega$  and *weak HRS*= $290k\Omega$  for reading the output value

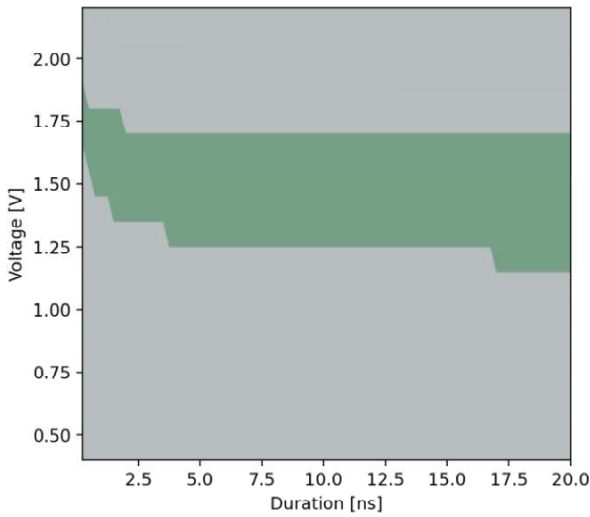


**Figure 7** – NAND operation with weak state inputs ( $1225\Omega$ ,  $297.5k\Omega$ ), and with *weak LRS*= $1.3k\Omega$  and *weak HRS*= $290k\Omega$  for reading the output value

For the second case, we considered the inputs initialized to the weak LRS of  $5K\Omega$  and nominal HRS. This case is illustrated in the waveform of Figure 5. In this case the NOR operation did not work for any combination of voltage amplitude and duration, as seen in Figure 8. However, the NAND operation worked, with a larger range of voltages, as shown in Figure 9. Nevertheless, there are no common values of control signals for which the NAND operation is performed correctly when considering nominal and weak states. As a consequence, the operation cannot work.



**Figure 8** – NOR operation with weak state inputs ( $5k\Omega$ ,  $300k\Omega$ ), and with weak  $LRS=50k\Omega$  and weak  $HRS=150k\Omega$  for reading the output value



**Figure 9** – NAND operation with weak state inputs ( $5k\Omega$ ,  $300k\Omega$ ), and with weak  $LRS=10k\Omega$  and weak  $HRS=290k\Omega$  for reading the output value

#### IV. CONCLUSIONS

In this paper we have analyzed the electrical behavior of some significant LIM implementations (MAGIC NOR and FELIX NAND) under various operating conditions. Our results showed that:

- while operations are performed correctly from a logic point of view, the resistance of the output memristor does not always reach its ideal value;
- the higher the distance between nominal and weak state, the larger the control voltage range where the

LIM operation is considered correct. This knowledge can lessen the restrictions on the voltage regulators (to generate the control voltages);

- the ranges in which the operations are performed correctly can be narrow, and they depend on the resistive value of the input memristors;
- concatenating operations (i.e., using the output of one operation as input of the next operation) starting from non-ideal resistive values can lead to wrong results. To overcome this problem, refresh cycles should be added at the end of every logic operation to restore the resistive state to its nominal value (either HRS or LRS) in order to guarantee the correct result of complex calculations.

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