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# Comparison of One and Two Stage RF Rectifiers Designed in FDSOI 28 nm and BiCMOS 55 nm

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**Abstract**— The context of this article is a low power application: RF energy harvesting. In this paper, we compare performances of two Dickson voltage rectifiers realized with two different technologies: FDSOI 28 nm and BiCMOS 55 nm. The measurement of I-V characteristics of diodes in both technologies reveals that FDSOI shows a smaller threshold voltage and less leakage current compared to BiCMOS. It is also ascertained through the measurement results that the efficiency of the rectifier realized with the FDSOI is better than that of rectifier obtained using BiCMOS. Furthermore, the impact of back gate polarization (BGP) in FDSOI is investigated and a novel dynamic BGP is proposed. Power conversion efficiency (*PCE*) of 44 % is achieved in FDSOI, whereas, a *PCE* of 37 % is observed in BiCMOS.

**Keywords** : Radio-frequency energy harvesting, FDSOI 28 nm, dynamic back gate polarization, integrated circuit.

## I. INTRODUCTION

The next internet revolution already on the way, will be Internet of Things (IoT) with a large number of wireless micro sensors spread in our environment to monitor our “life” in a more cleverly way (health, security, transportation, energy...) [1-2]. The drawback of IoT is their power: “How supply these without spreading pollution around us due to dispersion of heavy metal in their battery?” Although, thanks to recent improvements in last microelectronic technologies new circuits are now able to consume very low electrical power level. For example, a 32 bits, 50MHz, ultra-low voltage microcontroller can be powered by only 0.37V and requires a sleep power around 50 nW [3]. In the same time, average RF power density of Wireless Local Area Network (WLAN) or Global System for Mobile Communications (GSM) can now reach up to 10 nW/cm<sup>2</sup> as shown in [4]. Moreover, in wireless circuit, antenna occupies a large volume of the IoT for a small time of use (less than one minute per day). The idea is to reuse the antenna to harvest the ambient RF energy and relieve the battery. The lifetime of the battery of IoTs could be reinforced.

To convert RF to DC non-linear elements need to be used, usually Schottky diodes, but a sensitivity of -40 dBm at

2.45 GHz has been obtained with tunnel diodes [5]. Howbeit, these types of diodes are still difficult to integrate in microelectronic technologies and circuits. Recently a three stages voltage multiplier, designed in 0.18  $\mu$ m CMOS technology which can achieve 1 V output voltage for an input power of -27 dBm [6].

In this paper, we compare measured performances of two RF-DC converters design with two technologies: one is one of the latest bulk BiCMOS 55 nm technology and the second one is the FDSOI 28 nm described as well adapted to low power applications. This article is organized in four parts: this brief introduction, a description of the RF-DC converter principle, design method, measurements results and a conclusion.

## II. RECTIFIER PRINCIPLE

RF-DC conversion is based on diodes, alternatively known as charge pumps. Croft-Walton charge pump was modified by Dickson to reduce the parasitic capacitances at the transitional nodes between the different stages [6]. Moreover, this charge pump is more suitable for integrated circuits [7]. A two-stage Dickson voltage rectifier is presented in Figure 1. The power conversion efficiency (*PCE*) is one of the most important parameters to define the efficiency of such a circuit. This parameter is defined by:

$$PCE = \frac{(V_{out})^2}{R_{Load}} \frac{1}{P_{RF,abs}} \quad (1)$$

The maximum output voltage of an  $n$  stages Dickson multiplier, without load resistance, is estimated to be:

$$V_{out} = 2 \cdot n(V_{RF,max} - V_{th}) \quad (2)$$

where  $V_{RF,max}$  and  $V_{th}$  represent the maximum input RF voltage and the threshold voltage of a transistor respectively. In this estimation, to simplify the study, the threshold voltage is considered the same for different transistors. Furthermore, leakage currents are not taken into consideration.

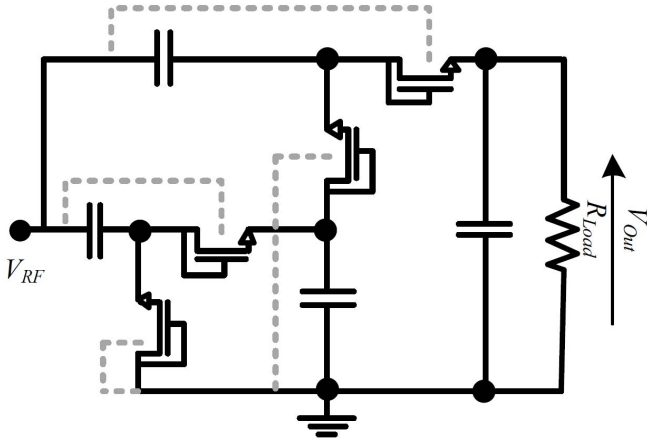


Fig. 1. Two stages Dickson voltage rectifier with a load resistance  $R_{Load}$  at the output.

### III. DESIGN METHOD IN BiCMOS AND FDSOI

To design integrated RF-DC rectifiers, it is necessary to replace Schottky by transistors configured as a diode (gate connected to the drain as shown in Figure 1). Classical bulk microelectronic technology, e.g., BiCMOS is widely used for integrated circuits. Nonetheless, it suffers from parasitic and leakage currents in the substrate due to reduction of transistor size. On the other hand, FDSOI is a promising alternative, in which, a buried oxide layer (BOX) is placed between the active area and the bulk to reduce parasitic capacitances between the source and the drain. Owing to the introduction of the BOX; (i) the electrons flowing from the source to the drain are efficiently confined, reducing leakage currents, (ii) a bulk polarization (BGP) allows to control leakage current and the threshold voltage. One and two-stages rectifiers are realized in BiCMOS 55 nm and FDSOI 28 nm technologies. The transistors are chosen to reduce losses in the circuit. The dimensions are  $140\text{ }\mu\text{m} \times 30\text{ nm}$  for FDSOI transistors and  $280\text{ }\mu\text{m} \times 60\text{ nm}$  for BiCMOS transistors. To reduce the series resistance, transistors with interdigitated fingers are used. On the other hand, the  $(W, L)$  ratio is conserved for transistors in both technologies.

In FDSOI technology, it is important to use the back gate bias, which represents a new degree of flexibility and additional control over transistors characteristics. As described in [8], the I-V characteristics, measured for a N-type transistor, and for different back gate bias, show that when a negative bias is applied, the threshold voltage increases and the leakage currents decrease and vice versa. So it is not possible to ensure a low threshold and less leakage at the same time with a fixed bias. Furthermore, for the P-type transistors, the threshold voltage is higher than that measured with N-type which is not advantageous for the RF-DC circuits.

To boost the performance, N-type transistors will be used with dynamic back gate polarization [9]. This kind of bias provides additional control of the leakage currents when the transistors are reverse polarized and ensures a low threshold voltage and a small voltage drop across the transistors when they are in direct polarization.

### IV. MEASUREMENTS RESULTS

In this section, the measurement and simulation results of the static characteristic for two transistors connected as a diode, designed in FDSOI and BiCMOS, are represented. In addition, simulation and measurement results of two-stage Dickson multiplier designed in both technologies are depicted. Furthermore, a comparison between one and two-stage of Dickson multiplier designed in FDSOI is showed to figure the effect of increasing the number of stages on performance.

#### A. FDSOI vs. BiCMOS

Figure 2 shows the measurement and simulation results of I-V characteristics of a transistor configured as a diode in both technologies. In the direct polarization, the threshold voltage of the transistor in FDSOI technology is smaller than that in BiCMOS. However, for a reverse voltage polarization smaller than 0.6 V, FDSOI transistor has leakage currents marginally greater than those of BiCMOS. Nevertheless, the leakage currents of BiCMOS become much larger than that of FDSOI if the reverse bias is beyond that value.

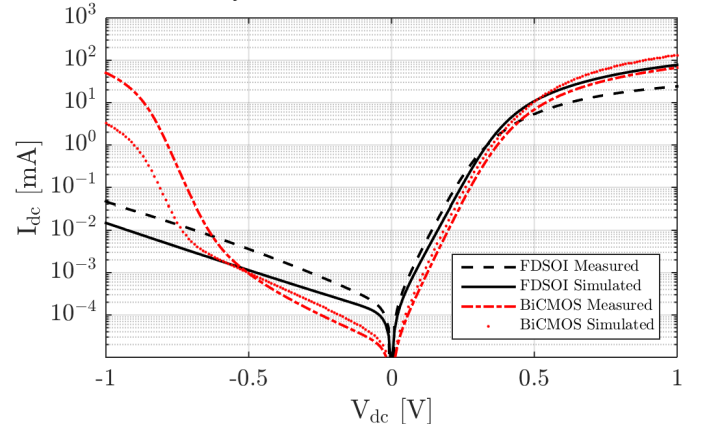


Fig. 2. I-V characteristics in FDSOI and BiCMOS technology for a N-type transistor connected as a diode

Figure 3 represents the measurement setup to characterize the RF-DC devices. These measurements are performed using a manual station with infinity probes of  $50\text{ }\mu\text{m}$  pitch. In our study, we are interested to measure the intrinsic efficiency of the rectifiers in both technologies, and not to improve the impedance matching. The impedance matching ensures higher conversion efficiency with better sensitivity to low input power. For this reason, an S-parameters measurement, provided by a vector network analyzer (VNA), is important to estimate the absorbed power. The VNA is used to generate an RF power at 2.4 GHz.

The maximum *PCE* measured in both technologies for different input powers is shown in Figure 4. The maximum *PCE* achieved with two stages rectifier designed on FDSOI is 44 % at 3 dBm. On the other hand, with BiCMOS, the maximum of *PCE* is 37 % at 2 dBm. Additionally, in FDSOI, the BG is dynamically polarized which improves the performance. Furthermore, the simulation and the measurement results are in close agreement with each other.

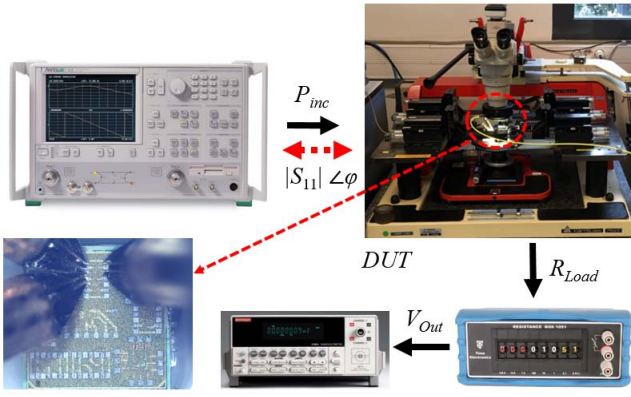


Fig. 3. Representation of the setup for the characterization of RF-DC circuits.

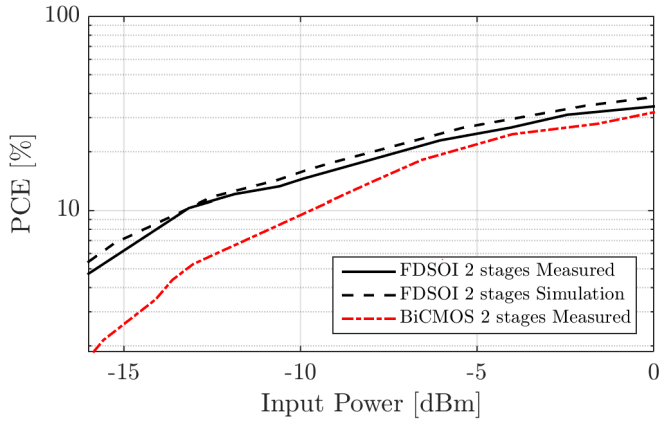


Fig. 4. Comparison of the maximum  $PCE$  vs. input power measured for two-stage rectifiers realized in FDSOI and BiCMOS technology

Figure 5 represents the  $PCE$  measured for both technologies as a function of the load resistance for same input power (0 dBm). The maximum  $PCE$  achieved is 35 % and 28 % with an  $R_{Load}$  of 10 k $\Omega$  and 7 k $\Omega$  for FDSOI and BiCMOS, respectively.

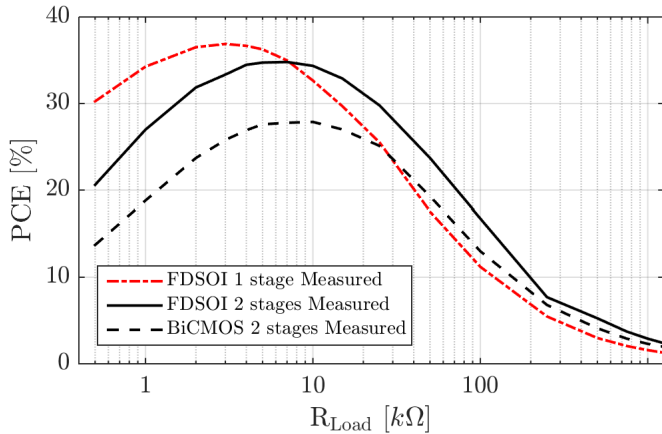


Fig. 5. comparison of the  $PCE$  vs.  $R_{Load}$  for two stages Dickson rectifier designed in FDSOI and BiCMOS technology

### B. One and two-stage of Dickson rectifier in FDSOI

In this section, a comparison between one and two-stages rectifiers is performed. The transistors used have the same size for both rectifiers. Figure 6 represents the measured output voltage for both rectifiers with respect to the load resistance. This result is obtained using the same input power. For the small load resistance, the output voltage achieved with one stage is slightly bigger than what is obtained with two stages. Whereas, for higher load resistance, the output voltage obtained with two stages is bigger than that of one. Moreover, the output voltage achieved with one and two stages reach a steady state for high resistance. This value is almost equal to that obtained when the load resistance is replaced by an open circuit. Note that the higher output voltage of the two stages is almost the double of one stage.

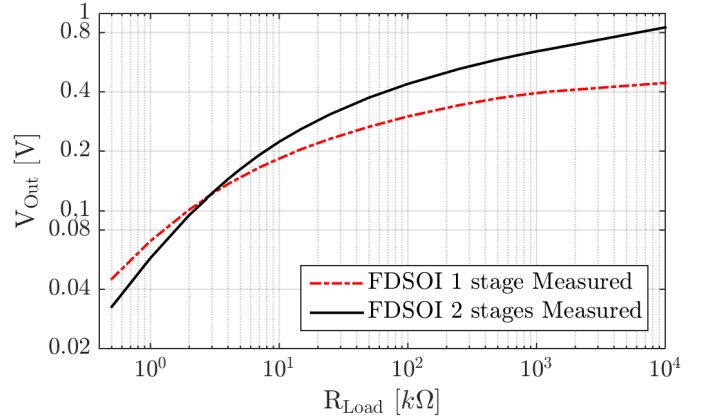


Fig. 6. Measurement result of one and two-stage rectifier in function of load resistance

As shown in Figure 5, the maximum  $PCE$  for two-stage rectifier is obtained for load resistances that are bigger than those of a single stage. This shift is due to the fact that the two-stages rectifier, can deliver an output voltage bigger than that of one stage, for higher load resistance as shown in Figure 6.

In addition, for a single stage, the  $PCE$  is slightly higher than that of two stages. This degradation is due to the fact that the output voltage is not exactly the double of that of a single stage, because of the voltage drop across the two transistors added for the second stage, and also because of leakage currents. So, by increasing the number of stages, the maximum of the  $PCE$  cover higher load resistance, but the maximum value of the  $PCE$  will decrease because of the voltage drop and leakage current.

### CONCLUSION

This paper describes the design of one and two stages of RF rectifiers for energy harvesting. One has been designed in the bulk technology, BiCMOS 55 nm, and the other one SOI technology, FDSOI 28 nm. These rectifiers have been optimized to reduce losses, especially for transistor equivalent series resistance. Static I-V diode measurements represent a lower threshold voltage and less leakage current for FDSOI technology compared to that of BiCMOS. On the other hand, a  $PCE$  of 35 % is obtained in FDSOI rectifier against a  $PCE$  of 28 % for BiCMOS rectifier for the same conditions (an input RF

power 0 dBm @ 2.45 GHz with an  $R_{Load}$  of 10 k $\Omega$  and 7 k $\Omega$  respectively). Furthermore, by increasing the number of stages of a rectifier, the maximum *PCE* is obtained with higher load resistances, since the output voltage of the rectifier can reach higher values. In addition, FDSOI is an appropriate technology for energy harvesting due to the low threshold voltage, less leakage currents and an appropriate use of the thanks to the Back Gate which can improve the *PCE*.

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