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# 10Gbps Length adaptive on-chip RF serial link for Network on Chips and Multi-processor chips applications

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**Abstract**—This paper introduces the use of duo-binary modulation for a 10-Gbps RF on-chip long range serial link. RF signaling is used to reduce the delay so that a 5 mm line is crossed in less than 50 ps. Furthermore, the duo-binary approach is used to reach higher bandwidth efficiency since this modulation uses a two-time smaller bandwidth for the transmission. The RF design complexity is also reduced thanks to duo-binary modulation.

**Keywords**—component; RF serial link; duo-binary modulation.

## I. INTRODUCTION

Transistor scaling allowed achieving higher density packing of devices along with faster transistors. However, the performance of the interconnections did not follow the trend and is today the main bottleneck for high-speed transceivers developments. Higher transistor density also implies higher wires density. In that context, RF link still leads to the best solution for “on chip” long range connections [1]. However, wires are more sensible to their environment as compared to active devices, i.e. closer wires are more sensible to crosstalk and longer  $RC$  delay due to wires switching in opposite polarity for example.

One other main issue in communication systems is distortion due to the channel physical properties. This might be due either to the dispersive nature of the channel where the frequency components propagate at different velocities, or due to an increase in the attenuation coefficient of the channel due to the skin effect for example. The attenuation is much higher for high frequencies components and causes the pulse traveling through the channel to both decrease in amplitude and spread in time domain.

Several methods have been carried out in order to solve these issues. Equalization was used to reduce the frequency selectivity of the channel by reversing the distortion [2]. Then reconstructing the original transmitted signal, the coefficients for the equalizers can be either fixed for a time-invariant channel using training sequences or after an estimation of the channel. Otherwise, to reverse the effect of the time-varying channel an adaptive equalization is required where a known training sequence is inserted periodically, then algorithms such as least mean square are used to update the coefficients of the equalizer [3]. For a fixed channel, to reach higher data rates, larger bandwidths in the base band have to be equalized,

or more complex modulations such as PAM-4 can be used. However, several comparators are required for PAM modulation and more complex filters and algorithms are required for equalization. Moreover, the complexity and power consumption of the equalizers dramatically increased in the last years. The equalization approach was attractive with the transistor and voltage scaling, which is not optimal anymore since voltage scaling is slowing down. Thus the complexity of the system limits the reachable data rates.

In this work, to answer these issues, an approach inherited from [4] using a modulated RF carrier and suitable for long-range links up to several mm length is proposed. For a proof-of-concept, a 10 Gbps length adaptive serial link for large digital ICs is designed.

Using both RF and Base band signaling on the same transmission line is possible [5]-[6] to achieve higher data rate than only base band signaling. RF-band offers much higher available bandwidth with low latency. Hence it can be implemented as a solution for traffic bottlenecks in Network on Chip (NoC) for example. Herein, a 60-GHz carrier is proposed to transmit the data. RF transmission line was chosen because the group delay of the channel is almost constant over a wide bandwidth. Thus the signal travels at the same speed that is equal to half the speed of light when considering standard Back-end-of-lines, leading to low propagation delay as compared to  $RC$  delay encountered at lower frequencies.

Next, to make use of the bandwidth efficiently a pre-encoded duo-binary modulation [7] is proposed to compress the spectrum of the signal and thus use a two time smaller bandwidth. The pre-encoded duo-binary modulation leads to relaxed design constraints on the RF components compared to a NRZ modulation. Only half of the NRZ bandwidth is used. In addition, this duo-binary modulation could be used with a simple power detector without any local oscillator in the receiver.

The paper is organized as follows. After this introduction, the system architecture is described in Section II. Then, the serial link parameters are outlined in section III. The duo-binary modulation and differential pre-encoder are detailed in section IV along with simulation results, and the paper is concluded in section V.

## II. SYSTEM ARCHITECTURE

The proposed system is described in Figure 1 and is detailed in this section. The binary data goes through the differential pre-encoder, which consists in a simple modulo-2 addition. This step is used to cancel the propagation error that can be introduced by the duo-binary modulation and to simplify the demodulation. Next the duo-binary encoder introduces controlled Inter Symbol Interference (ISI) between the previously sent bit and the present bit to compress the spectral density closer to the DC. Next the 60-GHz carrier is modulated and transmitted over differential transmission lines.

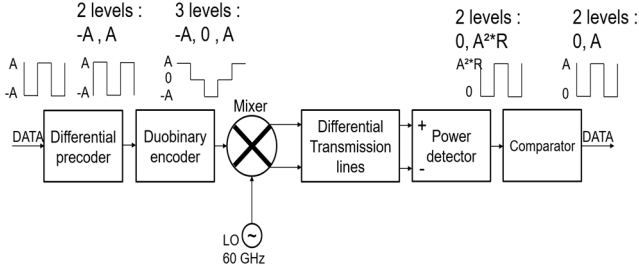


Figure 1. Proposed system architecture.

The proposed approach can be used for both single ended and differential lines. A differential transmission line was used herein because it is less sensitive to crosstalk and electromagnetic interference generated by nearby signals [8].

The amplitude of the received signal depends on both the transmitted power, which is considered as constant, and the attenuation of the transmission line, which is proportional to its length. An RMS power detector is used to demodulate the received signal and thus generate a 10 Gbps baseband signal from the received signal. Hence, the generated signal is a square function of the received signal amplitude. This operation also allows reducing the number of possible states from three to two as explained in the following sections.

Finally, the power detector output is compared to a threshold to generate the data for the following stage.

## III. SERIAL LINK PARAMETERS

### A. Differential Transmission Line used for the Link

On-chip interconnects offer a rather constant propagation speed at mm-waves, as shown in Figure 2, where a 50- $\Omega$  microstrip line was simulated using the highest metal layer with the ground in M9 using the 10 Metal layers stack from STMicroelectronics 28-nm FD-SOI technology. The phase velocity increases rapidly from few MHz up to about 10 GHz. Then, from 10 GHz up to 60 GHz, the phase velocity increases only by 7%, meaning low dispersion.

Hence, for large bandwidth transmissions, a flat group delay is obtained, leading to reduced distortion and ISI as compared to a base-band transmission, as mentioned in the introduction. The transmission line is designed in the BEOL with SiO<sub>2</sub> substrate with a relative dielectric constant equal to 4, leading to a signal that propagates with half the speed of

light, (i.e.  $1.5 \cdot 10^8$  m/s). Thus 5-mm on-chip length can be traveled in less than 50 ps.

Furthermore, for an appropriately matched transmission line, its delay can be linearly related to its length. Hence, the main characteristics of the propagation channel (attenuation and delay) are easily predictable and can be anticipated in the floorplan and design steps of the ICs. For the present case, the differential microstrip line uses 4.2- $\mu$ m wide strips with a 10- $\mu$ m spacing, leading to a 1.1-dB/mm attenuation at 60-GHz. Higher performance could be reached, but at the expense of larger footprint.

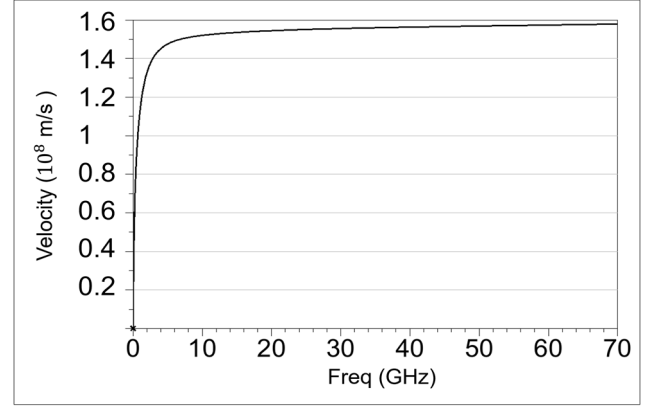


Figure 2. Propagation speed (phase velocity) in a 50- $\Omega$  transmission line.

### B. Main Performance Parameters

In this work, to simplify the use of serial links in large digital ICs, a length adaptive link is proposed to cover a large range of distances with the same transceiver without any requirement of repeater, thus limiting both power consumption and system complexity. For different link lengths, several parameters vary. The most important ones are the propagation delay, the receiver gain, and the noise figure of the transmission line, i.e. its insertion loss, which directly impact the Signal to Noise Ratio (SNR) and Bit Error Rate (BER) of the system.

For simplification reasons, let us consider a simple cascaded system of a transmitter (Gain  $G_1$ , and noise figure  $F_1$ ) and the transmission line (attenuation  $A_2$ ) only. The noise figure of the cascaded system  $F_{casc}$  can be written as:

$$F_{casc} = F_1 + \frac{(A_2 - 1)}{G_1} \quad (1)$$

where  $F_1$  is the noise figure and  $G_1$  is the gain of the transmitter, respectively, which are considered as constant.

## IV. MODULATION

NRZ modulation serial links have been proposed [4]-[5]. NRZ is a low-complexity modulation, since the data is coded into two states, the main disadvantage of this modulation is its spectral efficiency, as it is not as efficient as more advanced modulations such as PAM4 or duo-binary modulations. Duo-binary modulation was considered in this

work because it has the same spectral efficiency as PAM-4 but with lower complexity, less comparators and less constraints on the linearity of the transmitter for example .

### A. Duobinary modulation

Duo-binary modulation is part of the poly-binary modulations invented by Adam Lender in 1963 [7]. It can theoretically double the data rate transmitted through a channel bandwidth BW, where ISI is introduced in a controlled matter to be removed at the reception. In its general form, the duo-binary modulation output bit  $y_k[n]$  as defined in equation(2) as the sum of the previous bit  $x_k[n - 1]$  and the present bit  $x_k[n]$  to be sent. It is described in Figure 3.

$$y_k[n] = x_k[n] + x_k[n - 1] \quad (2)$$

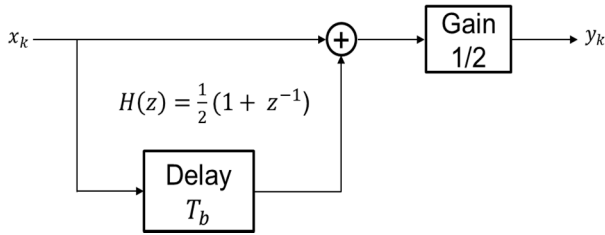


Figure 3. Duo-binary modulation principle.

A 10 Gbps pseudo-random binary sequence coded in NRZ where  $x_k = \pm 200$  mV was used, as shown in Figure 4. In time domain, the duo-binary modulation results in an output signal with three levels, instead of the two levels of NRZ modulation.

Considering simple duo-binary demodulation, for  $r_k = \pm 200$  mV where  $r_k$  is the received signal, the received bit is easily distinguishable since it can either take the value  $r_k = 200$  mV for a binary “1”,  $r_k = -200$  mV for a binary “0”, for  $r_k = 0$ V the received bit is decided by inverting the previously received bit .

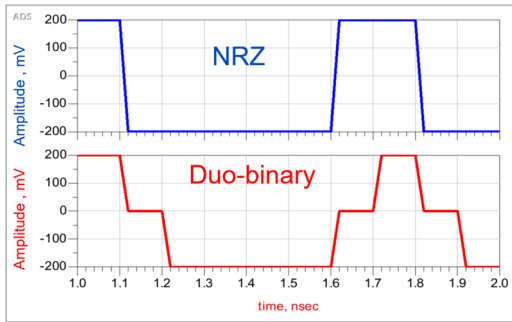


Figure 4. Example of duo-binary modulation output in time domain.

The spectral power density is shown in Figure 5. Note that the duo-binary modulation compresses the main lobe of the spectrum to half the bandwidth used by NRZ modulation. This was demonstrated in [7], with equations (3) and (4) giving the utilized spectrum for duo-binary and NRZ modulations, respectively.

$$W_{duobinary} = \frac{T}{4} \left( \frac{\sin(2\pi fT)}{2\pi fT} \right)^2 \quad (3)$$

$$W_{NRZ} = \frac{T}{4} \left( \frac{\sin(\pi fT)}{\pi fT} \right)^2 \quad (4)$$

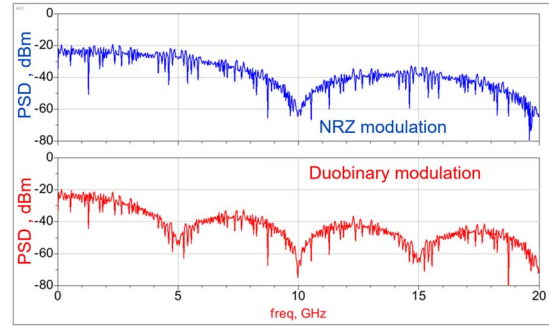


Figure 5. Power spectral density for NRZ and duo-binary modulations.

### B. Differential pre-encoder

The main drawback of duo-binary modulation is the propagation of an error to the next bits. To avoid this propagation error, a pre-encoder is required, this precoding is a modulo-2 addition operation. It can be realized using a XOR logic gate as follows:

$$x_k = x_{k-1} \oplus d_k \quad (5)$$

with  $\oplus$  the modulo-2 addition (XOR logic operation). Using this precoding, as shown in the simple scheme in Figure 6, the duo-binary output states becomes binary “0” for  $y_k = \pm 200$  mV and binary “1” for  $y_k = 0$ V.

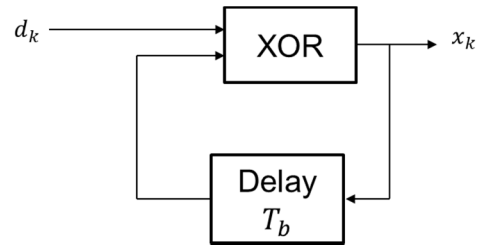


Figure 6. Differential pre-encoder scheme.

### C. Self-mixing operation

As mentioned before, a self-mixing operation at the receiver was used to relax the carrier synchronization where no PLL or VCO are used at the receiver, furthermore the self-mixing combined with the previously explained precoding and duo-binary modulations leads to a simpler demodulation process.

Before demodulation a three states signal is received:  $y_k = \{-A * \sin(2\pi ft), 0, A * \sin(2\pi ft)\}$ , where  $y_k = 0$ V refers to a binary “1”, while the two remaining states refer to binary “0”.

With a self-mixing operation, the number of states after demodulation can be reduced to two states  $y_k = \{0, kA^2\}$  only. Hence, the recovered signal can be treated as

a binary signal that can be compared to a threshold to generate the required amplitude for the following stage.

#### D. Simulation results

In Figure 7, simulation results in time domain are shown. The signal states through the system can be seen. First line,  $d_k$  is the binary data to be sent. Next,  $y_k$  is the duo-binary pre-encoded data used to modulate the 60 GHz carrier,  $m_k$  is the modulated signal before self-mixing, and  $r_k$  is the received self-mixed signal. The retrieved data after demodulation is the same as the sent data.

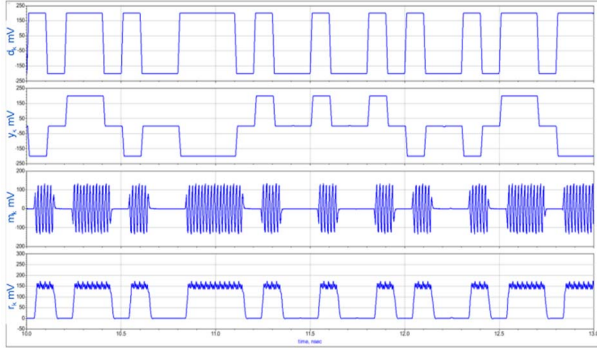


Figure 7. Duo-binary modulation output in time domain.

In Figure 8, the eye diagram of the system before and after the channel transmission can be seen. The simulated SNR is 23.9 dB, which leads to a BER that is lower than  $10^{-15}$ .

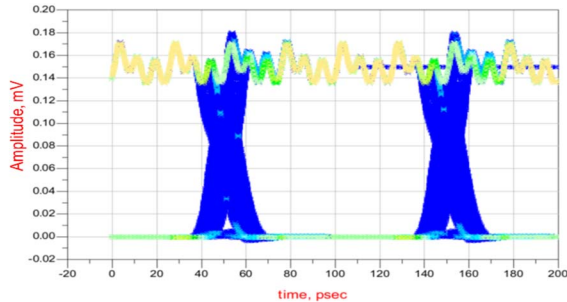


Figure 8. Duo-binary modulation output eye diagram.

#### V. CONCLUSION

A 10-Gbps length adaptive serial link was proposed in this paper. A modulated RF carrier was used to reduce the propagation delay and simplify the link design. Differential transmission lines were used to limit cross-talk effects. To increase the spectral efficiency of the link and relax the RF design constraints, duo-binary modulation was also implemented. This modulation has the same spectral efficiency as PAM-4 without the need for three comparators. Indeed, the use of a self-mixing process in reception combined with a differential pre-encoding leads to only two states, thus only one comparator was required. The simulation showed that the system exhibits a low BER without code correction

nor equalization. A prototype is under development in ST 28-nm FDSOI technology.

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