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Abstract

Unlike SiC unipolar devices, the on-state resistance of diamond unipolar devices based on bulk conduction has a negative temperature coefficient (NTC) which reduces the conduction losses at high junction temperatures. Thus, in order to associate these opposed temperature coefficients, the current article focuses on the modeling of an hybrid power device composed of a n-type 4H-SiC MOSFET and a p-type diamond bulk FET device. The optimal performances and sizing of SiC and diamond devices are introduced and calculated, as an initial benchmark under the same specifications. Based on an analytical modeling of both switching and conduction losses, junction temperatures and associated heatsink paremeters, the hybrid device performances are evaluated for a synchronous buck converter operating at 1200V - 1A and at an ambient temperature of 300K. The results described in the manuscript highlight an equilibrium of the hybrid device total losses over a large range of temperatures as well as a reduction by two of the SiC active area. The proposed analysis could be further extended to different voltage/current classes to meet the requirements of alternative applications.

Keywords: Diamond, SiC, Hybrid devices, Benchmark, Analytic modeling

1. Introduction

Thanks to its outstanding thermal and electrical properties, diamond is expected to improve significantly the performance of the next generation of power semiconductor devices, as presented in [1, 2, 3]. Numerous devices have been already presented in the literature, from diamond Schottky diodes to vertical Field Effect Transistors [4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18]. Diamond thermal substrate can also be used solely for its highest thermal conductivity such as in [19]. In the context of power electronics, the key benefit of diamond semiconductor devices is to reach the highest critical electric field in OFF-state, further allowing a reduction of the drift region thickness and an increase of its doping level [20]. This leads to a smaller specific ON-state resistance comparatively to other wide bandgap materials or Silicon, for the same breakdown voltage. Current diamond power devices are either based on bulk or surface conduction [1, 3]. For bulk conduction, unipolar devices based on Boron doping offer high free hole mobilities and a wide doping range (from $1{\cdot}10^{15}\mathrm{cm}^{-3}$ [21] to more than $1{\cdot}10^{21}\mathrm{cm}^{-3}$ [22]). This doping control and bulk conduction allow a controlled device optimization, a better reliability and replicability of the fabrication process. However, the diamond devices based on bulk conduction suffer from incomplete ionization, which increases the ON-state resistance at room temperature and below [23, 24]. At high junction temperatures (e.g. higher than 400K),

such devices exhibit a high free hole concentration thanks to better dopant ionization, which, combine to the high free carrier mobility, makes these devices attractive in the context of power electronics [25].

As previously done in [26, 27, 28] between SiC MOSFET and Si IGBT, the first objective of this article is to benchmark SiC with diamond devices operating under the same specifications in a simple converter system. Considering the current state of maturity with diamond power devices, a short-term target of 1A ON-state and 1700V OFF-state is assessed in this article. However, the study can be easily extended to other voltage/current classes in accordance with the targeted application. The benefits of diamond power devices are clearly assessed, while highlighting the reduced total losses, smaller active area and a smaller heatsink. Hence, diamond devices have the highest impact, especially at junction temperature above 400K. However, to reduce the required active area and to maintain the high benefits of diamond devices, we suggest a hybrid solution combining SiC and diamond in parallel, similarly to other hybrid associations with different materials and power device technologies [29, 30, 31, 32, 33, 34, 35]. Additionally, the hybrid SiC/diamond switch combines the low resistance of SiC at low temperature and the low resistance of diamond at high temperature, while reducing the required area of both devices. Finally, an electro-thermal simulation of the SiC/diamond hybrid switch is presented.

2. Benchmark Full-SiC vs. Full-Diamond

2.1. Assumptions and approach

To investigate the capabilities of a hybrid converter, it is first interesting to compare the performance of a full-SiC and a full-Diamond architecture. Therefore, a classical synchronous buck converter (half-bridge) is considered, as shown in figure 1, designed to operate at 1200V - 1A with a 50 kHz switching frequency, a 50% duty cycle and an ambient temperature of 300 K. The schematic is here detailed for a PMOS device as a controlled switch. It is important to note that this reduced operating current meets the defined requirements of a current research project for the development of p-type diamond devices [36]. The results presented here can be easily extrapolated to address higher power levels, and the approach is not specific to these converter specifications. Moreover, for the sake of this study, the selected components, SiC and diamond, will ensure a 1700V breakdown voltage to guarantee a safe operation with a converter input voltage of 1200V. To achieve the best performances and related to the free carrier mobilities and doping limitations, the SiC devices will

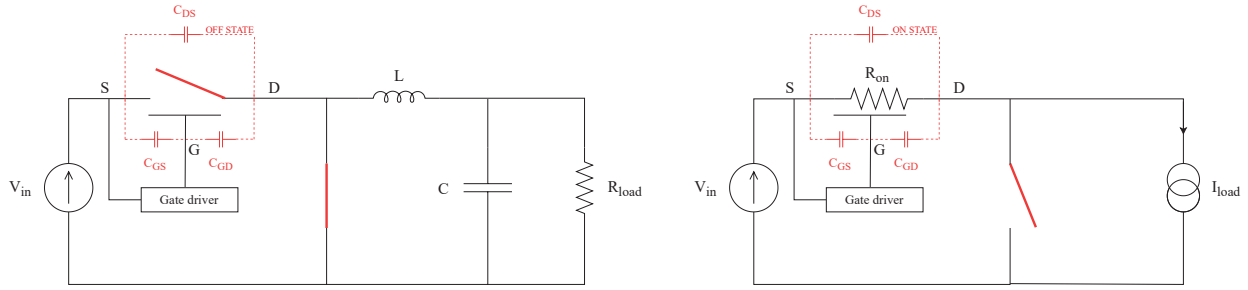


Figure 1: Electrical schematic of a synchronous DC/DC power buck converter in discharge (left side) and charge (right side) configuration. The converter is designed using a PMOS device as a controlled switch. The schematic implements an equivalent scheme for the transistor including the parasitic capacitances and the on-state resistance.

be based on a n-type drift region, whereas the diamond ones will consider p-type. Finally, based on the chosen breakdown voltage and switching frequency, only unipolar type of devices and current conduction based on majority carriers will be considered.

The converter performance is evaluated regarding the prediction of conduction and switching losses, as defined by equation (1), where only the transistor losses are considered. To that end, the two transistor states must be considered, the OFF-state (see the left schematic in figure 1) and the ON-state (see the right schematic in figure 1). In OFF-state, as the current is flowing through the second switch, no conduction losses are dissipated by the transistor. On the contrary, during the transistor ON-state, conduction losses appeared due to the device resistance (called the on-state resistance) between the drain and the source. In this state, the converter schematic is simplified by replacing the second order passive filter and resistive load by a constant current source. Furthermore, parasitic capacitances between each device terminals can be observed which induces switching losses due to the commutation time between two states (ON/OFF or OFF/ON). The calculations of both losses type are based on several assumptions which are key parameters to design and size the power devices: the device is of vertical type, and the conduction losses are only due to the drift region [25]; the drift region is considered in Non-Punch Through (NPT) configuration, which maximizes the doping density of the drift layer and reduces the device on-state resistance [20]; the turn off losses are neglected, which limits the switching losses to the stored electric charge in the output capacitance during the switching transition [3]. One should note that the NPT configuration has been chosen as a first order design but does not reflect an optimal design for both diamond [20] and SiC devices [37, 38]. The current work can further be extended to an optimal punch-trough (PT) design for both materials improving the BV vs R_{on} figure-of-merit.

$$P_{loss} = P_{cond} + P_{switch} \tag{1}$$

As a consequence, the conduction and switching losses equations for the controlled switch are respectively expressed in equations (2) and (3).

$$P_{cond} = \alpha \cdot R_{on} \cdot I_{load}^2 \tag{2}$$

$$P_{switch} = P_{on} = \frac{2}{3} \cdot C_{T(BV)} \cdot \sqrt{BV} \cdot V^{\frac{3}{2}} \cdot f \tag{3}$$

where α is the duty cycle, R_{on} is the device on-state resistance, I_{load} is the operating current (assumed constant), f is the switching frequency, $C_{T(BV)}$ is the transition capacitance, BV is the device breakdown voltage and V is the switched voltage. Assuming that the output capacitance is equal to the transition capacitance, this one is calculated, at BV and in NPT condition, by equation (4) with $\epsilon_0 \cdot \epsilon_r$ the device permittivity, S the active area and L_{drift} the thickness of the drift region [3]. This switching loss model is assumed to be independent with temperature, which was previously verified with parasitic capacitors mostly independent of temperature [39, 40]. Moreover, the switching losses based on this model represent a minimal value which can be obtained with ultra-fast gate driving leading to extremely fast di/dt sequence. As a consequence, only the dv/dt part is generating switching losses and taken into account in this model. Hence, the switching losses are independent on the switched power current (I_{load}), and only depend on the converter input voltage, the switching frequency, and the device parasitic capacitance as presented in

equations (3) and (4). Knowing the device architecture and the gate charge waveforms, which is not the case for diamond based devices, the model could be further improved to account for both the turn-off loss and the load current dependence on the switching loss, as proposed in [41].

$$C_{T(BV)} = \epsilon_0 \cdot \epsilon_r \cdot \frac{S}{L_{drift}} \tag{4}$$

As mentioned earlier, the doping level and the thickness of the drift layer were calculated in NPT configuration by solving the 1D ionization integral [42] with the coefficients from [43] for SiC device and from [44] for diamond one. The results are reported in table 1 for a 1700 V breakdown voltage together with the corresponding critical electric field, E_{crit}. Due to the lack of clear physical parameters in the avalanche regime for diamond [45], the impact ionization coefficients are supposedly independent of the temperature. Hence, the breakdown voltage is assumed to be independent of the temperature.

Material	L_{drift} [μm]	$N_{d/a,drift}$ [cm^{-3}]	E_{crit} [MV/cm]
4H-SiC	14.5	9.1 x 10^{15}	2.39
Diamond	4.38	5.6 x 10^{16}	7.77

Table 1: Key parameters of the SiC N-type and the diamond P-type drift region for a 1700 V breakdown voltage in NPT condition.

For the following studies, it will be assumed that the thermal behavior of the system is fully managed and that the junction temperature is controlled making it an input parameter for simulations.

2.2. Full-SiC

2.2.1. Analytic modeling

For predicting the conduction losses, it is required to calculate the device specific on-state resistance, which is linked to the device active area, S, and the on-state resistance, R_{on}. In the case of a 4H-SiC material, due to the low-doping value of the drift region, the incomplete ionization effect is neglected [46] leading to the equation (5) for the specific on-state resistance.

$$R_{on,s} = R_{on} \cdot S = \frac{L_{drift}}{q \cdot \mu_n(T) \cdot N_{d,drift}} \tag{5}$$

where q is the electron charge, $\mu_n(T)$ is the temperature-dependent electron mobility and $N_{d,drift}$ is the donor impurity concentration of the drift layer from table 1. The electron mobility is derived from the empirical model reported in [47] for a 4H-SiC device. The corresponding expression is detailed hereafter.

$$\mu_n(T) = \frac{\mu_0}{\left(1 + \left(\frac{\mu_0 \cdot E}{v_{sat}}\right)^{\beta}\right)^{\frac{1}{\beta}}} \tag{6}$$

where μ_0 is the electron mobility at low electric field, E is the electric field, v_{sat} is the saturation velocity and β is a constant related to v_{sat}. The equation (5) is clearly an underestimate of the actual value, since the bulk mobility is assumed. Indeed, it is known that in SiC MOSFET power devices, one should also consider the substrate, the JFET and the accumulation resistance as well as the channel resistance resulting from

a reduced channel mobility, especially in the 600V-3300V voltage range, which increases the total on-state resistance. As a reminder, this simplified model only considers the bulk mobility in the drift region.

2.2.2. Simulations results

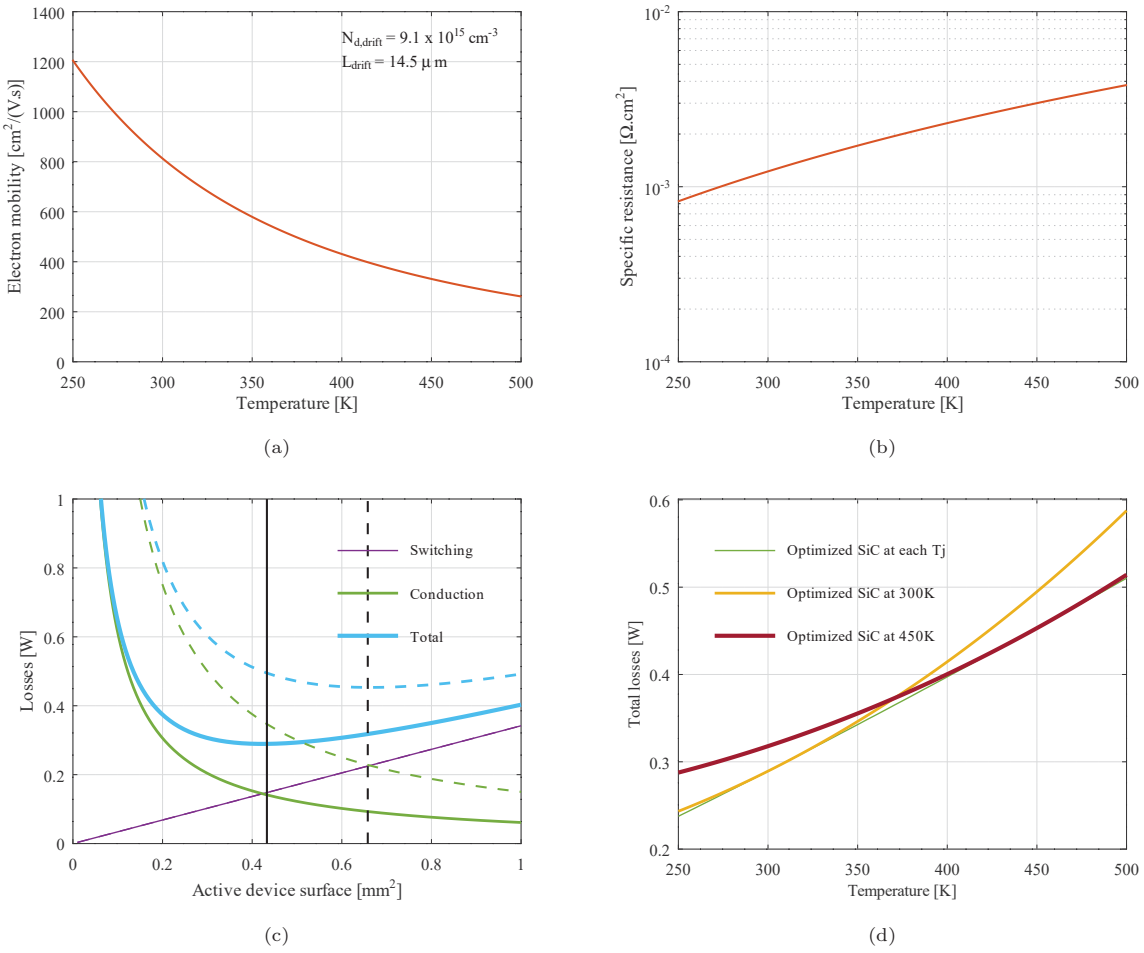


Figure 2: (a) Electron mobility and (b) Specific on-sate resistance according to the temperature, (c) Detailed losses according to the device surface for T=300K (solid lines) and T=450K (dashed lines) and (d) Total losses according to the temperature for various optimization conditions of a n-type 4H-SiC device for BV=1700V. For all simulations, the electric field was fixed to E=1000V/cm.

Based on the analytic model proposed in the previous section, simulations were performed for a 4H-SiC device featuring a 1700V breakdown voltage and the parameters shown in table 1 for the drift region. The results are reported in figure 2a for the electron mobility where a negative temperature-dependence is observed due to the negative temperature coefficient of all scattering mechanisms (phonons and impurities) [25]. This causes the mobility of the studied device to decrease from 1200cm^2/(V.s) at 250K down to 250cm^2/(V.s) at 500K. Figure 2b presents the simulation results for the specific on-state resistance where a positive temperature-dependence is highlighted. The device $R_{on,s}$ expands from 0.8mΩ.cm^2 at 250K to 4 Ω.cm^2 at 500K, thereby increasing the conduction losses, and thus the total losses of the device, with the temperature. This feature is shown in figure 2c where the conduction, the switching and the total losses

are observed at 300K (solid lines) and at 450K (dashed lines) for a wide range of device surface. From this figure, it can be noticed that the device losses are increased with increasing temperature regardless of the device area. Moreover, an extremum can be extracted for the device surface allowing to minimize the total losses at a given junction temperature, as represented by the vertical lines. This optimal area is the best trade-off between conduction losses and switching losses. Based on this figure, the optimal device areas were extracted for several conditions : (i) at T_j=300K, (ii) at T_j=450K and (iii) at each junction temperatures ranging from 250K to 500K. From these extraction results, the total losses evolution according to the temperature is plotted in figure 2d for the corresponding sized devices. This particular graph indicates that the minimum losses over the temperature range are obtained when the device surface is optimized at each device temperature. On the contrary, the optimization at a given temperature of 300K or 450K only allows to minimize the losses around this specific point while a maximum 20% increase of the total losses is observed beyond. Nonetheless, as an elevation of the device junction temperature (relative to room temperature) due to self-heating is expected, one can size the device area at a 450K temperature to guarantee its efficiency at nominal operating conditions.

2.3. Full-Diamond

2.3.1. Analytical modeling

Diamond, in contrast to 4H-SiC, suffers from incomplete ionization due to a high activation energy of the dopants [23], in the context of bulk conduction. Therefore, it is necessary to calculate the hole concentration as a function of the temperature, the compensation level and the p-type doping density. A formulation has been proposed in [48] based on the neutrality equation which is reported in equation (7).

$$p(T) = \frac{1}{2}(\phi_a(T) + N_d)\left(\left(1 + \frac{4 \cdot \phi_a(T) \cdot (N_a - N_d)}{(\phi_a(T) + N_d)^2}\right)^{1/2} - 1\right) \tag{7}$$

where

$$\phi_a = 0.25 \cdot N_v(T) \cdot T^{1.5} \cdot e^{\frac{E_A}{k_B T}} \tag{8}$$

with N_v the effective densities of state and E_a the thermal activation of the boron acceptor calculated as in [49]. Furthermore, to properly calculate the conduction losses of p-type diamond devices, an empirical model for the hole mobility is used based on the formulation from [50]. This model takes into account the temperature dependence and the impurity density ($N_{imp} = N_d + N_a$) dependence of the mobility. The corresponding formulation is reported below with $\mu(300, N_{imp})$ the mobility at T = 300 K and $\beta(N_{imp})$ the temperature dependence exponent.

$$\mu(T) = \mu(300, N_{imp}) \cdot \frac{T}{300}^{-\beta(N_{imp})} \tag{9}$$

Consequently, the specific on-sate resistance for diamond devices is calculated using the formulation reported hereafter where both the mobility and the hole concentration are temperature-dependent.

$$R_{on,s} = R_{on} \cdot S = \frac{L_{drift}}{q \cdot \mu_p(T) \cdot p(T)} \tag{10}$$

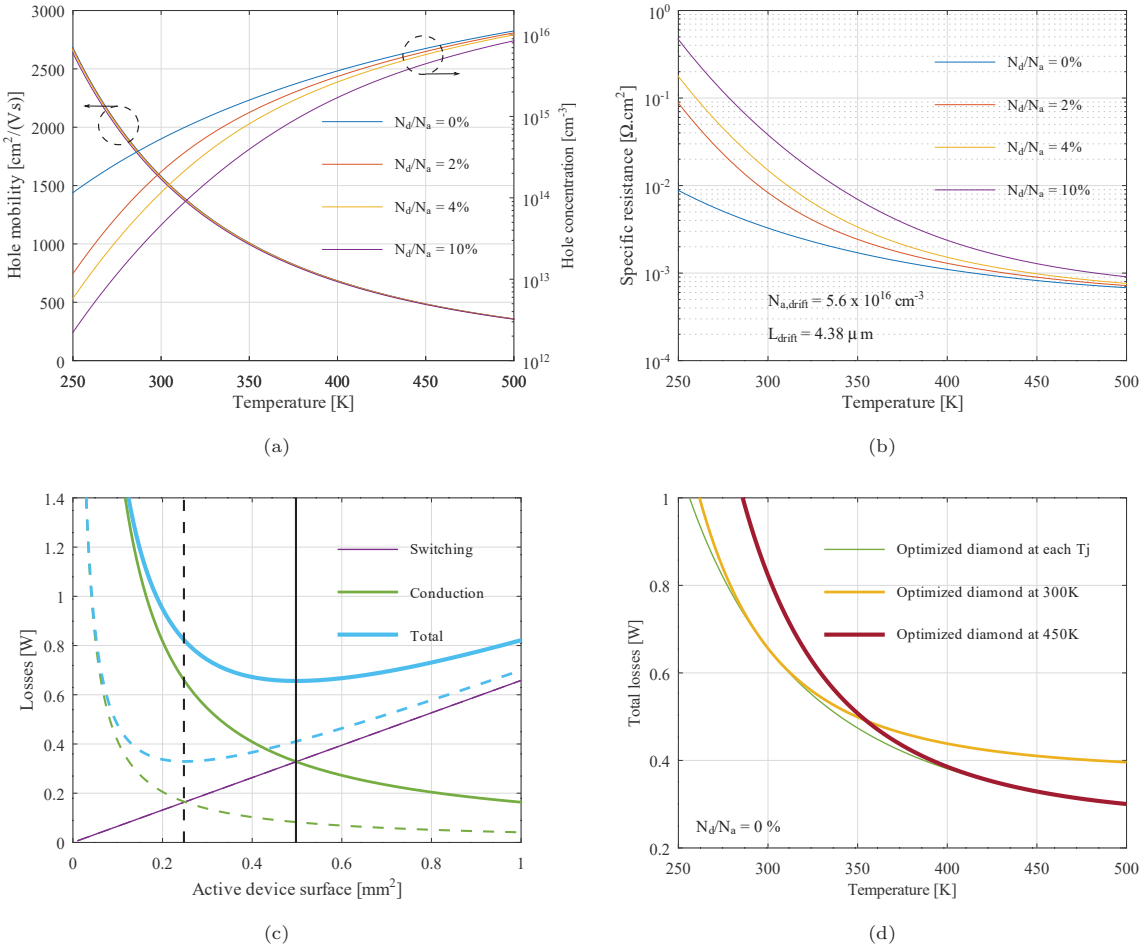


Figure 3: (a) Hole mobility and Hole concentration, (b) Specific on-state resistance, (c) Detailed losses according to the device surface for T=300K (solid lines) and T=450K (dashed lines) and (d) Total losses according to the temperature for various optimization conditions of a p-type diamond device for BV=1700V. Different densities of impurities are investigated N_d/N_a=[0;2;4;10]% for the first two figures while it has been fixed to N_d/N_a=0% for the last two figures.

2.3.2. Simulations results

The corresponding simulation results are reported in figures 3a and 3b with the hole mobility, the hole concentration and the specific on-state resistance evolution according to the temperature. Different densities of donor impurities are investigated ranging from 0 to 10% of the acceptor doping level which corresponds to common reported values [51]. Concerning the hole mobility, in figure 3a, a negative temperature-dependence is observed for diamond devices similarly to 4H-SiC. This causes the mobility to decrease from 2600cm^2/(V.s) at T=250K down to 400cm^2/(V.s) at T=500K. It is interesting to note that regardless of the donor impurities density, the hole mobility is not impacted, especially at temperatures beyond 400K. On its side, due to the incomplete ionization of dopants, part of the carriers is trapped by donor atoms [25] which considerably reduces the hole concentration, specifically at temperatures below 400K as observed in figure 3a. For example, at room temperature, the hole concentration without compensation is equal to $p(300K)_{0\%}$=1x10^{14}cm^{-3}, corresponding to an ionization ratio of 0.17%, while with a 10% compensation ratio, the hole concentration

drops by more than one order of magnitude to $p(300K)_{10\%}$=2x$10^{12}cm^{-3}$, leading to an ionization ratio of 0.004%. At higher temperatures, beyond 400K, the compensation effect tends to be reduced leading to an increase of the hole concentration and of the ionization ratio. The consequences of this particular behavior induced by the incomplete ionization of dopants can also be observed on the specific on-state resistance (from figure 3b) which presents a negative temperature coefficient meaning that the conduction losses will be lower at high temperatures. Indeed, without compensation, the specific resistance decreases from $R_{on,s}$=0.01Ω.cm^2 at 250K to $R_{on,s}$=0.8mΩ.cm^2 at 500K. In accordance with the hole concentration evolution, the specific resistance is increased with increasing compensation, especially at temperatures below 400K. For the rest of the study, the ideal scenario without compensation is preferred for the modeling of p-type diamond device. Consequently, the simulation results from figure 3c and 3d are obtained in this particular case. As done in section 2.2.2 for a SiC architecture, figure 3c presents the conduction, the switching and the total losses at 300K (solid lines) and at 450K (dashed lines) for a wide range of diamond active area. Contrary to the SiC device, it can be observed a large decrease of the total losses at high junction temperature, regardless of the active area, due the reduction of the specific resistance. Moreover, a reduction by two of the optimal area is highlighted at T=450K compared to T=300K which consequently minimize the required chip size. Finally, figure 3d represents the total losses evolution according to the temperature for various optimization conditions, similarly to the study performed in section 2.2.2 for 4H-SiC device. It can be noticed from this plot that the minimum total losses are reached at high device temperature, which is consistent with the evolution of the specific on-state resistance. Consequently, the total losses are two times lower at 500K than at 250K, demonstrating the benefit of using diamond devices at high junction temperatures.

2.4. Comparison

Prior to suggest an hybrid device between a n-type SiC and p-type diamond MOSFET, it is interesting to compare their performances and characteristics. To that end, figure 4a presents the specific on-state resistance evolution according to the temperature for both materials. From this plot, it is noticeable that the use of diamond devices for temperatures below 350K is not relevant as the specific on-state resistance is higher than for SiC devices. Nevertheless, beyond this device temperature of 350K, the trend is reversing and the specific-on state resistance becomes lower for diamond than for SiC component. Figures 4b and 4c present the calculated optimal device areas and minimum losses for SiC and diamond component according to the device temperature. One can observe that, regardless of the temperature, the diamond surface is smaller than the SiC one and the gap between those areas tends to grow with temperature. Moreover, a similar trend can be noticed on the graph from figure 4c with a drastic decrease of the total losses using diamond devices at a device temperature of 450K or 500K. This is mainly due to the negative temperature coefficient of the diamond, contrary to the 4H-SiC, which reduces the conduction losses. Finally, the last aspect to investigate is the heatsink volume required for the investigated application. Since the device junction temperature is here considered as an input parameter, the thermal resistance can be scaled to increase the junction temperature (in the case of diamond device) and consequently reduce the losses. The thermal resistance is calculated according to the equation below [52].

$$R_{th} = \frac{T_j - T_{amb}}{P_{loss}} \tag{11}$$

Regarding this relation, it is only considered a single thermal resistance reflecting the heat exchange

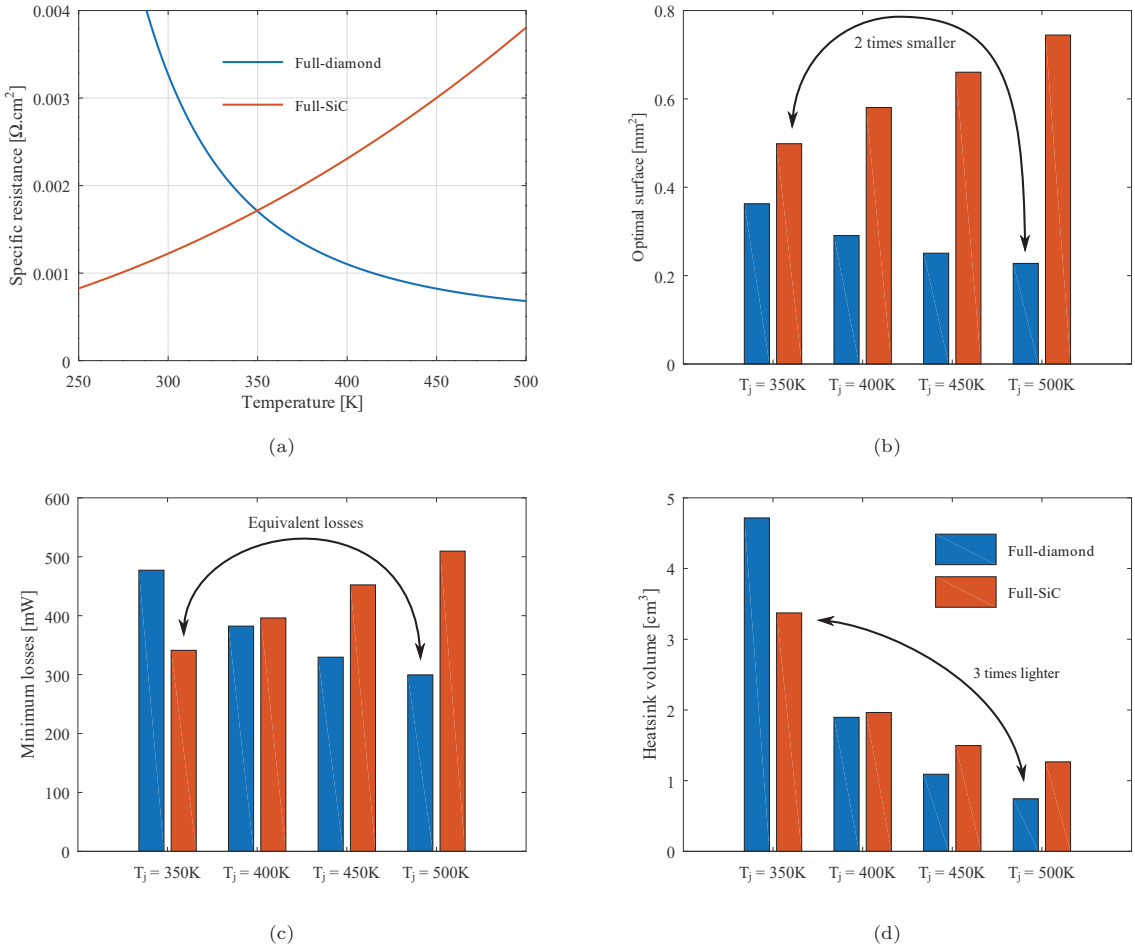


Figure 4: (a) Specific on-state resistance, (b) Optimal surface, (c) Total losses and (d) Heatsink volume according to the temperature for a n-type SiC and a p-type diamond device for BV = 1700 V.

between the device junction temperature and the ambient temperature. Therefore, it is assumed ideals thermal contacts between the semiconductor device and the cooling system. For the calculation of the heatsink volume, is has been considered natural convection with a volumetric resistance of 500 $cm^3.K.W^{-1}$ [3] leading to the following expression :

$$V = \frac{500}{R_{th}} \tag{12}$$

The simulation results are displayed in figure 4d where it is observed a reduction of the heatsink volume using diamond device for temperatures beyond 400 K. At 500 K, the heatsink volume is two times bigger using SiC device than diamond one. The benefits of diamond devices at high junction temperatures can be directly observed from the highlighted points in figure 4b, 4c and 4d which compare the performances of SiC device at 350K and diamond one at 500K : a reduction by two of the device active area and by three of the heatsink volume is achieved for diamond based device compared to SiC device while the minimal losses are mostly equivalent for both materials.

2.5. Preliminary discussion

Although the expected performances of diamond power devices are clear, as highlighted herein before, the benefits are not as high as one could imagine: even though the required chip area of diamond is reduced by a factor of two and the heatsink volume by three for the same total losses comparatively to SiC, this comparison under estimates the benefits of diamond devices. Several key elements can be mentioned to explain these results:

- The switching loss model of equation (3) is the lowest possible energy loss during the turn on transition. In this model, the parasitic capacitor has a key role and its dependence on the drift region thickness was presented on equation (4). Due to the reduced drift region thickness of diamond comparatively to 4H-SiC (almost three time thinner) and the dielectric permittivity almost two time smaller with diamond, the turn on energy loss is approximately 150% bigger with diamond than 4H-SiC, for the same active area. In the reality, the parasitic capacitors are not only due to the space charge region extension in the drift region, but also to the device architecture (e.g. lateral vs. vertical, additional drain to source parasitic capacitors due to layout and interconnect). As a result, the predicted higher switching losses with diamond than 4H-SiC for the same device area is definitely a worst case scenario. Nonetheless, this model is fair and represents the lowest possible value.

- The switching loss model does not take into account the energy loss during the di/dt phase of the turn ON sequence. Hence, the switching losses model of equation (3) does not consider the switched current and the associated switching losses. Thanks to the reduced area with diamond devices and the consequent reduction of parasitic input capacitance, a reduction of switching losses will be achieved during the di/dt phase with diamond devices. This is not predicted by the current model, which would reduce the switching losses of diamond devices comparatively to 4H SiC.

- The conduction losses in the conduction channel are not considered. In the context of 4H-SiC, the low electron mobility in the inversion channel and its associated significant resistance cannot be neglected relatively to the drift region resistance. Consequently, the conduction losses predicted by equations (2) and (5) underestimate the total conduction losses of 4H SiC. In diamond MOSFET based on Boron doping and the deep depletion, the bulk hole mobility is achieved in the channel region which maintains the channel resistance to an order of magnitude below the drift region.

- Consequently to this analysis, the expected performances of actual diamond power devices are surely underestimated. Nonetheless, this quantitative comparison based on clear assumptions is the foundation of first benchmark and a more complex association as presented hereinafter.

Following this discussion and based on the results presented in figure 4a, a hybrid association will be introduced in the following section. It will combine the low specific on state resistance of 4H-SiC at junction temperatures below 350K and the best performances of diamond at junction temperatures above 400K.

3. Hybrid SiC-D power modules

3.1. Assumptions and approach

Based on the modeling presented in section 2 for SiC and diamond devices, the current part gets interest in the design of an hybrid power device as presented in figure 5a, which consists of a n-type SiC device (with

a corresponding area S_{SiC}) and a p-type diamond device (with a corresponding area $S_{diamond}$). As this new architecture can imply a non-symmetric current distribution between the devices, a new formulation for the conduction losses is required depending on the current flowing through each device (see equation (13)). Conversely, the switching losses are estimated from equation (14) which lead to a constant contribution since the commutation losses are independent of the load current. The total losses of the hybrid device are obtained from the combination between the switching and the conduction losses.

$$P_{cond} = \alpha \cdot (R_{on,SiC} \cdot I_{SiC}^2 + R_{on,diamond} \cdot I_{diamond}^2) \tag{13}$$

$$P_{switch} = \frac{2}{3} \cdot \sqrt{BV} \cdot V^{\frac{3}{2}} \cdot f \cdot (C_{T(BV)_{SiC}} + C_{T(BV)_{diamond}}) \tag{14}$$

where I_{SiC}, respectively $I_{diamond}$, is the current flowing through the SiC, resp. diamond, device. Those currents are computed according to the equations reported hereafter which depends on the devices on-state resistance, and consequently, of the devices active areas. The aim here is then to establish hypotheses to determine those areas in order to properly combine the advantages of SiC device at junction temperatures below 350K and of diamond device at junction temperatures above 400K.

$$I_{diamond} = \frac{R_{on,SiC}}{R_{on,SiC} + R_{on,diamond}} \cdot I_{load} \tag{15}$$

$$I_{SiC} = \frac{R_{on,diamond}}{R_{on,SiC} + R_{on,diamond}} \cdot I_{load} \tag{16}$$

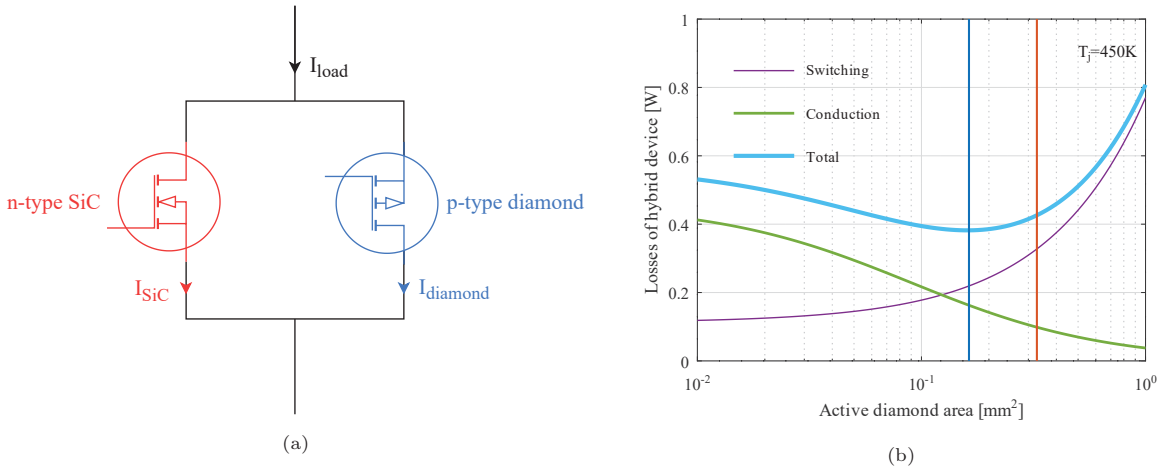


Figure 5: (a) Schematic of an hybrid SiC-D device and (b) Optimization simulation results of the diamond active area within the hybrid architecture in order to minimize the losses at T_j=450K.

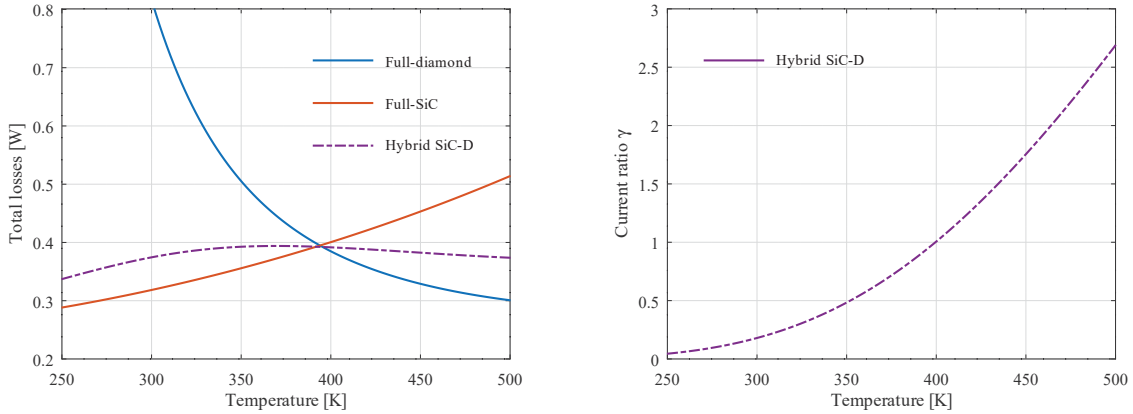
In this study, at the nominal operating point, the junction temperature for both devices is set commonly to a value of T_j=450K. According to the figure 4b, the SiC active device area is fixed at half of the optimal area for a full-SiC architecture at that same temperature, i.e. S_{SiC}=0.33 mm^2. Keeping this information in mind, the diamond device area is optimized to minimize the total losses of the hybrid device at T_j=450K. The approach is illustrated in figure 5b where the SiC surface has been fixed according to the previous hypothesis,

as represented by the vertical red line. Then, the losses (total, conduction and switching ones) of the hybrid device are plotted according to the diamond surface at T_j=450K. From this plot, an extremum can be extracted corresponding to the minimum total losses of the hybrid device leading to an optimal diamond area of $S_{diamond}$=0.16mm^2, represented by the vertical blue line. It is noticeable that the diamond active area is twice as small as that of SiC device which will improve the thermal management of the commutation cell.

3.2. Benchmark at nominal operating point

Based on the hypotheses presented in the previous section, the areas of both SiC and diamond devices are fixed. Therefore, simulations are performed to estimate the performances of the developed SiC-D hybrid device which is compared to the performances of the full-SiC and full-diamond architecture sized at T_j=450 K. The results are presented in figure 6a for the total losses and in figure 6b for the current ratio, calculated following equation 17, both according to the temperature.

$$\gamma = \frac{I_{diamond}}{I_{SiC}} \tag{17}$$



(a) (b)

Figure 6: (a) Total losses evolution according to the temperature for a full-SiC, full-diamond and hybrid SiC-D architectures and (b) corresponding current ratio according to the temperature for the diamond transistor within the SiC-D hybrid device.

First, it can be observed that the total losses evolution for the hybrid device is close from the full-SiC architecture ones for temperatures below 400K and from the full-diamond architecture ones for temperatures above 400K. Indeed, the current ratio between the diamond current and the SiC current is reversing along the temperature for both devices. For temperatures ranging from 250K to 400K, the major part of the load current flows through the SiC device while the opposite result is observed for temperatures beyond 400K. Therefore, the hybrid device allows to efficiently use the PTC of SiC at moderate temperatures and the NTC of diamond devices at elevated temperatures leading to an equilibrium of the total losses quantity along the temperature. Also, as displayed in table 2, the hybrid device topology results in a reduction of the SiC active area by a factor of two and a reduction of the heatsink volume. Comparatively to a full-diamond architecture, the benefits of the lower on state resistance of diamond at junction temperatures above 400K

are still obtained with the hybrid association, albeit with a required diamond area two times smaller. This last point is particularly interesting due to the limited access to large area diamond wafers and for reducing the manufacturing cost for the hybrid switch compared to a full-diamond solution. The presented simulation results are only valid at nominal operating point, i.e. for a load current of 1A. The next section therefore focuses on the impact of this load current on the performance of the commutation cell.

Material	Full-SiC	Full-diamond	Hybrid device SiC-D
S_{SiC} [mm^2]	0.66		0.33
$S_{diamond}$ [mm^2]		0.25	0.16
Total losses @450K [W]	0.45	0.33	0.38
Heatsink volume @450K [cm^3]	1.5	1.1	1.27

Table 2: Comparative case study between the full-SiC, the full-diamond and the hybrid architecture for the 1700V comparison.

3.3. Impact of load variation

In the previous sections, the junction temperature was considered as an input parameter, responsible for the obtained electrical behavior while it can also be a consequence. Indeed, the variation of the load current impacts the thermal response of the system leading to an electrothermal coupling that need to be accounted during simulations. To that end, the LTSpice electrical simulator is used to relate the electrical behavior to the thermal one. The corresponding simulation is performed using a DC sweep on the load current from 0.1A to 1.5A, as presented in figures 7a and 7b. The simulation model attached to the transistors is quite simple as (i) the switching losses are considered as an offset since there are independent of both temperature and load current and (ii) the conduction losses are simulated according to the device on-state resistance, temperature and associated current. For the calculation of the on-state resistance, power fits are performed on the devices specific on-state resistance as the analytic equations cannot be easily embedded within the simulator. The corresponding fits are only valid for temperatures ranging from 250K to 500K. For the thermal management, the conditions to respect are an ambient temperature of 300K and a junction temperature of 450K for both devices at a load current of 1A, in accordance with the converter specifications. These specifications lead to the calculation of thermal resistances, representative of the heatsink required

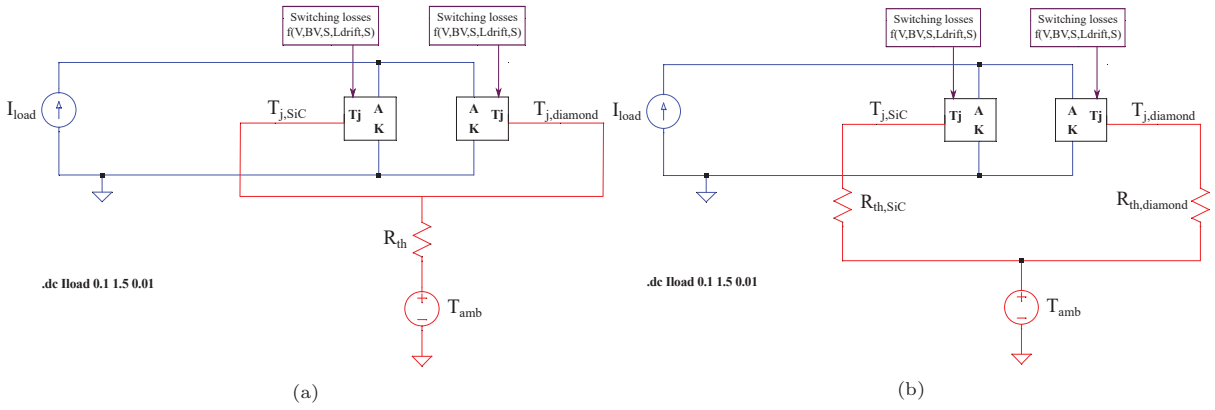


Figure 7: Electrical schematic for a thermal management with (a) a common and (b) an independent junction temperature between both devices. The schematics were simulated on the LTSpice software.

for the application, in order to fix the devices junction temperatures. It results in two possible cases : (i) the junction temperature is common between the SiC device and the diamond one in the hybrid architecture, see figure 7a, which leads to only one thermal resistance for the thermal management or (ii) the junction temperature is independent between both devices, see figure 7b, which leads to two thermal resistances, one for the SiC device and one for the diamond device. Moreover, the calculated thermal resistances based on the previously detailed assumptions are fixed to a constant value regardless of the load current.

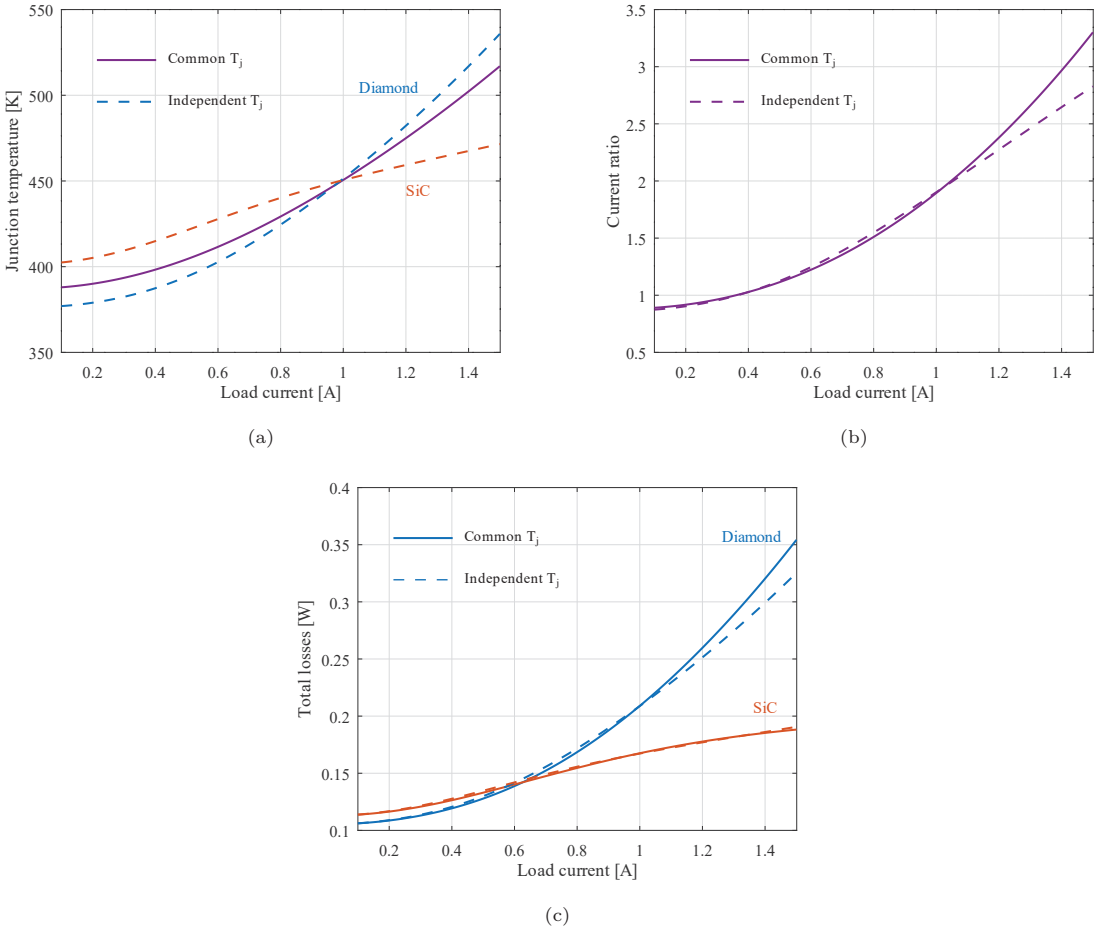


Figure 8: (a) Junction temperature, (b) current ratio and (c) total losses evolution according to the load current for a common (solid lines) and independent (dashed lines) thermal management of the hybrid device.

The simulation results for both scenarios are plotted in figure 8a, 8b and 8c with, respectively, the temperature, the current ratio and the total losses evolution according to the load current. At the nominal operating point of 1A, we retrieve the performances shown in the previous section with a junction temperature of 450K ,a current 1.8 times higher for the diamond device than for the SiC one and total losses of 0.38W. As expected, at light load, the major part of the current is conducted by the SiC device, leading to higher losses and junction temperature compared to the diamond device. On the contrary, at over-current conditions, the current contribution in the diamond device is predominant which, thereby, increases its junction temperature and equivalent losses. Concerning the two thermal managements, minor differences

can be highlighted, especially at over-current conditions. Indeed, above the nominal operating point, the current ratio becomes higher in the case of the common T_j which increases the diamond current contribution within the hybrid device, and, therefore, the device junction temperature for both materials up to 520K at I_{load}=1.5A. On the contrary, for the independent thermal management, the SiC device is not forced to operate at the same junction temperature than diamond which leads to a limited increase of the device temperature up to 470K at I_{load}=1.5A. On its side, the junction temperature of the diamond device is larger in that case, up to 535K at 1.5A, to counteract the limited increase of the SiC temperature and reduce its on-state resistance.

The detailed thermal resistances for both thermal management are reported in table 3 where it can be noticed that the two studied scenarios leads to a similar equivalent volume for the heatsink. The difference remains then in the temperature management of both devices : either the elevation of the junction temperature for the SiC device must be minimized and be maximized for the diamond one, or, both devices are thermally managed together. Nevertheless, the proposed hybrid device does efficiently combine the NTC of diamond and the PTC of SiC devices capable to deliver quasi-constant total losses along the temperature and reduced chip size area and heatsink volume.

Case figure	$R_{th_{SiC}}$ [K/W]	$R_{th_{diamond}}$ [K/W]	$V_{th_{SiC}}$ [cm^3]	$V_{th_{diamond}}$ [cm^3]
Common T_j	400		1.27	
Independent T_j	900	725	0.55	0.69

Table 3: Comparative case study between the common and independent thermal management of the hybrid device detailing the thermal resistance and the equivalent heatsink volume.

4. Discussion

Under clear assumptions, we have presented the possible benefits of diamond versus SiC, and a hybrid parallel assembly. As introduced in section 2.5, the assessment of switching losses is quite challenging due to their dependence on many factors (e.g. parasitics in the driving and power loops, EMI vs. switching losses trade-off, transconductance, parasitic capacitors, ...). The model used for the output capacitor is based on a vertical transition capacitor, whereas more complex 2D modeling is required to benchmark more accurately different devices based on different architectures. As far as the hybrid assembly is concerned, the results are attractive to effectively reduce the required power device areas and total losses, and to combine the positive temperature coefficient of SiC with the negative temperature coefficient of diamond. Nonetheless, the paralleling of a n-type SiC FET and a p-type diamond FET is surely challenging in terms of gate driving and packaging. Moreover, the dynamic driving of both gates is open to investigating, albeit offering new degrees of freedom. Ultimately, experimental studies are necessary to confirm the quantified benchmark of full-SiC vs. full-diamond and the hybrid assembly. The targeted specifications of this study can be seen as a short-term milestone, thanks to large area diamond devices and mono-crystalline substrates.

5. Conclusion

An analytical approach has been presented to benchmark SiC and diamond power devices in a half bridge power converter. The device specification was 1700V for breakdown voltage, assessed by state of

the art impact ionization coefficients, and the converter specification was 1200V input voltage and 1A for output load current. A typical switching frequency of 50 kHz has been set, with a duty of 50% and ambient temperature of 300K. The comparison of full-SiC vs. full-diamond has shown a reduction of the chip area by a factor of two, the heatsink volume by a factor of three and with smaller losses, while comparing SiC at 350K junction temperature with diamond at 500 K. To combine the benefits of SiC at junction temperatures below 350K and the ones of diamond above 350K, while reducing the required device areas for both materials, a hybrid association is introduced and quantitatively analyzed. The optimal sizing of diamond in parallel with SiC shows a reduction by a factor of two for the required SiC area, with an additional diamond area two times smaller than the SiC area. The current sharing and total losses as a function of junction temperature is presented in a steady-state analysis, considering the junction temperature as a design parameter. Additionally, an electro-thermal simulation of the hybrid assembly showed the evolution of junction temperatures and current sharing as a function of output load current, from light load to over-current conditions. The results quantified an efficient combination of SiC and diamond, where SiC conducts most of the output current at light load, and diamond at higher output current with small resistance. The hybrid assembly can be considered as a short-term milestone for diamond power devices.

CRediT authorship contribution statement

Marine Couret - Conceptualization, Methodology, Software, Validation, Formal Analysis, Investigation, Writing - Original Draft **Anne Castelan** - Methodology **Nazareno Donato** - Conceptualization, Methodology, Writing - Review and Editing **Florin Udrea** - Conceptualization, Validation **Julien Pernot** - Methodology **Nicolas Rouger** - Conceptualization, Methodology, Validation, Writing - Review and Editing, Project administration, Funding acquisition

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

The figures raw data presented in this manuscript are available on Zenodo [53].

Acknowledgments

The authors would like to thank Idriss Nachete for its contribution to the modeling of diamond-SiC based hybrid power devices presented in this article. This project has received funding from the Clean Sky 2 Joint Undertaking (JU) under grant agreement No 101007868. The JU receives support from the European Union's Horizon 2020 research and innovation program and the Clean Sky 2 JU members other than the Union.

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