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Dopant activity for highly in-situ doped polycrystalline silicon: hall, XRD, scanning capacitance microscopy (SCM) and scanning spreading resistance microscopy (SSRM)

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Keywords: dopant activation, afm, scm, sssr, polysilicon, passivating contact

Abstract

Progressing miniaturization and the development of semiconductor integrated devices ask for advanced characterizations of the different device components with ever-increasing accuracy. Particularly in highly doped layers, a fine control of local conduction is essential to minimize access resistances and optimize integrated devices. For this, electrical Atomic Force Microscopy (AFM) are useful tools to examine the local properties at nanometric scale, for the fundamental understanding of the layer conductivity, process optimization during the device fabrication and reliability issues. By using Scanning Capacitance Microscopy (SCM) and Scanning Spreading Resistance Microscopy (SSRM), we investigate a highly *in situ* doped polycrystalline silicon layer, a material where the electrical transport properties are well known. This film is deposited on a oxide layer as a passivating contact. The study of the nano-MIS (SCM) and nano-Schottky (SSRM) contacts allows to determine the distribution and homogeneity of the carrier concentration (active dopants), especially by investigating the redistribution of the dopants after an annealing step used for their activation. While the chemical analysis by Secondary Ions Mass Spectroscopy (SIMS) quantifies only the dopant concentration in the polycrystalline layer, the comparison with macroscopic characterization techniques as Hall effect measurements, supported with XRD characterization, shows that careful SCM and SSRM measurements can be used to highlight the dopant activation. This analysis gives a complete investigation of the local electrical properties of the passivating contact when the parameters (applied voltages and applied forces) of the AFM nano-contacts are correctly controlled.

1. Introduction

Scanning Probe Microscopies (SPM) are powerful tools in the field of material characterizations at the nanoscale [1, 2]. Since its invention, over 30 years ago, several electrical modes have been developed and optimized based on Atomic Force Microscopy (AFM) [3–5]. For microelectronic characterization at the wafer level, both Scanning Capacitance Microscopy (SCM) [6–8] and Scanning Spreading Resistance Microscopy (SSRM) [9, 10] modes have been implemented to map carrier concentrations of semiconductors with high spatial resolution [5, 9, 11]. These two electrical modes are contact modes, where conductive tips interact with the sample to probe the local electrical properties [12, 13]. Figure 1 presents the Scanning Electron Microscopy (SEM) views of the used probes. The size of the contact depends directly on the tip apex and the surface roughness of the analyzed sample. The SCM probe (figure 1(a)) is a silicon probe fabricated for contact the analyzed surface (with this cantilever a relative low force is applied). The diamond coating of the SSRM probe (figure 1(b)) allows to increase the tip conductivity and the spring-constant of the cantilever, in order to indent the surface and create the electrical path through the sample.

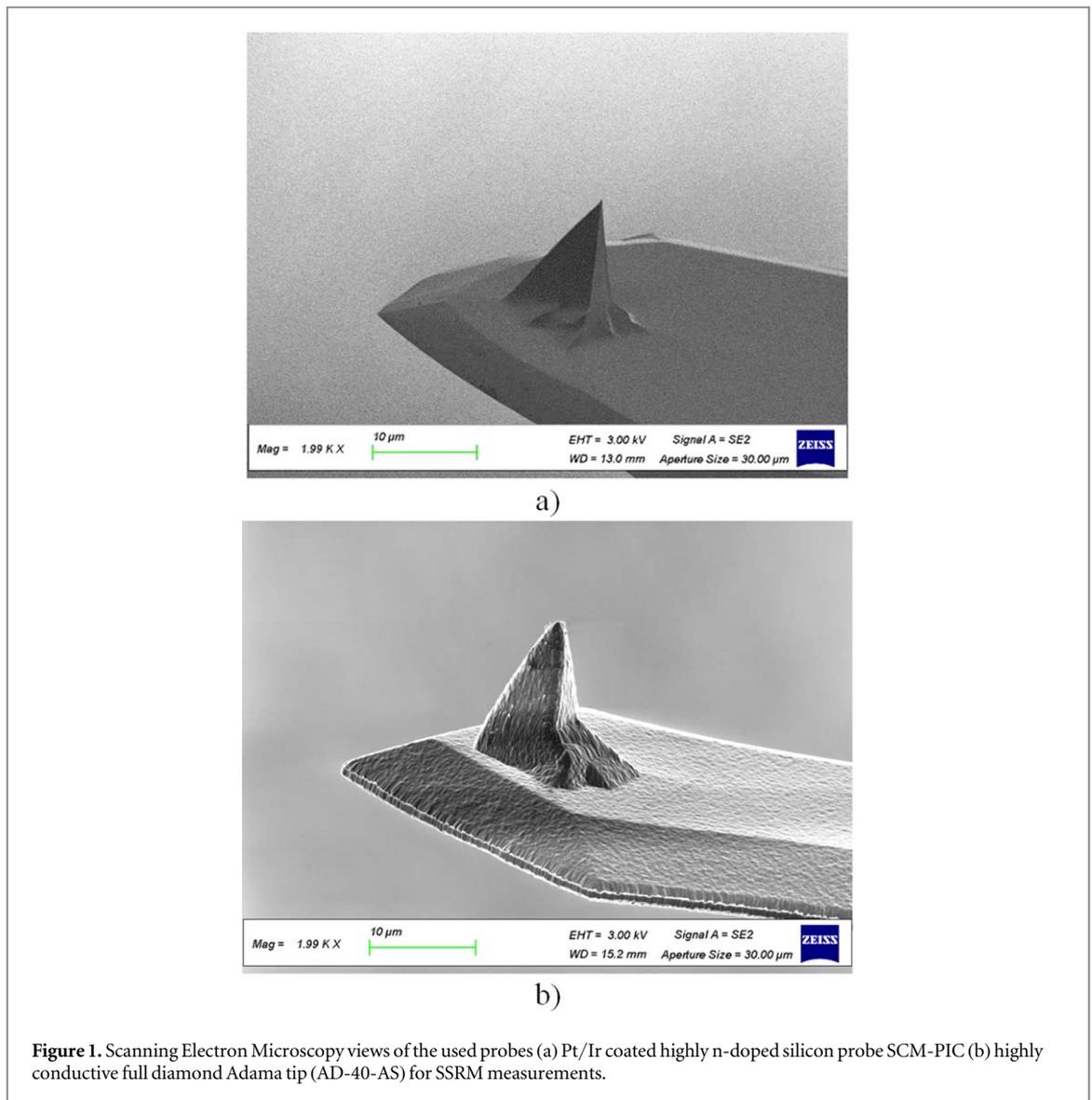


Figure 1. Scanning Electron Microscopy views of the used probes (a) Pt/Ir coated highly n-doped silicon probe SCM-PIC (b) highly conductive full diamond Adama tip (AD-40-AS) for SSRM measurements.

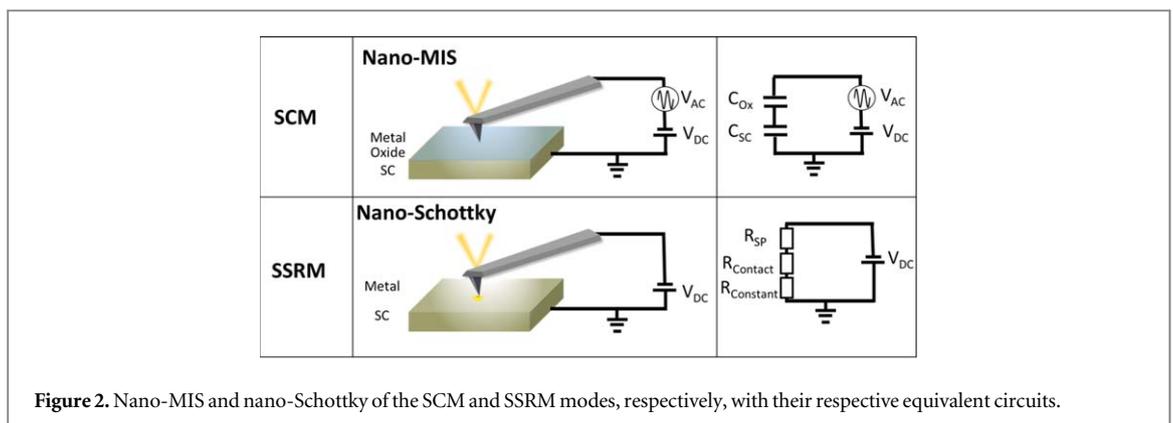


Figure 2. Nano-MIS and nano-Schottky of the SCM and SSRM modes, respectively, with their respective equivalent circuits.

Using SCM, the nano-contact between the conductive tip and the sample provides a nanometer-sized Metal-Insulator-Semiconductor (MIS) capacitor structure [14–16] (figure 2). Here, the metallic electrode is the tip, the semiconducting electrode is the sample, and the necessary insulator is a thin oxide layer being created on the sample surface by a controlled thermal oxidation step. The capacitance of the nano-MIS is controlled by an applied DC voltage bias (V_{DC}) on the sample, while the tip is grounded. In addition, a low frequency (around 100 kHz) AC voltage (V_{AC}) generates the capacitance variation of the free carriers of the sample under the local contact. This local capacitance-voltage variation ($\partial C / \partial V$) is recorded while the tip scans the surface of the

sample, under different V_{DC} , allowing to identify the working regime (depletion, accumulation) of the nano-MIS and therefore the locally present active dopant type and concentration. Thus SCM provides 2D maps of local dopant activities.

For SSRM measurements, the conductive AFM tip is in direct contact with the analyzed surface and forms a nano-Schottky (Metal-Semiconductor) contact [9, 17, 18] (figure 2). Using a logarithmic amplifier with a dynamic range of seven orders of magnitude, the current flowing from the tip through the sample to the back-contact is recorded at each pixel, when a DC bias is applied between the tip and the sample back contact. For silicon, during SSRM measurements, a highly stressed region just below the tip is necessary to create the conductive β -tin silicon phase [19–21]. Therefore, SSRM measurements are carried out with a strong tip-sample contact, applying the necessary mechanical pressure [19]. Using ultra-hard tips (doped diamond) allows to avoid the deformation of the tip during the measurements and to guarantee the reliability of the generated data [22]. The equivalent model of this nanocontact is a sum of resistances in series: the tip resistance, the spreading resistance of the nano-Schottky contact, the contact resistance between the probe and the sample, the bulk resistance of the sample and the back-contact resistance [23, 24]. For a stable tip and a stable electrical contact of the sample with the AFM chuck, the tip, bulk and back-contacts resistances can be represented by a unique constant resistance; $R_{Constant}$ (figure 2). The local resistance of the sample is therefore the unique locally varying magnitude, and its variation can be imaged locally by the SSRM measurements to record 2D-maps of the local resistance. Three dimensional procedures have been also reported [17, 25–27].

For both SCM and SSRM modes, the obtained 2D acquisition maps consist in an image of the tip-sample system's electrical response a fixed set of AFM operating conditions (effective tip-sample contact area, applied force, DC bias, AC bias, frequency ...). For crystalline doped layers, for dopant concentrations from 10^{15} to 10^{20} at cm^{-3} , a good reproducibility with high spatial resolution have been demonstrated [28–31].

Nowadays, highly integrated semiconductor technologies aim at co-integrate many different devices, both of a two-dimensional (planar) and three-dimensional (vertical) type, simultaneously on or in the same substrate. During the semiconductor processing, two main issues appear during the layer deposition steps: first, deposition uniformity in the vertical structures (pores, columns, ...) and second, the control of mechanical deformation of the wafer (also called wafer warpage) due to the strain introduced by the deposited layers. Depending on their size and density, the vertical structures may have an important effect on the mechanical stability of the wafer, so that the deposition uniformity and the wafer warpage may differ both through the deposition furnace load and along the position on a single wafer. Therefore, the homogeneity in terms of layer thickness and electrical properties inside a given wafer (intra-wafer uniformity) but also along the different simultaneously processed wafers (inter-wafer uniformity) must be controlled and optimized. Resulting non-uniformities can concern either the layer thicknesses and the filling of the 3D structures. In addition, when the process includes several deep three-dimensional patterns and therefore weakening of the mechanical robustness of the wafer, critical wafer warpage can occur, leading to handling problems or wafer breakage and thus to significant line-yield falls. In order to avoid such problems, polycrystalline materials were often selected for the device fabrication. Layers exhibiting polycrystalline character represent the best trade-off between structure filling, wafer warpage, thickness uniformity and uniform electrical properties. Moreover, since uniform conductivity performances are required, an *in situ* doping technique is preferred over the classical implantation doping [32]. Fabricated as multiple layers, global electronic and mechanical properties are strongly dependent on the microstructure and internal phases of the used materials.

In order to study the electrical activation of dopant atoms by SCM and SSRM, we investigated a well-known *in situ* doped polycrystalline silicon (polysilicon) films. Electrical transport properties of polysilicon material have been understood for decades [33–36] and has enabled numerous applications in high integrated circuit and solar cells [37]. At the grain boundaries trapping centers of carriers and minority carriers' potential barriers have been researched to control the electrical efficiency of the deposited layer. The control of the microstructure [38, 39], electrical [40, 41] and mechanical properties of the polysilicon layer are of great importance in microelectronics because of their direct link with device performances and buckling failures at the wafer level. In order to minimize the device contact resistances [42], and to enhance carrier mobility and device drive current, semiconductor layers with high concentration (higher than 10^{20} cm^{-3}) are used. Deposited on an ultrathin SiO_x layer, a passivating contact is created, this structure is designed as a tunnel oxide passivating contact [43, 44].

In this context, we show that SCM and SSRM modes are perfect tools to provide answers to scientific and technological issues for semiconductor devices, especially for highly doped layers. In a previous study, we have demonstrated that AFM electrical modes allow to map the as-deposited polysilicon layer (with a phosphorus doping concentration of 10^{20} at cm^{-3}) [45]. Here, we go further by studying the nano-contact between the AFM tip and the sample to fully exploit the SCM and SSRM modes for both as deposited and annealed films. The goal is to highlight the capability of electrical modes based on AFM to mapping the dopant activation. The silicon layer is deposited with a polycrystalline *in situ* doped structure, with a high ($>10^{20}$ at cm^{-3}) phosphorus dopant concentration. For this, the macroscopic properties of the layers such as the average wafer stress, layer resistivity

evolution and Hall conductivities are determined. We analyze in this work, the close link between the microstructure and local electrical properties of a doped Low Pressure Chemical Vapor Deposition (LPCVD) polysilicon. The evolution of the microstructure after the annealing step is investigated using x-Ray Diffraction (XRD) combined analysis with MAUD software. This analysis allows to determine the anisotropic crystallite shape, crystalline texture, unit cell parameters and thickness of the polycrystalline films. The local properties of the layers are investigated by SCM and SSRM measurements, allowing for an insight on the nanoscale level, but also a comparison with the chemical doping compositions of the layers obtained by Secondary Ions Mass Spectroscopy (SIMS).

2. Experimental aspects

2.1. Materials

As substrate, (100) oriented, p-type (boron doped) single crystal silicon wafers were used. A silicon dioxide layer of 100 nm was grown on these substrates by wet thermal oxidation. Then, the highly *in situ* phosphorous doped polysilicon films were deposited by LPCVD with a total thickness around 750 nm. Note that, here we focus on the local measurement of the dopant activity of the highly *in situ* doped polysilicon, the used SiO₂ layer is relatively thick. These depositions were carried out in a conventional horizontal furnace, a horizontal hot wall reactor from THERMCO (5200 Series) with fused silica tube and liner, and silicon carbide wafer holder. For these experiments, the dilution ratio of phosphine (PH₃) in silane (SiH₄) has been fixed at 5×10^{-3} . A pressure of 26.6 Pa is used, and deposition temperatures varied from 560 °C to 635 °C.

The annealing steps were performed in a conventional horizontal furnace. In order to preserve the electrical properties of the as-deposited layers, a first annealing step is a low-temperature oxidation step under O₂ followed by a high-temperature step (under N₂). This way, a capping layer of polysilicon oxide is created at the surface. Afterwards, the wafers were annealed at 1000 °C during 40 min to achieve a homogeneous dopant redistribution and activation.

2.2. Characterization techniques

Polysilicon layer resistivities were determined from their resistance (measured by a four points probe equipment, Prometrix Omnimap RS35C) and thickness (measured by optical reflectometer, Nanospec AFT 4000).

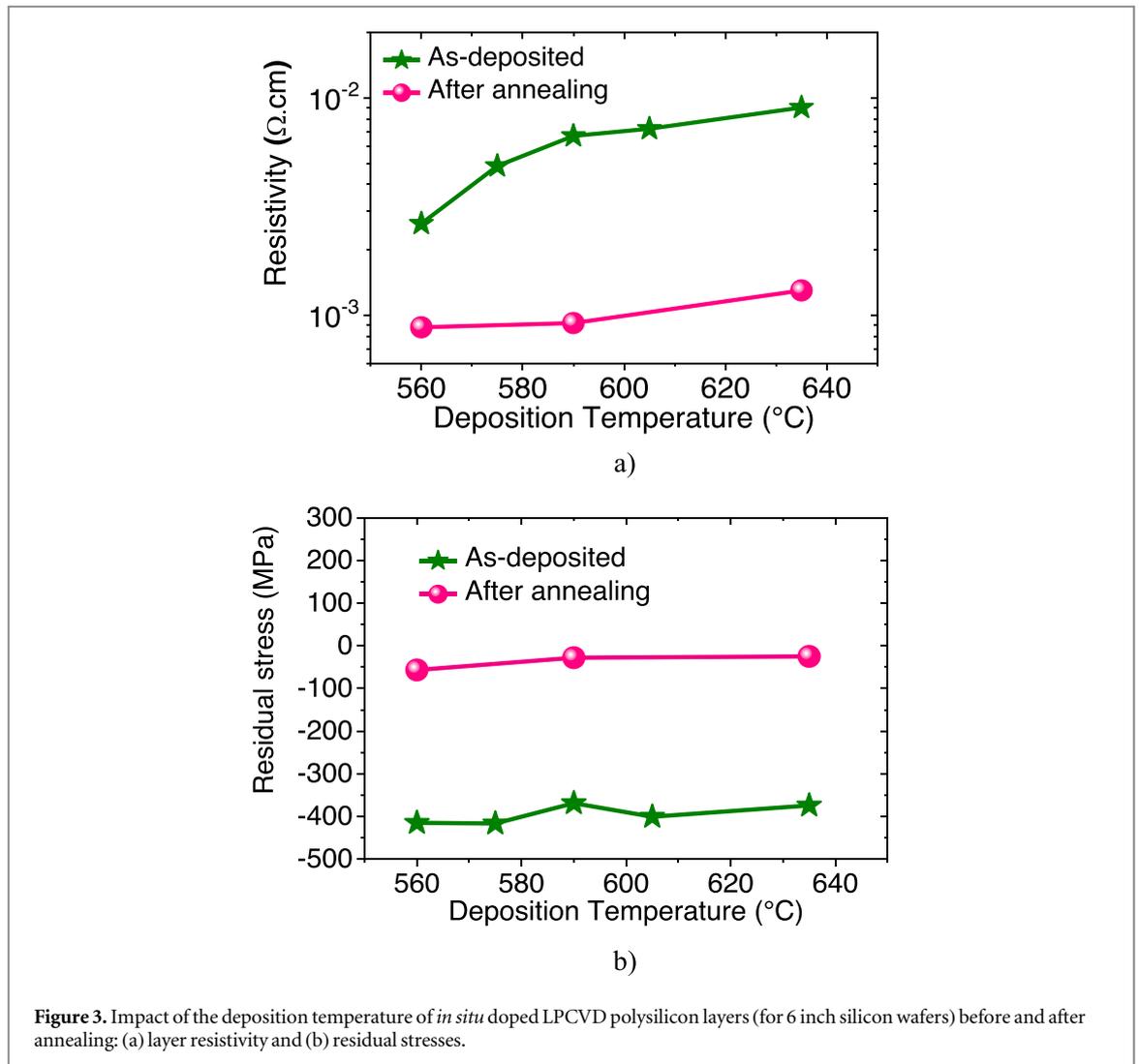
A FSM8800 curvature measurement system based on laser beam deflection was used to investigate the warpage. The average residual film stress in the polysilicon films is calculated, with the assumption of an isotropic distribution and the biaxial rotationally symmetric stress case, by the Stoney's equation [46]

$$\sigma = \frac{E_s}{6(1 - \nu_s)} \frac{t_s^2}{t} \left(\frac{1}{R_a} - \frac{1}{R_b} \right) \quad (1)$$

where E_s is the Young's modulus (1.3×10^{11} Pa) and ν_s the Poisson's ratio (0.28) of pure silicon, t_s and t the thickness of the silicon wafer and deposited film respectively, and R_a and R_b the measured radius of curvature after and before deposition, respectively.

Hall measurements were carried out on square pieces of 0.25 cm² obtained by cleavage. Four alumina contacts were deposited in the corners of the sample by evaporation and the electrical contact was achieved using wire bonding.

Quantitative analyses of the crystallographic textures and microstructures at the film scale was probed using 4-circles x-ray diffractometry with a setup equipped with monochromatized CuK_α radiation and a Curved Position Sensitive detector (CPS120 from ThermoFisher Scientific), described in details elsewhere [47]. The typical analyzed surface is of several mm², and the whole thickness of the layer is probed. We used the Combined Analysis formalism based on Full-Powder-Pattern Rietveld refinement [48], as implemented in the MAUD software [49], to determine simultaneously the textures and microstructures. Briefly, this methodology uses an extended cyclic Rietveld refinement of a series of x-ray diagrams measured at different sample orientations. We measured 936 diagrams every 5° in tilt an azimuth angles (χ and φ respectively), varying in the 0–60° and 0–355° ranges respectively, and for an incident angle of the x-ray beam on the sample of 20°. The instrument contributions (χ and ω broadenings, peak shapes, zero-shifts) were calibrated using the 660 srmb LaB₆ powder standard from NIST. A counting time of ten seconds for each sample orientation was used, and our optical setup provides with a 0.1° peak width in 2θ around 30°. Pole figures obtained are normalized into multiples of a random distribution (m.r.d). In such m.r.d units, a sample without preferred orientation exhibits uniform pole figures with 1 m.r.d levels, while a textured sample shows pole figures with maxima and minima of orientation densities ranging from 0 m.r.d (absence of crystals oriented in this direction) to infinity (for a single crystal on



few directions). The overall texture strength is evaluated through the texture index [49]. The normalized pole figures are calculated from the orientation distribution (OD) of crystallites, refined using the E-WIMV formalism after extraction of the peak intensities during the Rietveld cycles using the Le Bail approach. The OD and profile refinement reliabilities are estimated using conventional reliability factors.

The doping profiles along the layer thickness were obtained from phosphorus SIMS depth profiles using Cs^+ primary ions at 10 keV energy. Calibration of the SIMS apparatus was achieved with a phosphorus standard and the analyzed area was about $150 \mu\text{m}^2$.

AFM measurements were performed using a Dimension AFM (Bruker) operated at room temperature. A vibration-free table was used to eliminate any ground vibrations and/or acoustic noise. Tapping mode is used to acquire the topography. For SCM measurements, a Pt/Ir coated highly n-doped silicon probe (SCM-PIC) was employed. SSRM measurements were conducted with a highly conductive full diamond tip of Adama with an apex of 10 nm (AD-40-AS). The stiffness of the cantilever was determined by the thermal tune method, the spring constant of the cantilever of the used probe was 42 N/m. Force curves have been performed on a sapphire in contact mode to measure the sensitivity of the cantilever. For all electrical measurements, the scan rate was 0.5 Hz. All maps are recorded with a resolution of 512×512 pixels. Before and after each study, the tip apex integrity is checked either with SEM analysis (figure 1) or with a calibrating sample.

For the SCM and SSRM experiments, cross-sections of the samples were prepared. The sample was glued to a sample holder on the film side for protection, and the cross-sectional surface was then mechanically polished as to obtain a smooth surface. Successive polishing steps first with SiC paper with decreasing grain size down to $0.1 \mu\text{m}$ and then with colloidal solutions were done, until a mirror-like surface was obtained. For the SCM measurements, the cross section was annealed to obtain a native oxide layer. This annealing step was carried out at 270°C during 30 min. The thickness of the obtained oxide layer is estimated to be around 3 nm.

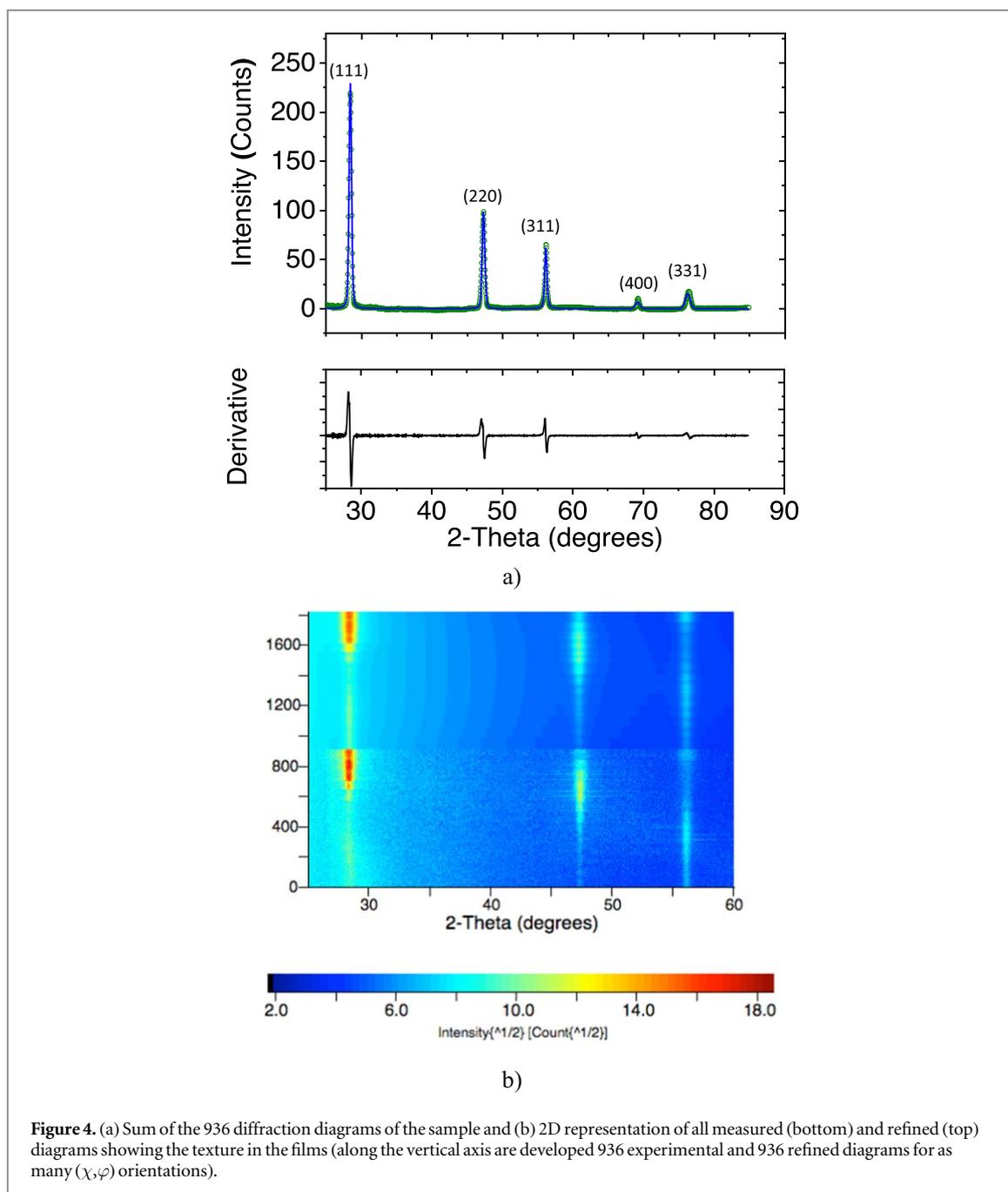


Figure 4. (a) Sum of the 936 diffraction diagrams of the sample and (b) 2D representation of all measured (bottom) and refined (top) diagrams showing the texture in the films (along the vertical axis are developed 936 experimental and 936 refined diagrams for as many (χ, φ) orientations).

3. Macroscopic characterizations: resistivity and stress

As function of parameters deposition, electrical properties are important parameters to control. In a first part, we compare the quantification of the properties (global resistivity, residual stress and microstructure) of the as-deposited highly *in situ* doped polysilicon layer before and after the annealing step. The evolution of the resistivity of the as-deposited layers as a function of the LPCVD deposition temperature is given in figure 3(a). The smooth evolution of the resistivity with the deposition temperature indicates the absence of any structural transformation, but it seems also that the doping species incorporation (from an electrical point of view) within the crystal lattice is better at low deposition temperatures, probably linked to the enhanced grain growth. In fact, lower deposition temperatures favor the grain growth over nucleation, leading to larger grains. Therefore, it decreases the grain boundary density, inducing less defects in the films. Finally, it enables larger doping efficiencies and reduces charge carriers scattering, decreasing the film resistivity.

To activate the dopant in the polysilicon layer, three wafer sets were annealed as described in the experimental section. A resistivity in the order of $10^{-3} \Omega \cdot \text{cm}$ is achieved after annealing for all initial deposition temperatures, showing that the annealing process is homogeneous for all the polycrystalline films.

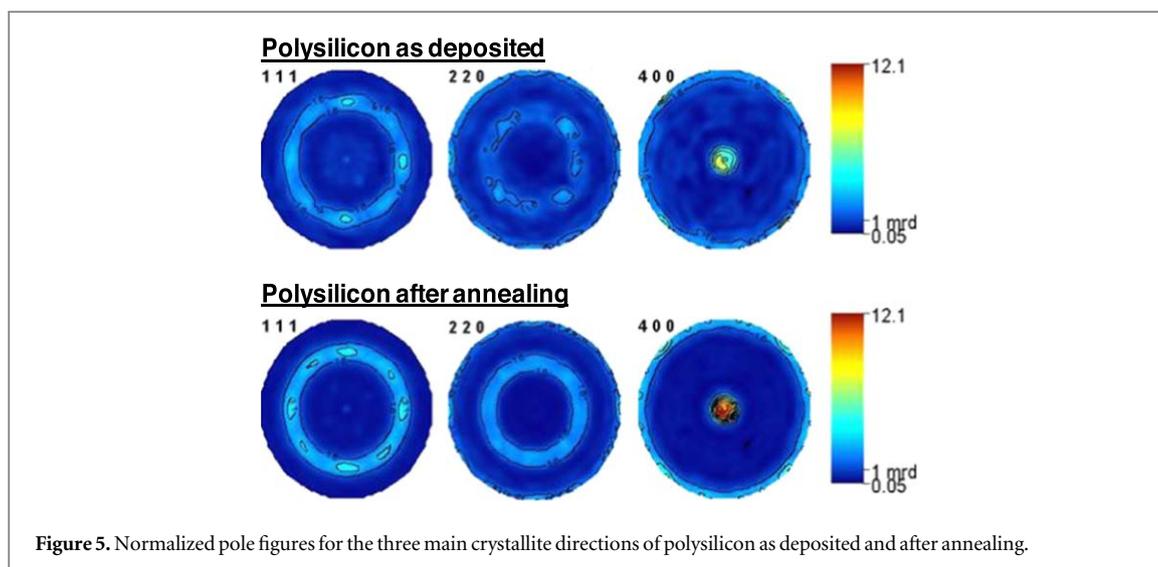


Figure 5. Normalized pole figures for the three main crystallite directions of polysilicon as deposited and after annealing.

In addition, during the manufacturing process, the electrical properties are not the only parameter to be taken into account to determine the optimized deposition parameters. In fact, for strongly thinned wafers or for high densities of 3D structures, a wafer deformation may have a severe impact during the fabrication process. The residual stress of the as-deposited films is represented in figure 3(b). For all deposition temperatures, the residual stress of the layer is compressive, with an only small variation.

The high temperature annealing also significantly reduces the film stress to a moderate tensile stress of about 25 MPa. Therefore, the annealing process leads to the activation of the dopant in the polycrystalline film and an important reduction of the residual strain independently on the initial deposition temperature.

In the following, we will focus on the study of the LPCVD film deposited at 635 °C.

4. Microstructure characterization

X-Ray Diffraction (XRD) combined analysis were performed to reveal the texture and the structure of the polysilicon layers [48, 50]. Mean crystallite anisotropic shape and sizes, cell parameter and quantitative crystallographic textures are calculated from XRD measurements. Combined analysis Measurements and fits are presented for the sum of all measured diagrams (figure 4(a)) and for all diagrams as a 2D plot (figure 6(b)). Calculated and observed diagrams favorably compare, with relatively low reliability factors and GoF (Goodness-of-Fit) values for the whole set of 936 diagrams (table 1). The film structure is consistent with a regular diamond cubic structure of silicon with a cell parameter around 5.43 Å. When tilting the samples, significant peak shifts could be observed, indicating stabilization of residual strains in the films. The cell parameter value given here corresponds to the refined relaxed state, provided by the combined analysis approach. It is then the cell parameter of the unstrained film which would have been prepared using exactly the same conditions. The refined values are always larger than those for bulk silicon.

The as-deposited sample exhibits small mean crystallite sizes (i.e. mean coherent size domains) of about 120 Å and quasi isotropic shapes (with an anisotropic shape factor Γ very close to 1). The annealing induces a strong grain growth and the development of an enhanced texture. According to our measurements, annealed samples present [111]-elongated crystallites with a largest dimension reaching 6400 Å and a larger anisotropic shape ratio. It results in ellipsoidal shaped crystallites whose largest length is along the [111] direction. Regarding crystallographic texture (figure 5), the {400} pole figures exhibit a maximum distribution density value in their center, corresponding to the normal Z to the film plane. Another large density value is observed on a ring along the equator of these pole figures, showing then the existence of a $\langle 100 \rangle$ -cyclic-fiber texture component, with the $\langle 100 \rangle$ fiber axis being aligned with Z. From the three recalculated and normalized pole figures this texture component seems to be major, and an important amount of crystallites are then aligned with their $\langle 100 \rangle$ direction parallel to Z of the substrate. However, the ring observed on the equator of {400} is deviating slightly from perfect homogeneity, along the X and Y directions of the sample corresponding to the main axes of the substrate. It then exists also a minor orientation component corresponding to a kind of epitaxial relationship with the substrate defined by $\langle 100 \rangle$ -polysilicon//[100]-Si. These two components of orientation are observed as well in as-deposited as in annealed samples. After annealing, the pole figure exhibits enhanced orientation densities. It appears that the highest density is reached in the center of the {400} pole figure (12.1 m.r.d.). From

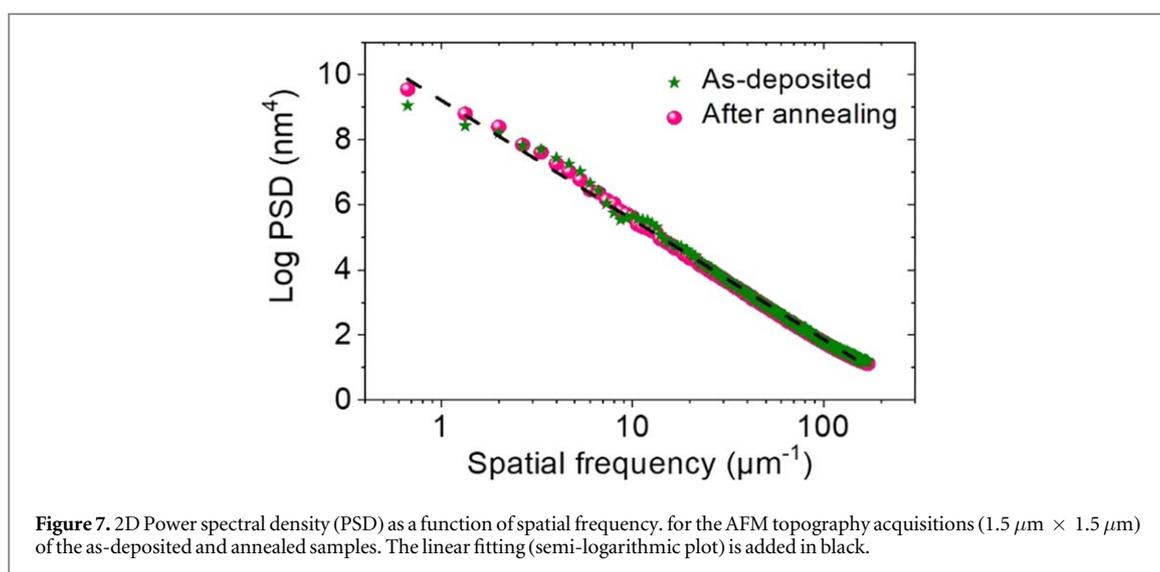
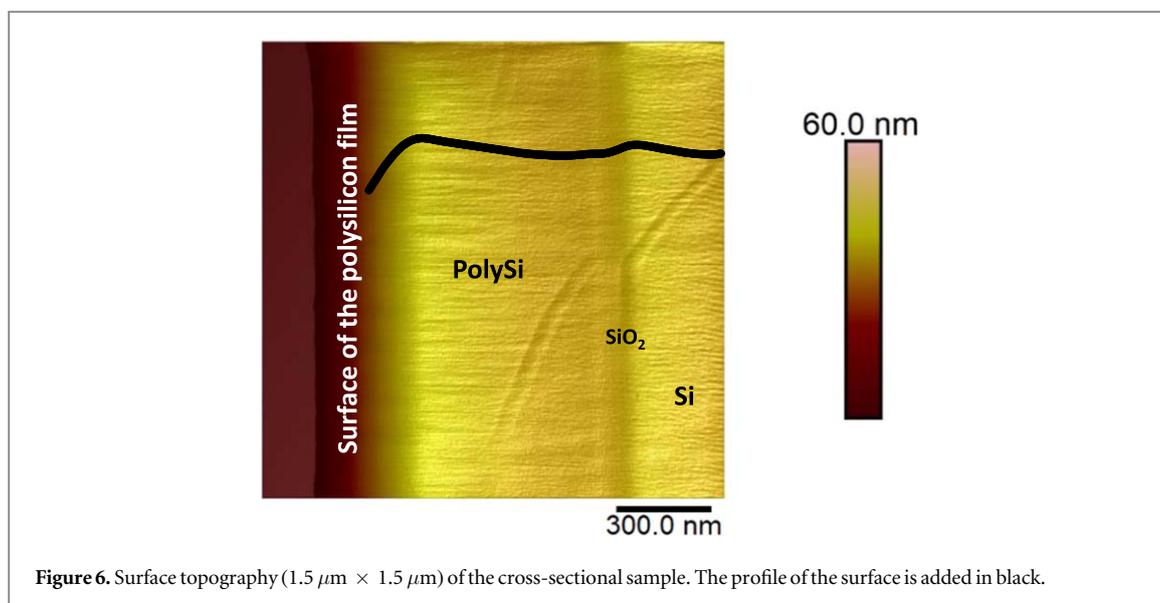


Table 1. Structural and microstructural parameters of the films resulting from the Combined Analysis refinement. a : cell parameter. Δa and $\Delta a/a$: absolute and relative difference in cell parameter from bulk silicon (5.43088 \AA). thickness values from interferometry measurements. Γ : grain shape anisotropy factor. maximum and minimum orientation densities on the $\{100\}$ pole figures. F^2 : texture index. Reliability standard R-factors for the refinements: R_w : weighted. R_{exp} : experimental. $GoF = (R_w/R_{exp})^2$.

Sample		As-deposited	After annealing
	Film thickness (nm)	759	761
Lattice parameter	a (\AA)	5.43109 (6)	5.43566 (2)
	Δa (\AA)	-0.00021	-0.00478
	$\Delta a/a$ (%)	-0.004 (6)	-0.088 (2)
Anisotropic (i.e. crystallite) size	[111]	122.9 (2)	6388 (77)
	[220]	118.7 (2)	973 (35)
	$\Gamma = [111]/[220]$	1.03	6.52
Texture parameters	Max (m.r.d.)	7.5	12.1
	Min (m.r.d.)	0.05	0.06
	F^2 (m.r.d.) ²	20.42	20.38
	Confience factors (%)		
	R_w	22.3	23.5
	R_{exp}	18.6	18.7
	$GoF (R_w/R_{exp})^2$	1.44	1.58

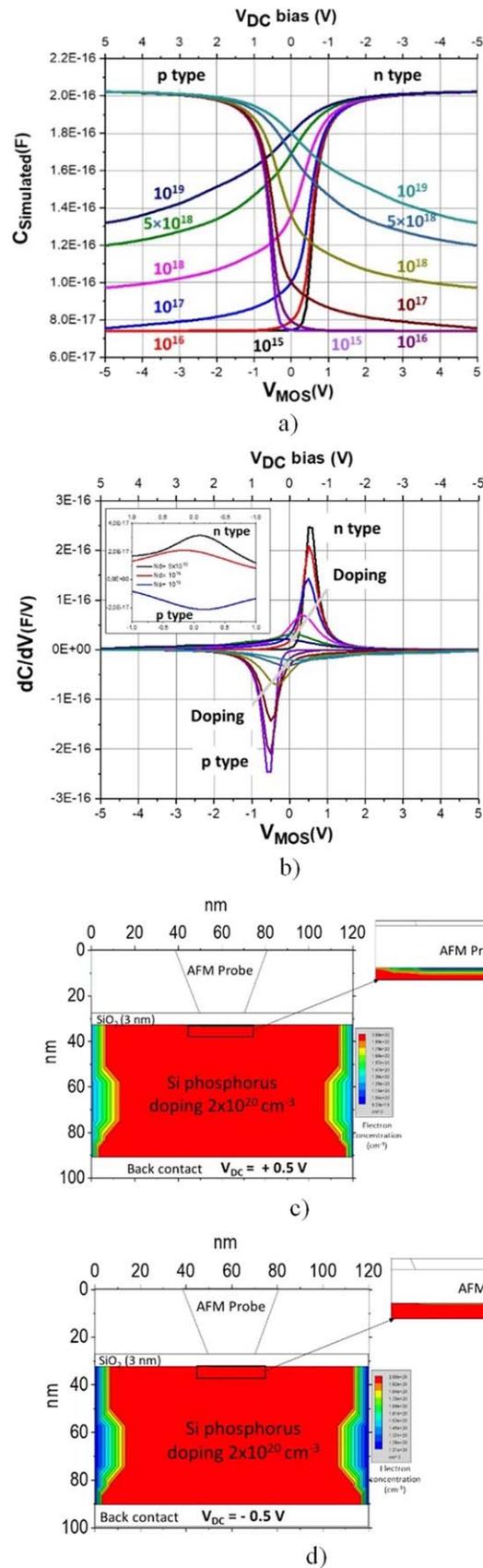


Figure 8. (a) C-V simulations of the nano-MIS contact for different doping levels. (b) dC/dV curves calculated from the simulations with the same color-code for the doping levels as in (a). The inset shows the case of the highly doped silicon. 2D TCAD simulations for a n-type layer with a charge concentration $2 \times 10^{20} \text{ cm}^{-3}$ for $V_{\text{DC}} = +0.5 \text{ V}$ (c) and for $V_{\text{DC}} = -0.5 \text{ V}$ (d).

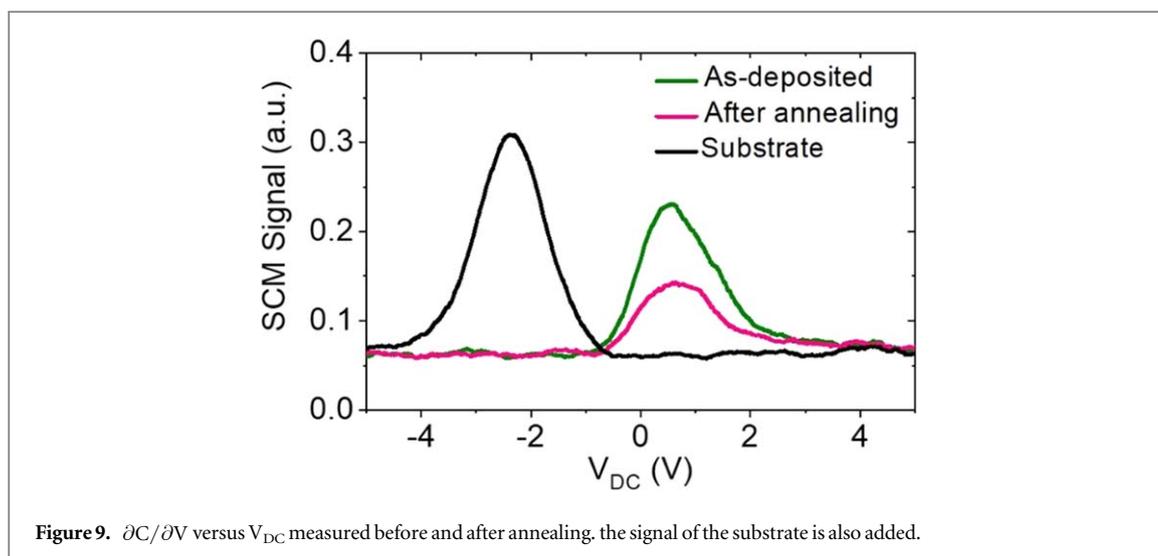


Figure 9. $\partial C/\partial V$ versus V_{DC} measured before and after annealing. the signal of the substrate is also added.

x-ray analysis, we demonstrate that the annealing process then favors the achievement of larger texture strengths in the films.

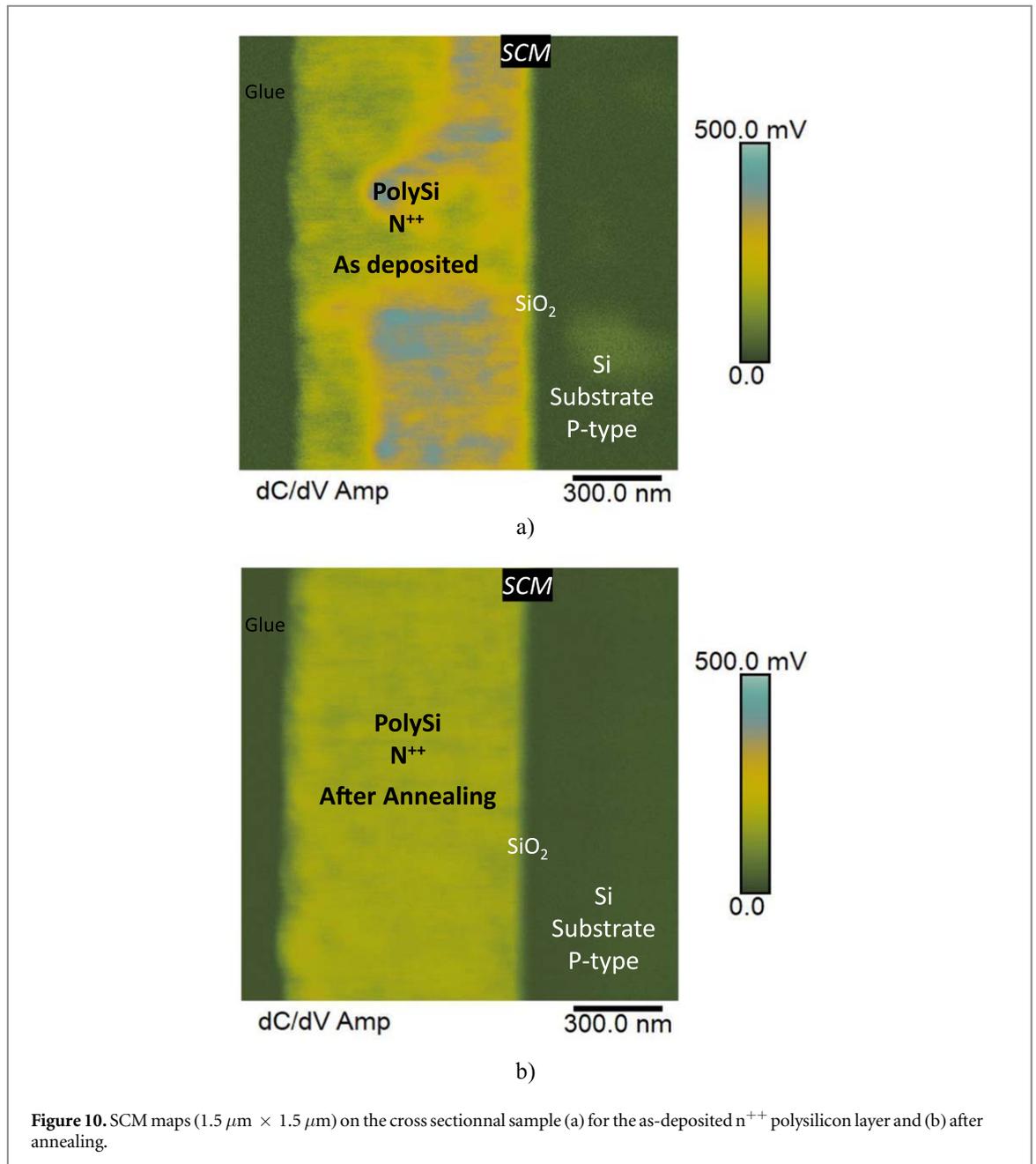
The crystalline structure was studied using XRD measurements, and shows a polycrystalline character with a main grain size about 123 Å in the [111] direction and 119 Å for the [220] direction before annealing, with a grain shape anisotropy factor of about 1.03. After annealing, the combined analysis showed that the grain size of the polysilicon increases by a factor of 52 in the [111] direction and of 8 for [220] direction. With XRD investigations, the crystallization effect was investigated and we have proved that after annealing polysilicon grains are significantly larger. This 3-D enlarge was also quantify. We assume that larger grains may explain the differences in terms of electrical performances noticed by the layer resistivity. After annealing, doping atoms may be more efficient and electrons may thus be more mobile. Then to study the local electrical properties, electrical measurements on AFM were performed.

5. Local electrical characterization

The topography of the layer after annealing is represented in figure 6. Despite the presence of some stripes due to the polishing process, we obtain a roughness in the polysilicon layer of $Sq = 1.8$ nm and $Sa = 1.3$ nm (statistical parameters calculated with the standard ISO 25178 [51]). This high-quality surface is in perfect adequation with nano-electrical modes in contact to ensure electrical stability [52]. Furthermore, the Power Spectral Density (PSD) analysis have been performed for the surfaces of the cross-sections of the samples before and after annealing [53, 54]. Figure 7 displays the 2D PSD curves obtained for the two samples. The two PSD curves show the same evolution as the fonction of the spatial frequency. The linear fitting of the semi-logarithmic plot is added. We can note a small difference at low frequencies (corresponding to large superficial features), probably due to the topographical change at the layer surface of the cross-section, related to the prxence of the glue. On the other hand, at high frequencies (above $10 \mu\text{m}^{-1}$) the curves are superimposed, the two samples present similar roughness.

For this highly doped layer, we have simulated the nano-electrical MIS contact with TCAD tools in order identify the extention of the measured properties with high precision. The conductive AFM tip in contact with the doped silicon layer was modelled as a nano-MOS structure. A planar contact with symmetry around the tip axis is simulated, the tip radius is 20 nm.

The thickness of the oxide layer on top of the cross-sectional sample was fixed to 3 nm, corresponding to the thickness estimation based on the preparation method of the cross-section. The simulations were carried out for silicon (n- and p-type) and a metal contact at the bottom was added to simulate the contact with the chuck. Thereby, the C-V curves are generated for different doping concentrations (figure 8(a)). The simulations have been done with a voltage sweep starting from negative biases (-5V) towards positive biases ($+5\text{V}$). The bias simulated here (V_{MOS}) is the inverse of the bias V_{DC} applied to the AFM chuck during measurements. As expected, the shape of the C-V curves depends on the doping concentration and the type of the silicon substrate. These simulated curves are in accordance with previous works [16, 55, 56]. Based on the SCM methodology, the doping concentration increase induces a decrease of the slope of the C-V curves and a shift of the position of the inflexion point of the curve. In order to highlight the strong impact of the V_{DC} voltage during the measurement of the highly doped polysilicon layer, the simulated dC/dV curves are displayed in figures 8(b) for different



doping levels (the high doping levels are shown in the inset). As we can see, when the doping level increases, the the derivative capacitance drops drastically. Therefore, in the present work, since the material is highly doped ($<10^{19} \text{ at cm}^{-3}$), a fine determination and control of the applied voltage is crucial to deplete the carrier charge under the tip contact and then perform an accurate analysis.

In addition, electron concentration distributions are represented for two V_{DC} (figures 8(c) and (d)), for a silicon layer doped at $2 \times 10^{20} \text{ at cm}^{-3}$. For $V_{\text{DC}} = +0.5 \text{ V}$, the TCAD simulation shows clearly the depletion area formed under the oxide layer at the tip contact, well confirmed by the reduced carrier concentration visible in the simulations under the tip. It is interesting to observe that despite the high carrier concentration in the polysilicon layer, the extension of the probed area of the sample is only slightly larger than the tip-sample contact, allowing therefore for an excellent spatial resolution. Therefore, the capacitance variation $\partial C/\partial V$ can be measured at this applied voltage when the V_{AC} is superimposed. While for $V_{\text{DC}} = -0.5 \text{ V}$ the accumulation regime is reached.

In order to quantify the effect of the V_{DC} for this highly-doped layer, we perform the local measurements. For this, we use the spectroscopic mode: the tip is localized on a fixed position on the sample and the AFM SCM signal versus applied voltage is recorded, and the $\partial C/\partial V$ signal is measured during a sweep of the V_{DC} bias (figure 9). We performed this analysis at the center of the polysilicon layer. For the as-deposited film, the peak position is located at 0.53 V, and shifts slightly to higher voltage when the layer is annealed, while the amplitude

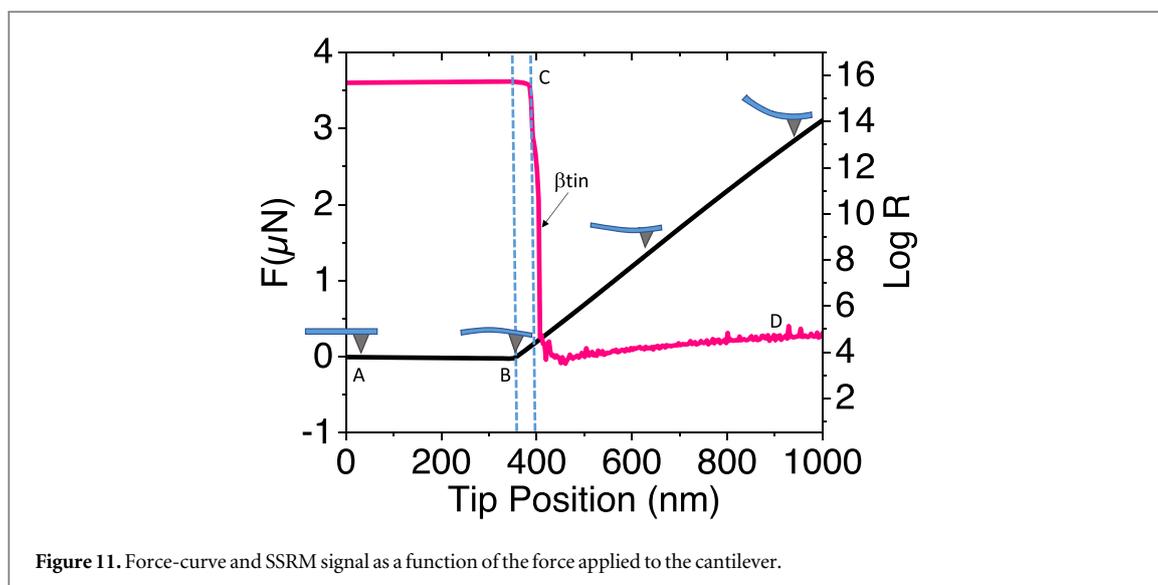


Figure 11. Force-curve and SSRM signal as a function of the force applied to the cantilever.

of the SCM signal decreases. Since $\partial C/\partial V$ is inversely proportional to the active doping level of the semiconductor, this behavior indicates clearly an increase of the active dopant concentrations in the polysilicon layer after the annealing step in perfect agreement with the simulations. For a positioning of the tip on the p-type substrate, the SCM signal shows a maximum at negative DC sample bias, according to the C-V change simulated by TCAD (figure 8(a)). Thus the control of the applied V_{DC} during SCM experiments plays a crucial role in the interpreting measured signal. This point is very important and even more for highly doping layer since the flat band voltage is shifted from 0 V.

Based on these results, an applied V_{DC} bias of 0.5 V and $V_{AC} = 1$ V is chosen for the comparison of the polysilicon 2D SCM mappings. The obtained SCM maps of the *in situ* doped polysilicon layer before and after annealing are shown in figure 10. In both acquisitions, the polysilicon layer can be clearly distinguished from the p-type substrate, due to the strong $\partial C/\partial V$ contrast at the chosen V_{DC} bias. The corrugated surfaces of the polysilicon materials at the interfaces with the glue (used to fabricate the cross-sectional samples) are related to the crystalline nature of polysilicon grains determined by XRD investigations. By comparing the two maps, the modification of the carrier distribution and activation during the annealing can be clearly observed. In fact, before annealing, the polysilicon layer presents a non-homogeneous doping carrier concentration of the active dopants concentration along the layer. After annealing, the polysilicon layer shows a uniform active dopant distribution in the bulk of the layer, and a smooth interface with the substrate. The oxide layer at the interface with the wafer seems to be slightly better defined, translating an electrical activation of the dopants reaching the polysilicon/oxide layer without any charge-depleted zone in the polysilicon layer. Also, at the surface of the polysilicon layer after annealing, a well-defined charge depleted region can be observed, corresponding to the oxide layer created before the principal annealing step in order to avoid the out-diffusion of the dopants.

SSRM is also deployed to analyse the activation of the dopant in the semiconductor layer. To carry out SSRM measurements with a high control, it is very important to control the tip-semiconductor contact [17, 24]. To quantify the force to be applied to the cantilever in order to create the β -tin pocket under the tip, a force curve was recorded on the polysilicon layer, with the corresponding measured resistance. In figure 11, we have represented both the force curve and the SSRM signal as a function of the Z position of the AFM piezoelectric displacement. Far from the sample, the SSRM resistance is larger than $10^{15} \Omega$ because of the absence of contact. Afterward, the cantilever is pulled down towards to contact the silicon surface (at the point B). At this displacement of 350 nm, the tip-sample contact is established, indicated by a change of slope in the force curve. With a further increase of the displacement, the diamond tip starts to penetrate the sample. Interestingly, a further displacement of 37 nm is necessary before the electrical resistance (SSRM signal) drops. This behaviour is the signature of the creation of the highly stressed β -tin region just below the tip contact. It is important to note that this distance corresponds to the displacement of the Z-piezo and represents the cantilever deflection and the effective penetration of the SSRM tip in the surface. The reaction of the cantilever has to be taken into account, so that the real penetration of the tip in the sample is smaller. When the force increases further, the resistance drops until reaching a plateau (D). The tip resistance contribution was measured in a conductive material (aluminium layer on another sample), the value is lower than $10^4 \Omega$.

With this calibration step, the scanned parameters for SSRM were fixed at $2.5 \mu\text{N}$ applied to the cantilever and a V_{DC} of 600 mV. During measurement, we verified the stability of the signal with the applied V_{DC} .

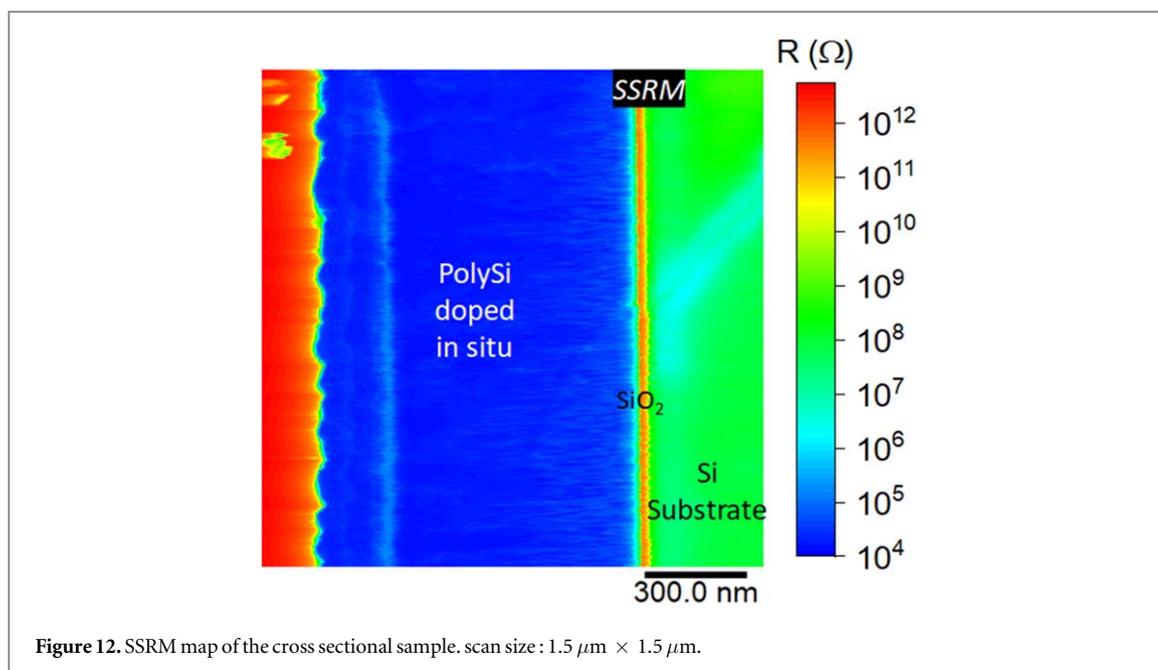


Table 2. Mean values for Phosphorus concentration from Hall Effect measurements.

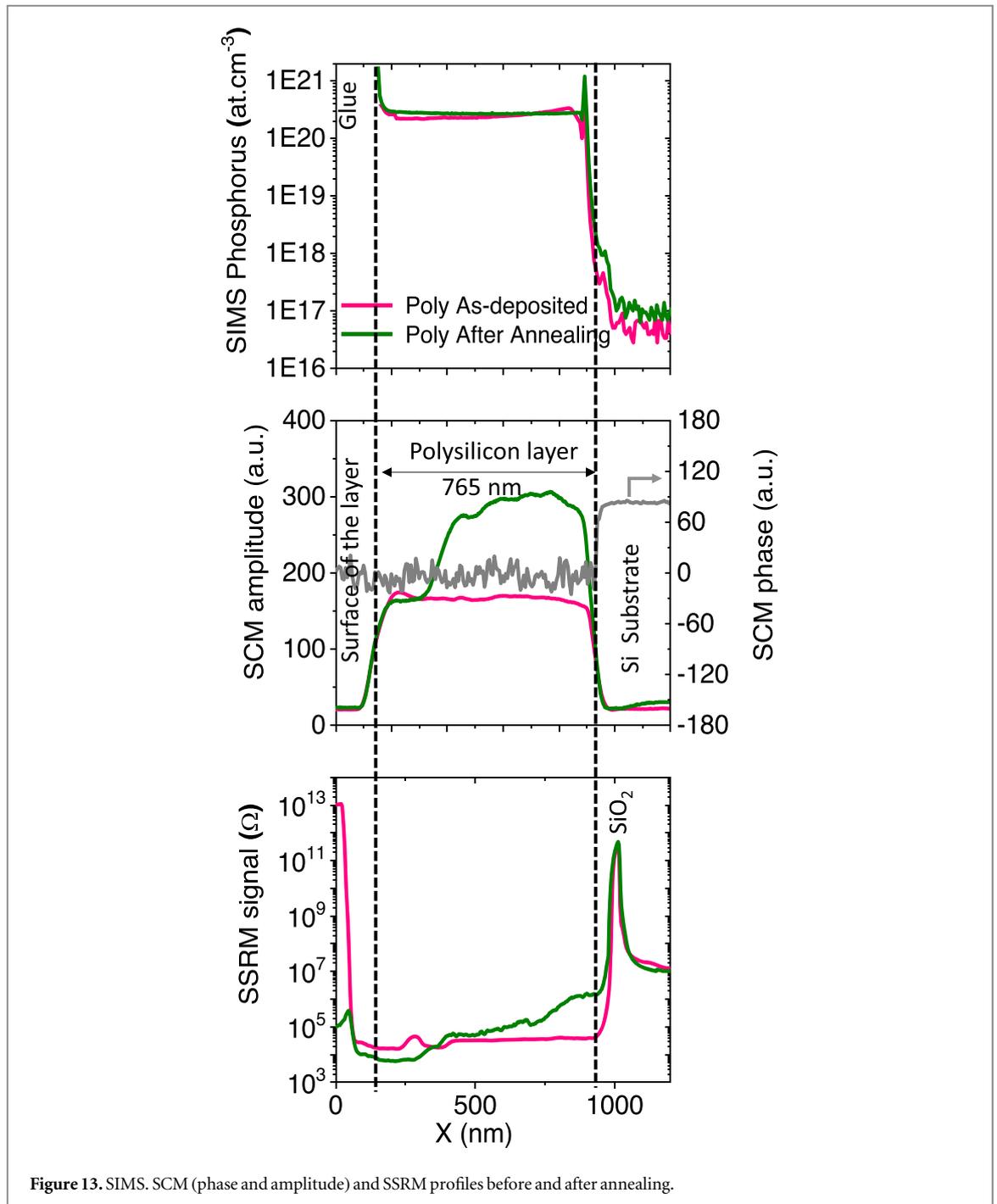
Sample	Phosphorus atoms concentration from Hall effect measurements (cm^{-3}) <i>Electrically active charge carriers</i>	Phosphorus atoms concentration from SIMS measurements (cm^{-3}) <i>Total amount of doping species</i>	Doping Efficiency (%) <i>Active carriers/Total carriers</i>
As-deposited	8.1×10^{19}	2.5×10^{20}	32
After annealing	2.4×10^{20}	2.7×10^{20}	89

according to the procedure presented in [17]. The SSRM map for the sample after annealing is represented in figure 12, in a 2D top view.

Again, the SSRM maps show a strong contrast between the substrate and the polysilicon layer, related to the change in dopant concentration. The polysilicon layer itself shows a homogeneous resistance through the bulk of the film, although some contrast is visible in the top part of the layer. At the interface with the glue, the SSRM contrast is correlated with the topography of the cross-sectional sample (figure 6): the curvature at the top of the layer (due to the polishing step) induces a change in the tip contact area and the exerted force, leading to this contrast. Also, at the surface of the polysilicon layer, the insulating region can be identified (light blue region at the top). This insulating region is related to the oxidation step in the annealing procedure, creating an oxide layer in order to trap the dopants. The SSRM mapping allows therefore to estimate the thickness of this layer to be around 45 nm. Furthermore, the oxide layer at the polysilicon/wafer interface can be distinguished clearly due to its insulating character, a high resistance is measured.

To complete the electrical investigations, the total phosphorus doping concentration for as-deposited and annealed samples was determined by SIMS (chemical analysis) on cross-sectional samples. The mean value of phosphorus concentration measured inside the layers before and after annealing are compared with Hall effect measurements in table 2. The dopant efficiency for the *in situ* doped layer is determined, showing that while only 32% of the dopants are active in the as-deposited state, close to 90% participate in electrical transport after the annealing step.

To highlight the complementarity of the SCM and SSRM modes, the profiles of SIMS, AFM electrical modes are compared in figure 13. Based on the detection of phosphorus atoms, the SIMS measurement allows for a 1D depth analysis. Despite its excellent accuracy, SIMS is limited to the chemical information of the material. In the case of activated dopants as in polysilicon material, the chemical information (presence of the chemical species) is different from the active carrier concentrations in the layer. In fact, the change observed in the Hall effect carrier concentration underlines the electrical activation of the P dopants during the annealing steps. As can be observed in figure 13, the SCM profiles show clearly the change in active doping concentrations before and after the annealing.



But even more, the chemical signature (SIMS profiles) of the phosphorus concentration remains unchanged after activation of the dopants, i.e. annealing. Thus, the annealing does not have an effect on the distribution of the dopants, only on activation of their charges. The electrical characteristics related to the transport properties of the polysilicon layer deposited on the oxide layer and the p-type substrate are clearly determined by SCM and SSRM. The results of the two modes, when executed carefully, can be compared directly. The SCM and the SSRM profiles allow therefore to estimate the electrical thickness of the polysilicon layer to be around 765 nm. Therefore, based on a nano-MIS and a nano-Schottky properties, we demonstrated the complementarity of the SCM and SSRM, respectively, to analyze highly doped and nano-structured films. As the conductive tip in contact with the analyzed surface represents a singular nano-object, our results show clearly that the control of the AFM parameters: tip properties, applied force, applied V_{DC} voltages during SCM and SSRM measurements allows to determine the dopant activity of the passivating contact. Furthermore, to finely control transport properties of materials, SCM and SSRM are complementary to the chemical compositions analysis obtained by SIMS, TOF-SIMS or Atom Probe Tomography (ATP).

6. Conclusion

The macroscopic and local structural and electric properties of a highly n-doped polysilicon LPCVD layer were investigated before and after the annealing step regarding the distribution and the activation of the dopants. The annealed layers show optimized properties for co-integrated device technologies and also for the filling of high aspect ratio 3D structures, as well as to achieve low resistance contacts and low passivating contacts. With a stress level of -25 MPa of the annealed film, wafer warpage can be minimized. In addition, the mean macroscopic resistivity decreases by the annealing, from $8 \times 10^{-3} \Omega \cdot \text{cm}$ to $7.3 \times 10^{-4} \Omega \cdot \text{cm}$, while the Hall mobility increased from 9.2 to $35.4 \text{ cm}^2/\text{V}\cdot\text{s}$. Combined XRD measurements revealed that grain growing occurs preferentially along [111] axis whose highest dimension of elongated crystallites reach 6400 \AA .

The analysis of the local properties, by SCM and SSRM, reveals a homogeneous active dopant distribution throughout the layer after annealing. These insights cannot be obtained by the combination of macroscopic characterization techniques or chemical analysis, underlining the interest of local electrical modes based on AFM. But even more, the two applied electrical modes, SCM and SSRM, are clearly complementary due to the contact formed between the tip and the sample. With the MIS-contact in the SCM mode, the SCM signal is sensitive to the active dopant distribution, through the modulation of the bias voltage. On the other hand, although employed at its detection limit due to the strong doping of the polysilicon layer, the SSRM signal using a tip-sample contact of the Schottky type, allows to extract the local resistivity and detect local resistivity variations. Here, insulating parts of the sample, as the oxide interface layer, can be localized. By compiling all results, we concluded that electrical transport investigations based on AFM are key parameters to reveal dopant activation in nano-structured films, even very heavily doped.

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Data availability statement

No new data were created or analysed in this study.

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