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New barrier layer design for the fabrication of gallium nitride-metal-insulator-semiconductor-high electron mobility transistor normally-off transistor

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Abstract

This paper reports on the fabrication of an enhancement-mode AlGaIn/GaN metal-insulator-semiconductor-high electron mobility transistor with a new barrier epi-layer design based on double $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ barrier layers separated by a thin GaN layer. Normally-off transistors are achieved with good performances by using digital etching (DE) process for the gate recess. The gate insulator is deposited using two technics: plasma enhance chemical vapour deposition (sample A) and atomic layer deposition (sample B). Indeed, the two devices present a threshold voltage (V_{th}) of +0.4 V and +0.9 V respectively with ΔV_{th} about 0.1 V and 0.05 V extracted from the hysteresis gate capacitance measurement, a gate leakage current below $2 \times 10^{-10} \text{ A mm}^{-1}$, an $I_{\text{ON}}/I_{\text{OFF}}$ about 10^8 and a breakdown voltage of $V_{\text{BR}} = 150 \text{ V}$ and 200 V respectively with $1.5 \mu\text{m}$ thick buffer layer. All these results are indicating a good barrier surface quality after the gate recess. The DE mechanism is based on chemical dissolution of oxides formed during the first step of DE. Consequently, the process is relatively soft with very low induced physical damages at the barrier layer surface.

Keywords: high electron mobility transistor, normally-off, gallium nitride, gate recess

(Some figures may appear in colour only in the online journal)



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1. Introduction

Gallium nitride (GaN) is one of the best candidate for high frequency and high power applications [1, 2] thanks

Table 1. Summary of the main GaN-HEMT normally-off technologies published in the literature. The V_{th} extraction technique is not the same for all these references.

Processing technic	V_{th} (V)	V_{GS} swing (V)	Reference
	3.60	−5–12	[9]
Fluorine implantation	0.55	−2–2	[10]
	3.59	−2–8	[11]
	1.70	0–8	[16]
P-GaN	3.03	0–10	[18]
	1.02	0–9	[19]
	1.20	−1–12	[22]
Recess	5.00	−3–9	[23]
	1.15	−2–12	[25]

to its outstanding material properties (high breakdown voltage, high electron velocity and good thermal conductivity) and advances in electrical modelling [3, 4]. The standard AlGaIn/GaN high electron mobility transistor (HEMT) device is a depletion-mode (D-mode) transistor. However, researchers are encouraged to develop enhancement-mode (E-mode) AlGaIn/GaN HEMT due to its several applications in analog, digital [5] and automotive industry [6]: for example, it provides essential fail-safe operation and simple circuit architecture for power switch applications [7] as well as allowing simple design for RF and microwave circuits [8].

To have an E-mode device, several ways are used to shift the V_{th} towards the positive value such as, fluorine implantation [9–11], introduction of additional layers on top of the barrier layer [12–19], fin-structure [20, 21] and gate recess [22–25] (table 1). One of the most common methods for the last approach is the gate recess using plasma which induces some degradation at the surface of the barrier layer [26]. To overcome this problem, the gate recess by digital etching (DE) process is used to minimize the degradation at the barrier layer surface [27, 28]. Self-limiting nature of the DE process allows an accurate control of the etching.

In this work, a new HEMT heterostructure (figure 1) based on a double AlGaIn barrier layer is proposed to obtain E-mode devices. The goal of the top AlGaIn barrier (etched by DE process) is to increase the charge density in the access region to reduce the serial resistance while keeping the charge density underneath the gate low enough to achieve a normally-off transistor. Thanks to the decorrelation in the optimization process between the internal part underneath the gate and the external part in the access region of the device, the Normally-off transistor is exhibiting good electrical performances.

2. Device fabrication

The HEMT epitaxial structure grown in CRHEA-France on silicon (111) substrate used in this study is shown in figure 1. The epi-structure starts with 1.5 μm GaN buffer layer followed by 5 nm $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ layer, 2 nm GaN layer and finally 10 nm $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ layer. At the end, the epi-structure is capped with 5 nm *in situ* SiN. The first 5 nm $\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$ layer has been

SiN cap	5 nm
$\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$	10 nm
GaN cap	2 nm
$\text{Al}_{0.2}\text{Ga}_{0.8}\text{N}$	5 nm
GaN	1.5 μm
AlN	16 nm
GaN	0.6 μm
AlN	0.2 μm
Si(111)	

Figure 1. Cross section of the epitaxial structure.

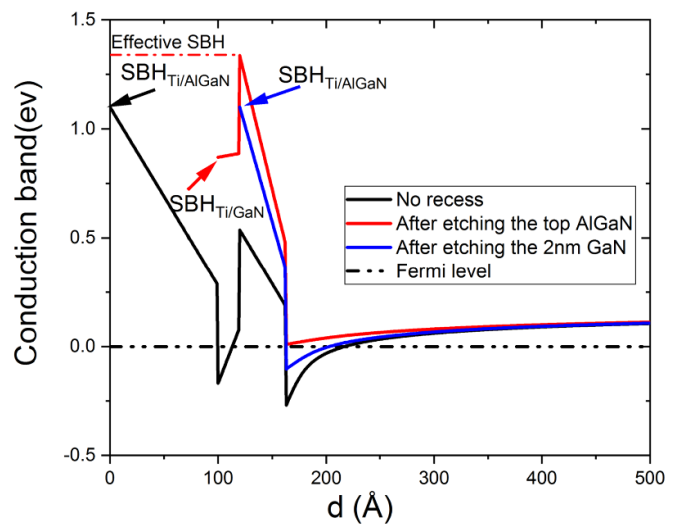


Figure 2. Schrödinger–Poisson simulation results.

defined after achieving a calibration design of experiment that ends up with an epi-structure which is totally depleted from free carriers.

A Schrödinger–Poisson simulation (figure 2) of the epitaxial structure has been performed to show the band gap engineering optimization process. This simulation takes only in account the four top layers of the heterostructure (AlGaIn–GaN–AlGaIn–GaN).

When the gate recess reaches the thin GaN layer (2 nm), the effective Schottky barrier height (SBH) of the gate electrode is about 1.3 eV taking advantage of the conduction band discontinuity (ΔE_c) between GaN and AlGaIn. The effective barrier height corresponds to the maximum band diagram energy that the electrons should overcome to go from the metal to the channel. The conduction band in the channel is then lifted-up over the Fermi level, which leads to a low charge density in the channel. The device pinch-off voltage is then shifted towards the positive values. After removing the entire thin

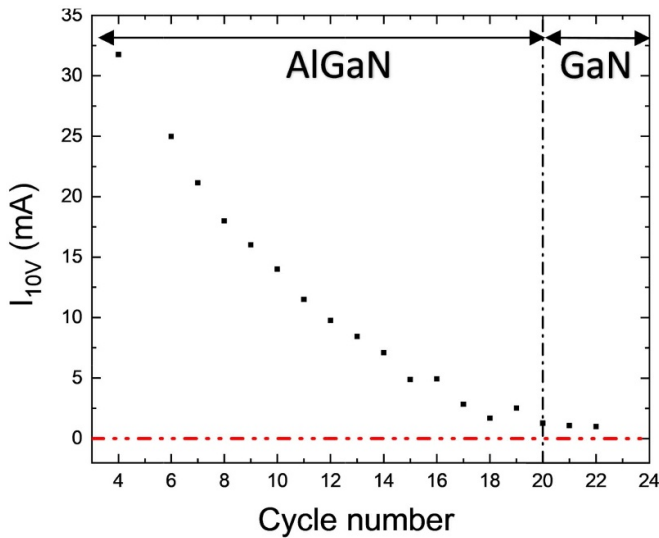


Figure 3. Current measured at 10 V versus the DE cycle number.

GaN layer, the V_{th} will shift back towards the negative values (blue curve). In order to keep the E-mode behaviour of the device with the present epi-layer structure, etching must be stopped before removing the 2 nm GaN layer, otherwise the device will become again D-mode or at least less E-mode.

The HEMT fabrication process performed at LN2-Canada laboratory starts with Ti/Al/Ni/Au ohmic contacts deposition using E-beam evaporation followed by a rapid thermal annealing then the device isolation is performed by N^+ ion multiple implantations. Afterwards, a 50 nm SiO_2 layer is deposited by plasma enhance chemical vapour deposition (PECVD) and used as a physical mask for the DE process. This oxide layer and the *in situ* SiN are etched by SF_6 plasma in order to define the gate area.

The next step is the DE of the top 10 nm AlGaIn barrier layer. This process is based on an oxidation of the AlGaIn by soft O_2 plasma (RF power—100 W/Pressure—300 mT/2 min) followed by wet etching of the oxide layer using HCl:H $_2$ O (1:10) solution during 1 min [28].

Electrical measurements have been performed as well as atomic force microscopy (AFM) observations on transistor pattern with source–drain distance of 10 μm and 1.5 μm opening in SiO_2 for the gate recess. Figure 3 shows the current measured on this pattern at $V_{DS} = 10$ V versus the DE iteration number. Using the AFM, we have extracted an etch rate of 0.5 nm per DE cycle.

On the plot shown in figure 3, we can observe two main regions. The first region (up to 20 cycles) corresponds to the etching of the top AlGaIn barrier layer. In this region, the current decreases as the DE cycle number is increasing. In the second region (over 20 cycles); where the etching reaches the 2 nm GaN, the current is relatively stabilised. We stopped the DE after 22 cycles corresponding to 50% etching of the 2 nm GaN layer.

We can conclude that the 2 nm GaN layer inserted in the barrier layer is an important element in the epi-structure which is mandatory to:

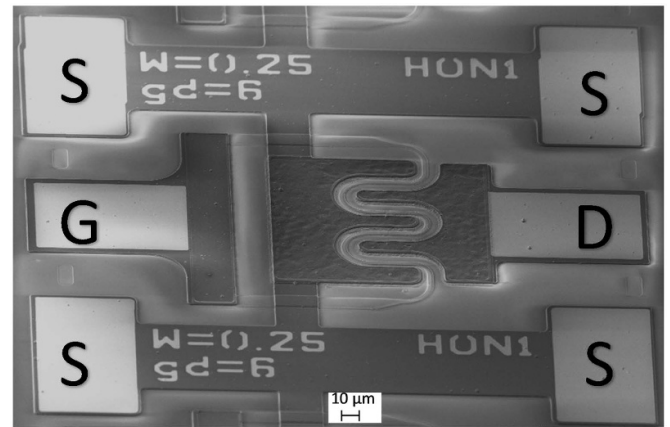


Figure 4. SEM image of an E-mode device.

- Obtain a V_{th} shift towards the positive values. Indeed, when the gate recess reaches the surface of GaN layer, the band diagram is lifted-up, which increases the effective SBH by at least 0.4 eV. Indeed, even if the Ti/GaN SBH is around 0.9, the real effective barrier height is around 1.3 eV (figure 2 red curve) thanks to the GaN/AlGaIn conduction band discontinuity. In other words, our barrier layer GaN/AlGaIn is 6 nm thick, if we have this barrier layer composed only with 6 nm AlGaIn, the pinch-off voltage will be negative because we will lose the benefit of these 2 nm GaN.
- Monitor the recess etching to obtain a well-controlled process. Indeed, when the recess reaches the GaN layer, the drain–source current saturates, and we can stop our recessing. This is an advantage to get a stable, reproducible and robust process.

Therefore, the 2 nm GaN layer is mandatory in the epi-structure and represents a big part of the novelty of this new band gap engineering approach to fabricate a normally-off GaN-HEMT device.

After the gate recess process, the sample is pretreated with a KOH solution, followed by a HCl solution [28]. The gate process is one of the most critical part of the HEMT fabrication process. We decided to use two different process for the gate oxide deposition. On the first sample (sample A), a thin 12 nm SiO_2 gate oxide layer is deposited by PECVD. On a second sample (sample B), a thin 12 nm Al_2O_3 layer is deposited by atomic layer deposition. The HEMT heterostructure is the same on both samples. This step is followed by the gate metallization (Ti/Au/Ni) deposited by E-beam evaporation. Afterwards, a SiO_2 passivation (800 nm) layer is deposited by PECVD followed by a thick interconnexion metal stack Ti/Au/Ni for transistor measurement pad. Figure 4 shows a scanning electron mobility (SEM) image of a fabricated E-mode device. Transmission line measurements reveal a contact resistance R_c of 1.28 Ω mm and a sheet resistance R_{sh} of 788 Ω mm. It is important to notice that no work has been done to optimize the ohmic contact resistance. The main goal of this paper is the demonstration of this new barrier layer engineering approach.

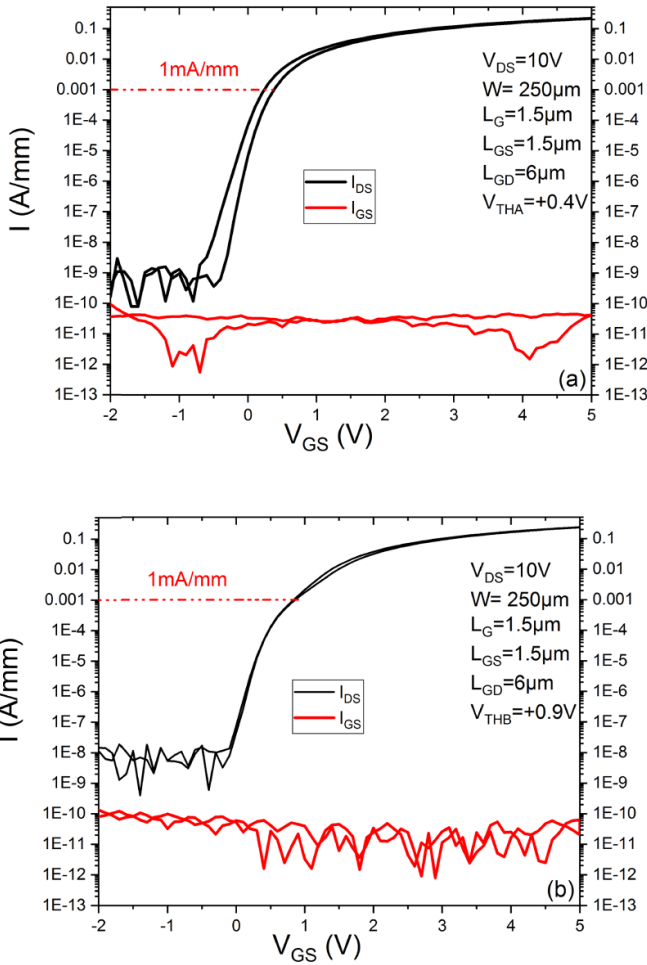


Figure 5. $I_{DS}(V_{GS})$ and $I_{GS}(V_{GS})$ characteristics of the fabricated AlGaIn/GaN HEMT: (a) sample A and (b) sample B.

3. Measurements and results

The AlGaIn/GaN HEMT devices under test (DUT) exhibit the following features: $L_G = 1.5 \mu\text{m}$, $L_{GS} = 1.5 \mu\text{m}$, $L_{GD} = 6 \mu\text{m}$ and $W = 250 \mu\text{m}$. All the electrical characterizations are performed in the dark. The DC $I_{DS}(V_{GS})$ characteristics (figure 5) presents a threshold voltage of +0.4 V (sample A) and +0.9 V (sample B) measured for I_{DS} equal to 1 mA mm^{-1} . These results confirm the normally-off behaviour of the transistor. The DUTs are presenting a maximum drain current of 190 mA mm^{-1} (sample A) and 177 mA mm^{-1} (sample B) at $V_{GS} = +5 \text{ V}$.

To shift the pinch-off voltage towards the positive values the aluminium content of the AlGaIn at the bottom of the barrier layer can be reduced below 20% to decrease the electrons density underneath the gate electrode. At the same time, we should increase the Al content in the top AlGaIn layer to reduce the serial resistance of the device.

In figure 5, we observe that the gate leakage current measured at $V_{DS} = 10 \text{ V}$ is below 200 pA mm^{-1} for both devices. The off-state drain leakage current of approximately 1 nA mm^{-1} and 10 nA mm^{-1} gives an I_{ON}/I_{OFF} ratio around 2×10^8 and 0.17×10^8 for samples A and B respectively.

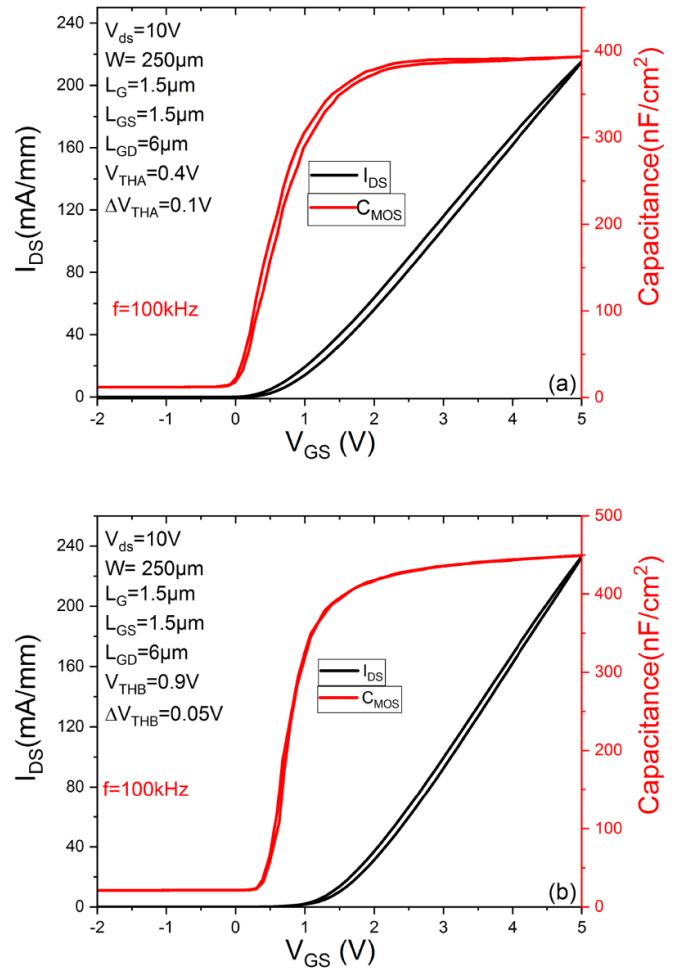


Figure 6. $C(V_{GS})$ measured diode and $I_{DS}(V_{GS})$: (a) sample A and (b) sample B.

The low ΔV_{th} as well as low gate leakage currents measured on samples A and B indicate that there is no significant damage induced by the DE process to the barrier layer surface.

To further validation of this observation, $C(V)$ measurements (figure 6) have been performed at 100 kHz on an oversized diode. A low hysteresis is observable on the $C(V)$ measurements as well. We can state here that the DE minimizes damages induced by the gate recess despite the important number of DE cycles.

A breakdown voltage of 150 V and 200 V at $V_{GS} = 0 \text{ V}$ has been measured on sample A and sample B respectively. An on-state resistance (R_{ON}) of $22 \Omega \text{ mm}$ and $16 \Omega \text{ mm}$ of sample A and sample B respectively are extracted from the DC $I_D(V_{DS})$ characteristics (figure 7).

4. Conclusion

This paper introduces a new band gap engineering approach of the barrier layer of AlGaIn/GaN HEMT heterostructure to fabricate E-mode devices. Thanks to DE process, these devices could be co-integrated with normally-on devices within advanced circuits. The obtained results validate this

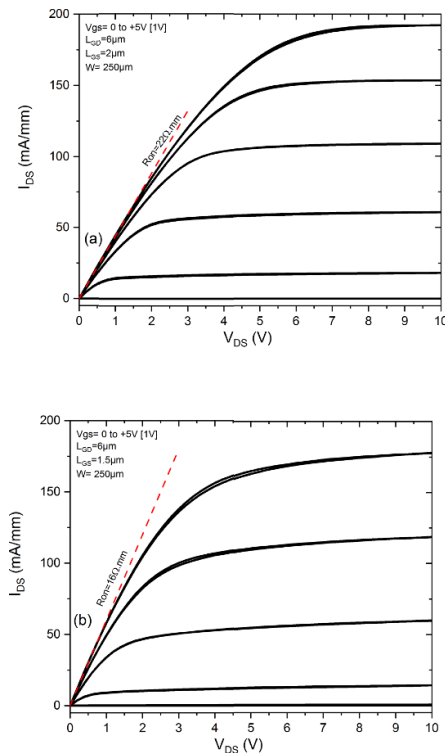


Figure 7. $I_{DS}(V_{DS})$ hysteresis characteristic of the fabricated AlGaIn/GaN HEMT: sample A (a) and sample B (b).

new approach and we have measured a V_{th} over 0 V. The ΔV_{th} of 0.1 V (sample A) and 0.05 V (sample B) and the low gate leakage current prove the low damage induced by the DE process despite the large number of etching cycles. The future work will consist in further decreasing the aluminum content in the bottom AlGaIn barrier layer to reach V_{th} over 1 V.

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References

- [1] Altuntas P *et al* 2015 Power performance at 40 GHz of AlGaIn/GaN high-electron mobility transistors grown by molecular beam epitaxy on Si(111) substrate *IEEE Electron Device Lett.* **36** 303–5
- [2] Mitova R, Ghosh R, Mhaskar U, Klikic D, Wang M-X and Dentella A 2014 Investigations of 600-V GaN HEMT and GaN diode for power converter applications *IEEE Trans. Power Electron.* **29** 2441–52
- [3] Wood J 2018 Compact, portable, and easy to use: a perspective on transistor modeling for gallium nitride high-power amplifier design *IEEE Microw. Mag.* **19** 80–98
- [4] Hassan B *et al* 2019 Large periphery GaN HEMTs modeling using distributed gate resistance *Phys. Status Solidi a* **216** 1800505
- [5] Micovic M *et al* 2005 GaN enhancement/depletion-mode FET logic for mixed signal applications *Electron. Lett.* **41** 1081–3
- [6] Kachi T 2014 GaN power device for automotive applications *2014 Asia-Pacific Microwave Conf. (November 2014)* pp 923–5
- [7] Chu R *et al* 2011 1200-V normally off GaN-on-Si field-effect transistors with low dynamic on-resistance *IEEE Electron Device Lett.* **32** 632–4
- [8] Feng Z H *et al* 2010 18-GHz 3.65-W/mm enhancement-mode AlGaIn/GaN HFET using fluorine plasma ion implantation *IEEE Electron Device Lett.* **31** 1386–8
- [9] Tang Z *et al* 2013 600-V normally off Si_x/AlGaIn/GaN MIS-HEMT with large gate swing and low current collapse *IEEE Electron Device Lett.* **34** 1373–5
- [10] Sun W-W *et al* 2015 Degradation mechanism of enhancement-mode AlGaIn/GaN HEMTs using fluorine ion implantation under the on-state gate overdrive stress *Chin. Phys. B* **24** 017303
- [11] Kurt G *et al* 2019 Investigation of a hybrid approach for normally-off GaN HEMTs using fluorine treatment and recess etch techniques *IEEE J. Electron Devices Soc.* **7** 351–7
- [12] Uemoto Y *et al* 2007 Gate injection transistor (GIT)—a normally-off AlGaIn/GaN power transistor using conductivity modulation *IEEE Trans. Electron Devices* **54** 3393–9
- [13] Hilt O, Knauer A, Brunner F, Bahat-Treidel E and Würfl J 2010 Normally-off AlGaIn/GaN HFET with p-type Ga gate and AlGaIn buffer *2010 22nd Int. Symp. on Power Semiconductor Devices IC's (ISPSD) (June 2010)* pp 347–50
- [14] Higashiwaki M, Mimura T and Matsui T 2007 Enhancement-mode AlN/GaN HFETs using cat-CVD SiN *IEEE Trans. Electron Devices* **54** 1566–70
- [15] Mizutani T, Ito M, Kishimoto S and Nakamura F 2007 AlGaIn/GaN HEMTs with thin InGaIn cap layer for normally off operation *IEEE Electron Device Lett.* **28** 549–51
- [16] Zhong Y *et al* 2019 Effect of thermal cleaning prior to p-GaN gate regrowth for normally off high-electron-mobility transistors *ACS Appl. Mater. Interfaces* **11** 21982–7
- [17] Greco G, Iucolano F and Roccaforte F 2018 Review of technology for normally-off HEMTs with p-GaN gate *Mater. Sci. Semicond. Process.* **78** 96–106
- [18] Hwang I *et al* 2013 p-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current *IEEE Electron Device Lett.* **34** 202–4
- [19] Tang X, Li B, Moghadam H A, Tanner P, Han J and Dimitrijevic S 2018 Mechanism of threshold voltage shift in p-GaN gate AlGaIn/GaN transistors *IEEE Electron Device Lett.* **39** 1145–8
- [20] Ren K, Liang Y C and Huang C-F 2016 Physical mechanism of fin-gate AlGaIn/GaN MIS-HEMT: V_{th} model *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA) (November 2016)* pp 319–23

- [21] Yadav C, Kushwaha P, Khandelwal S, Duarte J P, Chauhan Y S and Hu C 2014 Modeling of GaN-based normally-off FinFET *IEEE Electron Device Lett.* **35** 612–4
- [22] Liu S *et al* 2014 Al₂O₃/AlN/GaN MOS-channel-HEMTs with an AlN interfacial layer *IEEE Electron Device Lett.* **35** 723–5
- [23] Xu Z *et al* 2014 Demonstration of normally-off recess-gated AlGa_{0.5}N/GaN MOSFET using GaN cap layer as recess mask *IEEE Electron Device Lett.* **35** 1197–9
- [24] Kuzmik J *et al* 2010 Proposal and performance analysis of normally off n++ GaN/InAlN/AlN/GaN HEMTs with 1-nm-thick InAlN barrier *IEEE Trans. Electron Devices* **57** 2144–54
- [25] Hua M *et al* 2017 Normally-off LPCVD-SiN_x/GaN MIS-FET with crystalline oxidation interlayer *IEEE Electron Device Lett.* **38** 929–32
- [26] Hahn H, Lükens G, Ketteniss N, Kalisch H and Vescan A 2011 Recessed-gate enhancement-mode AlGa_{0.5}N/GaN heterostructure field-effect transistors on Si with record DC performance *Appl. Phys. Express* **4** 114102
- [27] Wang Y *et al* 2013 High-performance normally-off Al₂O₃/GaN MOSFET using a wet etching-based gate recess technique *IEEE Electron Device Lett.* **34** 1370–2
- [28] Chakroun A, Jaouad A, Bouchilaoun M, Arenas O, Soltani A and Maher H 2017 Normally-off AlGa_{0.5}N/GaN MOS-HEMT using ultra-thin Al_{0.45}Ga_{0.55}N barrier layer *Phys. Status Solidi a* **214** n/a–n/a