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Characterization and modeling of 650V GaN diodes for high frequency power conversion

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Abstract— The constant growth of electric consumption leads to considerable progress in power conversion. Recent studies have shown that using Gallium Nitride (GaN) as a technological building bloc permits to develop converter operating at high frequency with reduced volume and weight. Furthermore, it is conceivable the monolithic co-integration of devices towards full-GaN switching cells. Therefore, characterization of GaN power devices is needed to provide accurate models in a wide frequency band in order to design new generations of converters. An innovative modeling method for GaN High Electron Mobility Transistor (HEMT) power transistors based on the use of Scattering parameters (S-parameters) and small-signal equivalent circuit was recently developed and validated in previous studies. Meanwhile, the demand concerning GaN diodes increases, pushing forward the need for dedicated electric model. Through S-parameters, current-voltage and current-collapse measurements, this paper presents the characterization of packaged GaN diodes with the aim to establish an accurate nonlinear model. The analyzed devices are still in the development phase, but initial results are very promising and get close to commercial SiC diodes available on the market.

Keywords— gallium nitride (GaN), diode, power converter, characterization, s-parameters, model

I. INTRODUCTION

Because of a constant research for increasing energy conversion, new generation power converters are yet designed [1]. In this context, fast developments on power switching devices were performed using wide-bandgap (WBG) materials such as silicon carbide (SiC) and gallium nitride (GaN) [2], [3]. GaN arouses a great interest in power electronics permitting to significantly outperforms power devices based on silicium (Si). Because of high breakdown voltage, fast switching speed, high thermal conductivity, and low on-resistance, it is foreseen as the next generation of power semiconductor dedicated to power electronics [4]. Its ability to switch at high frequency may lead to significant reduction the size and weight of power converters. However,

accurate models of such components need to be established with the aim of simulating their behavior in power converters and thus predict possible energy losses and efficiency in a wide frequency band. Accurate models are necessary as the GaN technology still suffers from a degradation of its dynamic On-resistance (R_{ON}) due to trapping phenomena.

Different modeling methods can be used for the electric analysis of power devices. Since physics-based models use semiconductor physics to accurately describe the components, behavioral-based models enable the fitting of the electrical behavior but lack of flexibility and control from the technological parameters. In this paper, an approach based on small-signal equivalent circuit is chosen, since it becomes possible to get useful electrical data and enables technological feedback. This method is applied on different new GaN power diodes (650V / 6A – 650V / 15A) in TOP3 packages. Although these latter are not commercialized yet, GaN diodes are currently studied in the frame of a collaboration with STMICROELECTRONICS, a European foundry which gave us the opportunity to characterize and analyze their devices. Thus, dedicated electrical analysis and subsequent modeling could provide useful information to consider GaN diode/GaN HEMT monolithic integration.

The different steps to characterize GaN power diodes up to 1GHz are described in this paper. The first section presents the calibration method in order to de-embed the parasitic elements due to the transmission lines enabling the access of the devices under test (DUT). Then, a linear model derived from radiofrequency (RF) techniques is described in the section 2 and the method is extended for different operating point from 1.5V (on-state) to 600V (off-state). In addition, the nonlinear behavior of these diodes is studied, and a first model is shown in the last section, including a first insight on dynamic R_{ON} consideration.

II. S-PARAMETERS CALIBRATION & STANDARDS

Although S-parameters measurements can be carried out at any frequency, this technique is more often used for devices operating at radio and microwave frequency range. However, it has shown its interest in power electronics to establish accurate models for frequencies ranging from megahertz up to gigahertz, being able to consider harmonics effects stemming from the fast commutation. Modeling methods based on S-parameters were recently developed. In this frame, GaN HEMT power transistors and/or SiC power MOSFET were fully characterized through S-parameters measurements enabling the extraction of small-signal equivalent circuits [5], [6]. Using, the Rhode & Schwartz ZVA8 Vectorial Network Analyzer (VNA) for the characterization, coaxial connections are required, and specific characterization boards and standards are needed to get the most accurate calibration. Following the procedure described in the paper [7], in-house circuits (open line – short line – devices footprint) were designed and developed on Printed Circuit Board (PCB) well suited for VNA measurements (50Ω).

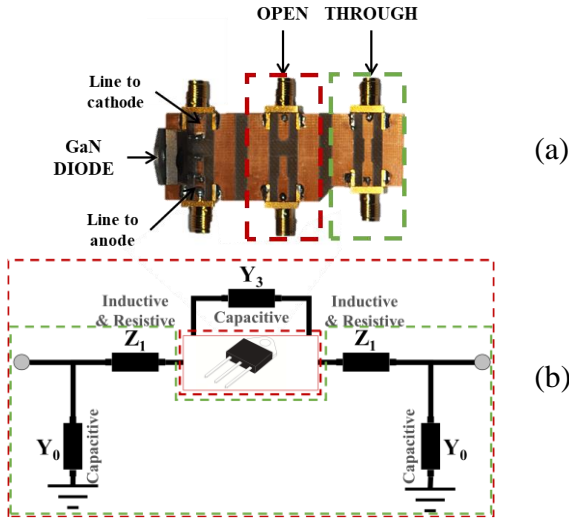


Fig. 2. (a) Characterization board for the GaN diodes & their calibration standards (b) Equivalent circuit of characterization

Fig. 1 (a) shows the circuits used in order to de-embed parasitic elements and focus on the DUT intrinsic characteristic. In Fig. 1 (b) the capacitive parameter Y_0 stands for the admittance between transmission lines and ground plane, whereas Z_1 , mainly inductive and resistive, features the complex impedance of the access lines. In order to characterize the DUT and remove the influence of the characterization board on measurement, a de-embedding procedure must be applied.

For this aim, different techniques can be used based-on either 1-port reflective technique or 2-port series-through technique and 2-port shunt-through technique according to the impedance to analyze. Regarding our setup, series-through technique is chosen for practical and accuracy reason [8].

III. LINEAR MODEL

After de-embedding the access parasitic elements thanks using the standard patterns (open/short), the diode can be modeled through its electrical equivalent circuit including the parasitic elements (package capacitances – pin inductance). In fig. 2(a), R_{AC} accounts for the cathode resistance –mainly

through the ohmic contact and the sheet resistance of the 2-dimension electron gas (2DEG)-, C_P is the intrinsic diode

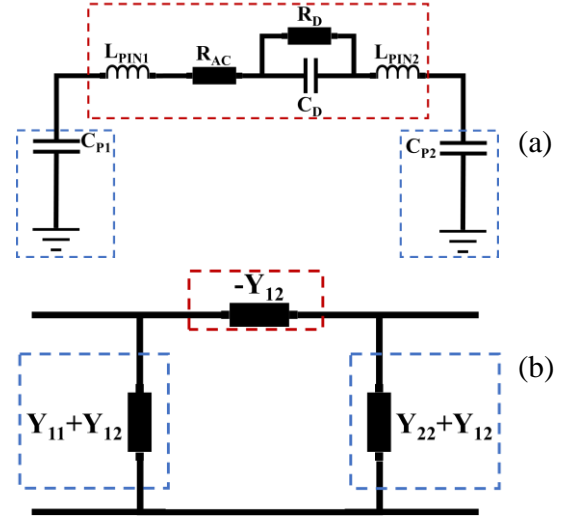


Fig. 1. (a) Diode equivalent circuit linear model (b) Y-equivalent circuit for reciprocal two-port network

capacitance arising from the depletion region, and R_D is the associated dynamic resistance.

It may be noticed that $C_{P1,2}$ and $L_{PIN1,2}$ refer mainly to the parasitic inductive and capacitive contribution of the TOP3 package. Working with S-parameters provides the opportunity to extract the values of each elements by analytic calculations.

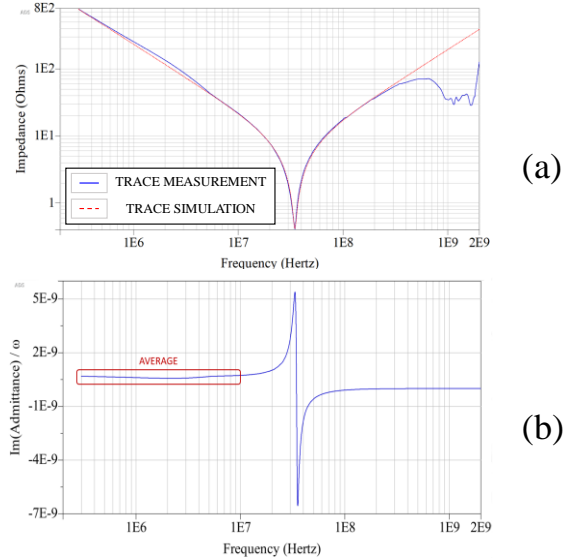


Fig. 3. (a) Impedance magnitude versus frequency (b) Imaginary part of the admittance versus frequency

The modeling method is applied at a fixed anode to cathode voltage $V_{AK}=0V$. As presented in fig. 3, S-parameters are converted to impedance or admittance [9] using Advanced Design System (ADS) software and plotted versus the frequency. As observed in Fig. 3(a), the resonance frequency can be easily identified. At $V_{AK}=0V$, the RF signal mainly flows through the access resistance R_{AC} (since the capacitance is almost short-circuited due to its high value) and corresponds to the impedance at the resonance. In turn, the intrinsic capacitance C_D is evaluated thanks to the impedance behavior before resonance (where the circuit is mainly capacitive), and the pin inductances $L_{PIN1,2}$ are deduced from the value of the resonance frequency ($F_0 = 17.6MHz$ for the GaN diode 6A – $F_0=34MHz$ for the GaN diode 15A). Finally, the dynamic

resistance R_D is obtained thanks to an optimization procedure to fit the measurements (Fig.3(a)).

TABLE I. EXTRACTED VALUES OBTAINED FOR THE DIFFERENT DIODES AT $V_{AK}=0V$

Diodes characteristics	Extracted values at $V_{AK}=0V$			
	C_D (nF)	L_{PIN} (nH)	R_{AC} (m Ω)	R_D (k Ω)
GaN diode – 650V – 15A – TOP3	2.73	15	138	3.78
GaN diode – 650V – 6A – TOP3	0.66	16.6	341	4.2
SiC STPSC8H065B – 650V – 8A – CMS	0.46	2.52	130	7.78

This procedure was applied to different GaN diodes and the results show that L_{PIN} remains similar for different voltage ranges since the package does not differ from one device to another. In table 1, it must be noticed that the scaling laws seem in accordance with the diode's layouts and characteristics. Furthermore, the results also obtained on SiC diodes are in agreement with the manufacturer's data, confirming the validation of our approach and the results obtained on the new GaN devices.

Then, the overall procedure can be applied for different working points from 1.5 to -600V thanks to an in-house bias tee made on printed circuit board, operating between 1MHz to 1GHz and withstanding 600V_{DC} and 10A [7]. The bias tee is required to bias our diodes without affecting the RF signal (50 Ω matched). The same process was applied for both GaN diodes with consistent results. However, the next section focuses the results obtained on the 6A diodes

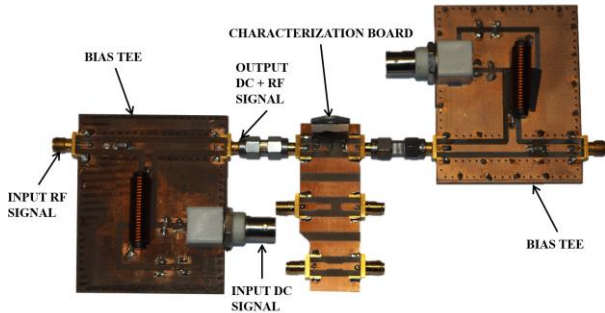


Fig. 4. Polarization setup using bias tees for DUT characterization

IV. NON-LINEAR MODEL

Biasing our diodes at different working point is necessary in order to analyze the behavior of each elements according to the voltage. As an example, Fig. 5 shows the evolution of L_{PIN} versus the reverse voltage up to 600V.

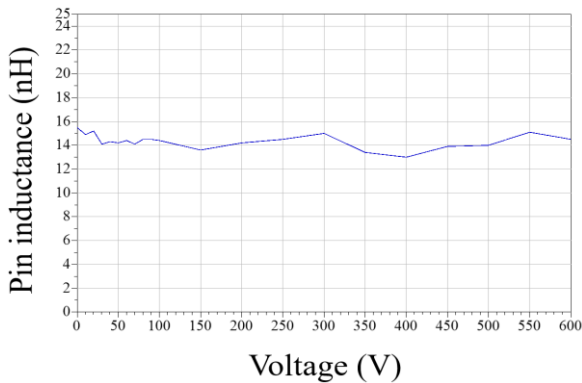


Fig. 5. Evolution of L_{PIN} versus V_{KA}

Using the presented method, it is verified that the extracted pin inductance remains almost constant (15nH) all over the voltage range.

However intrinsic elements vary according to the voltage reinforcing the interest of building a nonlinear model. Thus, in order to obtain reliable simulations, it is necessary to model the junction capacitance, the dynamic on-resistance and consider the effects of traps which still affect the ideal behavior of the diodes, remaining a blocking point in the performances of GaN devices. Fig. 6 illustrate the equivalent circuit of the proposed nonlinear model.

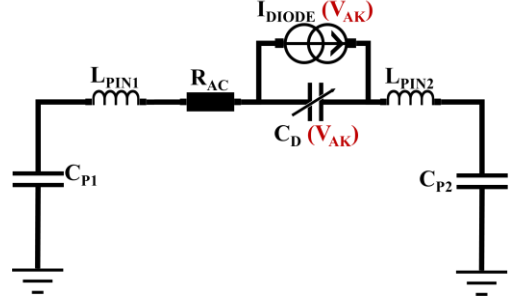


Fig. 6. Diode equivalent circuit non linear model

A. Junction capacitance modeling

In order to establish a complete model of the GaN diode, the extraction of the capacitance over the entire bias range must be performed. Fig. 7 shows its evolution versus the applied voltage. In order to validate the result obtained with the S-parameters, capacitance-voltage measurements were also carried out using an Agilent 4294A Precision impedance Analyzer associated with the B1505A Keysight setup. It is shown that the intrinsic capacitance extracted with the S-parameters method behaves in agreement with the capacitance obtained through the standard method: this validates again the method and the algorithms used during the de-embedding process.

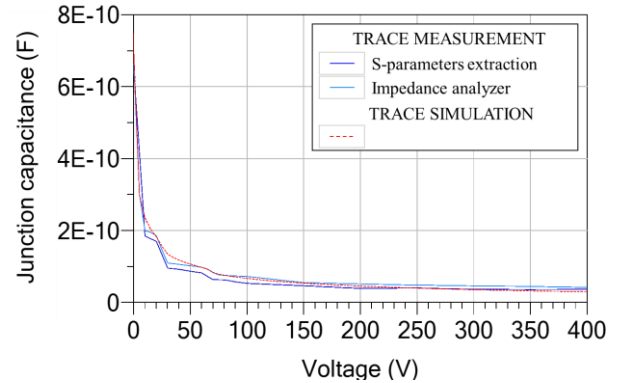


Fig. 7. Junction capacitance measurement & simulation

The capacitance behavior is fitted using the formula (1) where C_{j0} is the zero-bias junction capacitance, ϕ_{bi} is the built-in potential and γ is a function of the doping profile [10], [11]. C_{f1} , C_{f2} are introduced to model the effect of the field plates.

$$C_D = \frac{C_{j0}}{\left(1 - \frac{V_j}{\phi_{bi}}\right)^\gamma} + C_{f1} + C_{f2} \quad (1)$$

$$C_{f1} = A_1 \tan^{-1}\left(\frac{V_j + V_{f1}}{B_1}\right); \quad C_{f2} = A_2 \tan^{-1}\left(\frac{V_j + V_{f2}}{B_2}\right) \quad (2)$$

A good agreement is shown between the simulation and the measurement for the values listed in table 2.

TABLE III. FITTING VALUES OBTAINED FOR THE CAPACITANCE MODEL

GaN diode – 650V – 6A								
C_{j0} (nF)	ϕ_{bi} (eV)	γ	A_1 (F)	A_2 (F)	V_{F1} (V)	V_{F2} (V)	B_1 (V)	B_2 (V)
0.69	0.6	0.4	8.10^{-12}	4.10^{-12}	25	68	1	2.7

B. Current generator modeling

To complete the nonlinear model, the I-V characteristics of the diodes were measured thanks to the Keysight B1505A setup in pulse configuration, with a 100 μ s pulse width and a 100ms period. The same process was applied for different ambient temperature (25°C to 125°C) by placing the GaN diode directly on a heating brass chuck. Fig. 7 shows the measurement results where it is exposed that the value of the access resistance increases, which is a typical phenomenon affecting unipolar devices. Indeed, increasing the temperature leads to a significant decrease of the electron mobility [12].

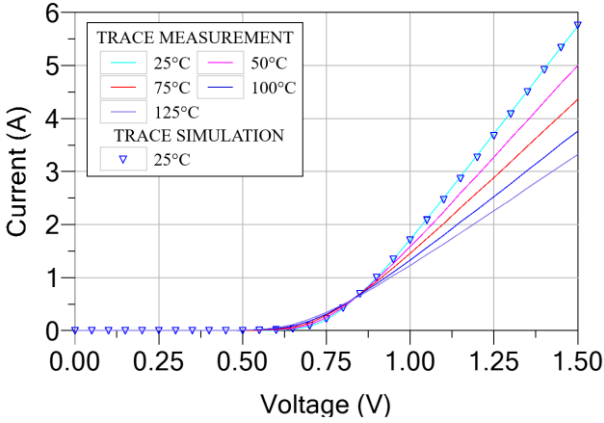


Fig. 8. Current-voltage measurements & simulation

The equation (3) considering only the thermal emission of electrons over the is used to fit our measurement for different temperature.

$$I_d = i_s \left(e^{\frac{V_{Dq}\phi_b}{\eta kT}} - 1 \right) \quad (3)$$

$$i_s = AT^2 Se^{-\frac{q\phi_b}{kT}} \quad (4)$$

In this model, i_s stands for the saturation current given by (4) with A the effective Richardson constant, S the device area, q the electron charge, ϕ_b the built-in potential and k the Boltzmann's constant, η the ideality factor and T the temperature [13], [14].

Once again, a good agreement is observed between measurement and simulation with the values presented in table 3. An increase of 70% of the initial value of R_{AC} has been highlighted constated at 125°C. The built-in potential and the ideality factor seem constant. It should be highlighted that the ideality factor η remains close to unity, indicating a very good behavior of the Schottky contact and a reduced active traps density beneath the anode. Both nonlinear parts C_D and I_d were implemented within ADS to describe the overall GaN diode behavior.

TABLE II. VALUES OBTAINED AFTER FITTING I-V CHARACTERISTIC FOR DIFFERENT TEMPERATURE

Applied temperature	GaN diode – 650V – 6A		
	R_{AC} (m Ω)	ϕ_{bi} (eV)	η
25°C	113.7	0.84	1.78
50°C	130.4	0.80	1.25
75°C	149.5	0.77	1.34
100°C	169.4	0.72	1.52
125°C	194.3	0.75	1.56

C. Current collapse modeling

Although promising, GaN power devices can suffer of degradation of the dynamic ON-resistance due to trapping effect after switching high voltage OFF-state stress [12]. It is therefore fundamental to study and model this defect. As shown in Fig. 9, the behavior of the GaN power diode differs according to the stress condition. On this specific device, different stress from 0V (no stress) to -500V, have been implemented during 0.5s OFF-state to 900 μ s ON-state. In this section, a first trapping model for a turn-on from -100 to 0.8V is so proposed.

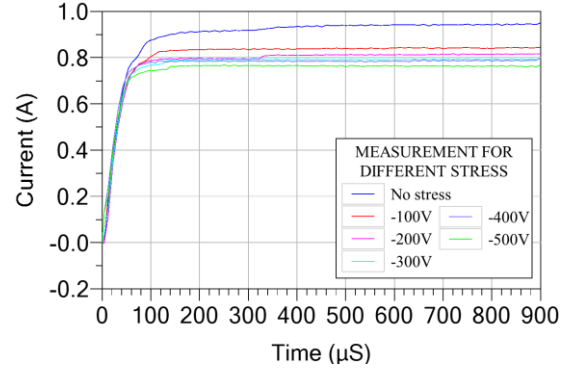


Fig. 10. Current-collapse measurements after different stresses

Authors proposed in [15] a current collapse model based on the RC circuit network for GaN HEMT. This RC network is used in order to model electron capture and emission effects. In Fig. 10, the dynamic R_{ON} degradation can be modeled by adjusting the values of the RC network. A traps current generator is added into the intrinsic diode model and thereby, permits to establish a complete behavioral model considering the current collapse effect.

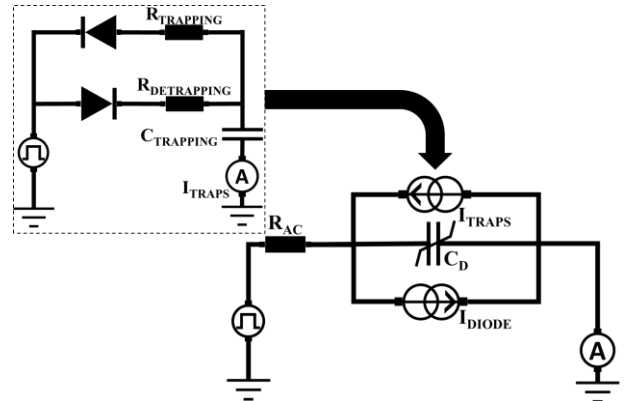


Fig. 9. Proposal trap sub-circuit

Fig. 11 shows the current-collapse measurements using the B1505A set up; different stresses are applied for 0.5s before

a turn-on switching. By adjusting the elements of the RC network ($R_{TRAPPING}$, $C_{TRAPPING}$) and the access resistance it is possible to describe the current collapse consecutive to the applied reverse voltage. In order to better fit the measurement, it may be interesting to optimize the model by adding other RC networks. Table 4 shows the values for the different stresses.

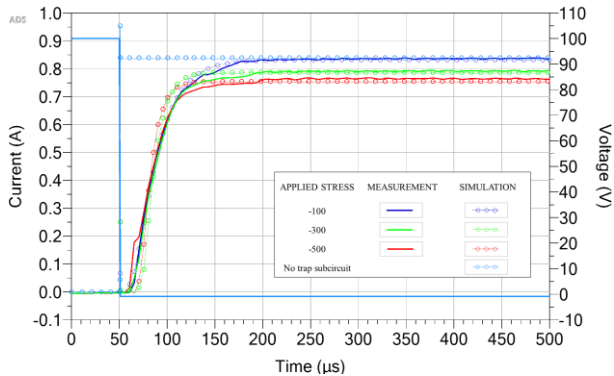


Fig. 11. Current-collapse analysis & modeling for different stresses

TABLE IV. VALUES OF RC NETWORK FOR MODELING CURRENT-COLLAPSE

GaN diode – 650V – 6A			
Applied Stress	$R_{TRAPPING}$ (k Ω)	$C_{TRAPPING}$ (nF)	R_{AC} (m Ω)
100	0.98	22	114
300	0.9	12.3	123.8
500	1	10.8	131.4

V. CONCLUSION

In this paper, for the first time, GaN packaged power diodes manufactured by STMicroelectronics have been characterized. This first measurement campaign enabled to extract accurately all the parasitic and intrinsic elements of the GaN devices. The validation of the linear method was confirmed through additional measurements carried out on commercial SiC diodes, and comparison with manufacturers data. Intrinsic elements values of the diodes indicate good performances in terms of stocking charge (through the reduced value of C_D) and relatively low access resistance and make it possible an attractive future monolithic co-integration with normally off GaN HEMTs. The different elements of the nonlinear model show good agreement to the measurements. Innovative methods are proposed in this paper, it allows to adjust the GaN diode model and thus make the simulations as accurate as possible. Still under development, these innovative diodes must be modeled to understand their behavior and thus give a technological feedback. For this reason, studies on considering the dynamic ON-resistance must be conducted to model even more precisely the mechanisms of entrapment. In the field of power electronics, development of GaN diodes is a crucial step for new generation converters, and specifically for medium power applications switching at high frequencies.

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