Improved Open-Circuit Voltage of Sb2Se3 Thin-Film Solar Cells Via Interfacial Sulfur Diffusion-Induced Gradient Bandgap Engineering

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Abstract: The performance of thermally deposited Sb_2Se_3 solar cells are severely limited by various bulk and interfacial recombination, instigating large open-circuit voltage (V_{OC}) deficit. Ternary $Sb_2(S,Se)_3$ is considered as a remedy, however, it is also subjected to a dilemma that improvement in V_{OC} will be escorted by J_{SC} loss due to the shrinkage of light harvest. Thus, a gradient of S/Se across the film is prerequisite to avoid this detrimental compromise. Herein, we explored the incorporation of S in Sb_2Se_3 absorber layer evaporated from CdS buffer layer during vapor transport deposition (VTD) process, and its further self-activated diffusion at interface upon ambient storage. For the gradient ITO/CdS/$Sb_2(S,Se)_3$/Sb_2Se_3/Au solar cell, the large bandgap $Sb_2(S,Se)_3$ at heterojunction side contributes to high V_{OC}, while the narrow

bandgap Sb_2Se_3 at top side confirms high J_{SC}. Sulfur diffusion at CdS/Sb_2Se_3 interface also improves the junction quality with an enlarged V_{bi}, reduced interfacial defects and recombination loss, thus improving V_{OC} from 393 to 430 mV. Such V_{OC} represents the highest value for that of thermally deposited Sb_2Se_3 solar cells. The champion device also delivers an interesting efficiency of 7.49%. This research provides substantial guidance in exploring efficient approaches to improve the performance of Sb_2Se_3 solar cells.

1. Introduction

To tackle the issues associated with the energy crisis and environmental pollution, green renewable energy, particularly solar energy, has dragged more attention since the discovery of photovoltaic effect. Though the currently available photovoltaic technologies are grooming persistently, researchers are still making their efforts to discover more desirable materials. Cadmium telluride (CdTe), copper indium gallium selenide (CIGS), and organic-inorganic metal halide perovskites-based state-of-the-art devices have achieved remarkably certified power conversion efficiencies (PCEs) exceeding 22% at laboratory scales [1], thus dictating the high-potential photovoltaic research scenarios. However, the high toxicity of Cd and Pb, and the scarcity of In and Ga, prompting researchers to further explore some alternative candidates. In this perspective, copper zinc tin sulfide/selenide (CZTS/Se) [2,3], copper antimony sulfide/selenide ($CuSbS_2$/Se_2) [4,5], antimony sulfide/selenide (Sb_2S_3/Se_3) [6,7], aroused in response to the aforementioned anxieties, neither scarce nor toxic, are getting growing concerns.

Among all inorganic chalcogenides, Sb_2Se_3 has received more courtesy for its excellent material characteristics and optoelectronic properties, the low-cost, low-toxicity and earth-abundant nature, accompanied with an appropriate optical band gap (~1.2 eV), strong light absorption coefficient ($>10^{-5}$ cm^{-1}), and good carrier mobility (~10 cm^2 V^{-1} s^{-1}) [8-10]. Since the first observation of chemically deposited Sb_2Se_3 thin film in photoelectrochemical cell

delivered a PCE of 0.66% [11], Choi *et al.* activated the booming development of mesoporous sensitized Sb_2Se_3 solar cell with an efficiency of 3.21% in 2014 [12]. Later on, various thin film preparation techniques for Sb_2Se_3 have been explored, gratifying efficiencies for planar Sb_2Se_3 solar cells have been attained. For instances, magnetron sputtering, rapid thermal evaporation (RTE), close spaced sublimation (CSS), vapor transport deposition (VTD), have reached their efficiencies to 6.84% [13], 7.62% [14], 9.2% [15] and 7.6% [16], respectively.

Although Sb_2Se_3 solar cells are about to achieve a benchmark efficiency of 10%, the V_{OC} revealed slow growth in contrast to the quickly developing PCE. For light absorbing semiconductor with a bandgap (Eg) ranging from 1.0 to 1.7 eV, the minimum V_{OC} deficit (defined as Eg/q-V_{OC}) can be less than 0.28 V according to the balance principle [17]. While in case of Sb_2Se_3 planar structure with the highest PCE (9.2%), it is more than 0.70 V [15]. Such a severe V_{OC} deficit can be attributed to the complicated deep defects, the short carrier lifetime, the unexpected surface/interface recombination and space-charge region (SCR) recombination [18]. To cope such issues, various strategies have been attempted, such as absorber engineering of post-selenization [19], *in-situ* sulfurization [20], co-evaporation of Sb_2Se_3/Se [21], and external doping [22], interfaces engineering of optimizing band alignment through single/double buffer layer modification [23,24], introducing hole transport layers like PbS quantum dots [25], Spiro-OMeTAD [26] and CZ-TA [27].

Currently, the results are still unsatisfactory, especially compared to the analogous $Sb_2(S,Se)_3$ solar cell with a champion 10% efficiency [28]. This ternary composition offers to enhance the J_{SC} or V_{OC} by varying Se/S-content in the $Sb_2(S,Se)_3$ film, nevertheless, a predicament that the improvement in the V_{OC} will be escorted by J_{SC} loss due to bandgap upsurge is also unavoidable. Thus, a gradient of Se/S across the film can be a prerequisite to avoid such detrimental compromise between J_{SC} and V_{OC}. Chen *et al.* reported a diffusion-controlled selenium-graded $Sb_2(S_{1-x}Se_x)_3$ with enhanced J_{SC} and a V_{OC} comparable to wide bandgap

Sb_2S_3 solar cell [29]. Tang *et al.* also demonstrated a V-shaped distributional bandgap in $Sb_2(S,Se)_3$ solar cell with synergetic increase of J_{SC} and V_{OC}. [30]. Moreover, the S diffusion from the CdS buffer layer have been witnessed to induce S-rich $CdTe_{1-x}S_x$ region near the CdTe/CdS interface, such inter-diffusion also enhanced device efficiency by reducing the interfacial lattice mismatch and detrimental defects [31,32]. Likewise, a post-annealing treatment induced S diffusion has been observed in CdS/CIGS interface with an increase in bandgap on the CIGS surface and PCE of the device [33]. These results triggered our senses to consider a similar S diffusion from CdS layer into Sb_2Se_3 film at the heterojunction interface, establishing a gradient bandgap structure of CdS/$Sb_2(S,Se)_3$/Sb_2Se_3. The junction between large bandgap $Sb_2(S,Se)_3$ and CdS would generate high V_{OC}, while a narrow bandgap of pure Sb_2Se_3 on the rear side enables sufficient light-harvesting for high J_{SC}, leading to boost the overall solar cell performance.

In this work, we fabricated ITO/CdS/Sb_2Se_3/Au thin film solar cell using VTD method for Sb_2Se_3 deposition. First, we optimized the deposition condition to obtain highly crystalline, compact, and large-grained Sb_2Se_3 film close to its ideal stoichiometric ratio. Afterwards, we explored the incorporation of S atoms in Sb_2Se_3 film evaporated from the CdS layer during VTD process. Upon ambient air storage, the S atoms further diffused at CdS/Sb_2Se_3 interface, leading to a self-activated formation of gradient bandgap of Sb_2Se_3. Accordingly, ITO/CdS/$Sb_2(S,Se)_3$/Sb_2Se_3/Au device structure was achieved. The film with a large bandgap ($Sb_2(S,Se)_3$) forms a junction with CdS at the interface to generate a high V_{OC}. While on the rear side of the solar cell, Se-rich/pure Sb_2Se_3 owing to its narrower bandgap, enables the improved light-harvesting for high J_{SC}. S diffusion from CdS at heterojunction interface also overhauled the junction quality by suppressing interfacial and bulk defects. Consequently, obvious progress in V_{OC} from 393 mV to 430 mV was achieved, resulting in an improvement of PCE from 6.83% to 7.49%.

2. Results and Discussion

The VTD method has gained more attention among nonchemical deposition strategies as it offers a more convenient way to separately control the source and substrate temperature [16,34]. Herein, a VTD processed photovoltaic device preparation is depicted in Figure 1. The morphology, thickness, and orientation of the films are conjointly dependent on the deposition temperature. Thus, we firstly optimized the deposition conditions to obtain a compact and highly crystalline film. The XRD patterns of Sb_2Se_3 films prepared at different deposition temperatures are presented in Figure 2a. All the peaks can be assigned to the orthorhombic phase of Sb_2Se_3, which belongs to the space group of Pbnm (JCPDS No. 15-0861). No obvious (hk0) diffraction peaks were found, suggesting the preferred orientation along c-axis direction. Moreover, the intensity of the preferred vertical (hk1) orientation was enhanced by increasing deposition temperature from 510 °C to 540 °C. The texture coefficient (TC) of the major (221) peak has been investigated to quantitatively study the orientation preference along this specific direction. The numerical TC values can be calculated based on the following equation [19]:

$$TC_{hkl} = \frac{\frac{I(hkl)}{I_0(hkl)}}{\left(\frac{1}{N}\sum_1^n \frac{I(h_i k_i l_i)}{I_0(h_i k_i l_i)}\right)} \quad (1)$$

where I(hkl) is the measured diffraction peak intensities of (hkl) planes and I_0(hkl) is the diffraction peak intensities from the standard XRD pattern. Temperature-dependent TC values are depicted in Figure 2b. The film prepared at 540 °C exhibited the highest TC value, which is highly beneficial for enhancing photo-generated carriers transport and reducing the grain boundary recombination loss [35]. SEM images of the as-prepared Sb_2Se_3 films show compact and granular nature (Figure 2c-g), the average grain size also increased from approximately 150 nm to 400 nm with the gradual increase of deposition temperature (Figure 2b).

The prepared films were utilized to construct a solar cell with planar superstrate configuration

of ITO/CdS/Sb_2Se_3/Au, and the photovoltaic performances were systematically measured. All the devices exhibited a gradual increase in the V_{OC} and J_{SC}, as shown in Figure 3a. The boost in J_{SC} can be attributed to temperature-induced crystallinity improvement, grain growth, orientation optimization and composition stoichiometry of the Sb_2Se_3 absorber layer. A slight increase in V_{OC} was possibly related to the gradient band structure of the deposited film at high temperatures during the VTD process. As for the VTD process, it has been reported that at an elevated temperature, Cd-S bonds will break, and S will leave the surface of the substrate due to its relatively high vapor pressure nature [36,37]. Thus, the vaporized S will combine with the VTD processed Sb_2Se_3 vapors to re-deposit on the substrate. For a fixed duration of evaporation, the amount of Sb_2Se_3 vapors to be transported on the substrate directly depend on the deposition temperature. At a lower evaporation temperature, the thickness of the deposited Sb_2Se_3 film would be low, and the presence of S atoms in the film would be quite obvious. In this case, the deposited film would probably be an alloy ($Sb_2(S_xS_{1-x})_3$) with a certain amount of S, as determined by SEM-coupled EDS analysis (Table 1). High deposition temperature with a slightly quick temperature rise rate was expected to reduce the S evaporation and bury it deep at the interface, forming $Sb_2(S,Se)_3$/CdS internal heterojunction, and covered by an outer layer of Se-rich/pure Sb_2Se_3 film with a narrower bandgap to harvest a wider light spectrum.

To further investigate the effect of S diffusion on device performance, all the devices were stored at room temperature in a transparent plastic box in ambient air, and the performance were checked from time to time till 24 days. Interestingly, the PCEs of all the devices gradually improved up to 6 days and then saturated, as depicted in Figure 3b. The optimal device deposited at 540 °C with highest initial PCE was chosen as the subject for further study. The results associated with the fresh (day zero) film and the corresponding device are labeled as D0, and the stored one (for six days) as D6. The storing time-dependent *J-V* curves

are illustrated in Figure 4a, drawn under the simulated AM 1.5 G solar irradiation. A J_{SC} of 28.75 mA/cm^2, V_{OC} of 393 mV, and FF of 60.51%, contributing a PCE of 6.83% for D0. In contrast, obviously increased to 7.49% of PCE was observed for D6, presenting a J_{SC}, V_{OC}, and FF of 28.22 mA/cm^2, 430 mV, and 61.71%, respectively. The statistical distribution of the key performance parameters belonging to a batch of fifteen devices are also depicted in Figure S1 (Supporting Information). The results confirmed the higher V_{OC} and PCE for most of the devices stored for six days. Furthermore, the forward and reversed biased scanned *J-V* curves of the champion D6 device could perfectly overlap, thus reflecting no observable hysteresis loss under its high-quality absorber layer and superior heterojunction interface (Figure S2, supporting Information). As shown in Figure 4b, V_{OC} and FF revealed a synchronous positive variation upon storing time, while the variation trends of J_{SC} was inversed. Therefore, PCE as a product of $V_{OC} \times J_{SC} \times FF$ can be improved by controlling composition at the interface so as to control the trade-offs between V_{OC} and J_{SC}. It is also worth noting that the V_{OC} could improve a lot while the J_{SC} slightly reduce upon storing the device. Such phenomenon has also been witnessed in our previous work as the selenium was partly replaced by sulfur in $Sb_2(Se_xS_{1-x})_3$ thin film [38]. Thus, we assumed that the S might further diffused into Sb_2Se_3 film at the interface, forming a comparatively larger bandgap $Sb_2(S,Se)_3$ thin layer to boost the V_{OC}. While a nearly non-fluctuated J_{SC} can be attributed to the Se-rich/pure Sb_2Se_3 outer part of the absorber layer. To vindicate our assumptions, different points of surface and cross-sections of the film were tested via EDS (Figure S3 and S4, Supporting Information), and the obtained compositional ratios are listed in Table 2. For D0, the surface contained 0.09 at.% S atoms and D6 had 0.13%. While near the CdS/Sb_2Se_3 interface, the cross-sectional composition of D0 and D6 contained remarkable 2.12% and 4.5% S atoms, respectively. The EQE spectra and the integrated J_{SC} for D0 and D6 devices are also presented in Figure 4c. Integrated J_{SC} calculated from EQE data were 27.1 mA/cm^2 and 27.0 mA/cm^2 for D0 and D6, respectively, which was close to the J_{SC} obtained from the *J-V*

curves. No discernible difference can be observed for those two EQE results, a small blue shift in long-wavelength region for D6 was consistent with the band edge shift according to the transmittance spectra (inset in Figure 4d), confirming a slight increase in the bandgap of Sb_2Se_3 film upon storage due to S diffusion, as presented in Figure 4d. According to the SEM images, the surface and cross-section morphologies of D0 and D6 show no obvious variation (Figure S5a and b, Supporting Information). Likewise, XRD patterns of the D0 and D6 Sb_2Se_3 films also remained unaffected (Figure S5c, Supporting information). Consequently, the extraordinary improvement in device performance, especially in the V_{OC} upon ambient air storage, and the overall consideration for the aforementioned results provoked us to turn our attention to the junction quality and defects presence inside the device.

By comparing the device parameters, the boost in efficiency can be mainly attributed to V_{OC} gain upon ambient air storage. While the V_{OC} is strongly dependent on the diode ideality factor (A) and reverse saturation current (J_0) according to Equation (2) [39]:

$$V_{OC} = \frac{AkT}{q} \ln\left(\frac{Jsc}{J_0} + 1\right) \tag{2}$$

Hence, we calculated J_0 and A along with the shunt conductance (G) and series resistance (R_S) to sightsee the mechanism of the heightened performance of D6. The junction-dependent electrical behaviors of D0 and D6 devices were explored comprehensively by treating the dark J-V characteristic curves in Figure 5a with noticeable rectifying characteristics using Equation (3) [40]:

$$J = J_0 exp\left[\frac{q}{AkT}\ (V - JR)\right] + GV - J_L \tag{3}$$

The values of shunt conductance G were extracted from the flat portions of plot dJ/dV against V (Figure 5b). The obtained G values for D0 and D6 were 6.70 and 5.23 mS/cm^2, respectively. Afterwards, by extrapolating the plots of dV/dJ against $(J + J_{SC})^{-1}$ to the y-axis in Figure 5c, the series resistance R_S were determined as 0.53 Ω cm^2 and 0.65 Ω cm^2 for D0 and D6 respectively, while the resulted ideality factor A were 1.96 and 1.80, obtained from the slope

of *AkT/q*. Finally, the reverse saturation current J_0 was extracted from the plot of $ln(J+J_{sc}-GV)$ against *V-RJ* (Figure 5d). The value of J_0 calculated from the intercept of the curve was 2.2×10^{-3} mA/cm^2 for D0, and 1.3×10^{-3} mA/cm^2 for D6. Consequently, a lower series resistance, lower reverse saturation current, and better diode ideality factor established a much superior CdS/Sb_2Se_3 junction quality, justifying the higher PCE for D6 device. In order to investigate the defect states of fresh deposited and ambient stored Sb_2Se_3 films, the standard space charge limited current (SCLC) model was applied under dark conditions [13]. Figure 5e and f display the logarithmic current-voltage characteristic curves for D0 and D6 devices, respectively. The curves can be divided into three regimes: the orange-colored part of the curves at lower bias voltage presented ohmic response, the central green-colored portions at intermediate voltage was trap-filled limited regimes (TFL), and the pink-colored portion displaying a trap-free child regime at high voltage [36]. It is known that once bias voltage surpasses the kink point from the TFL region, the current snappishly upsurges, signifying that the trap states are entirely filled by the injected carriers. Thus, the obtained onset voltages associated to the TFL region (V_{TFL}) were 0.19 V and 0.15 V for D0 and D6, respectively. Then the trap state density N_{trap} can be calculated conferring to the following Equation [13]:

$$N_{trap} = \frac{2\varepsilon_o\varepsilon_r V_{TFL}}{L^2 q} \quad (4)$$

Where L is the thickness of the Sb_2Se_3 film, q is an elemental charge, ε_0 is the vacuum permittivity, and ε_r is the relative permittivity (i.e., 15.1 for Sb_2Se_3). The obtained N_{trap} values for D0 and D6 were 1.82×10^{15} and 1.44×10^{15} cm^{-3}, respectively. Compared to D0, the D6 device showed a relative lower N_{trap} value, which can be ascribed to its more superior Sb_2Se_3 thin film quality with less trap sites and reduced defect centers.

A comparison of the key performance parameters between our champion D6 device and some previously reported state-of-the-art Sb_2Se_3 solar cells prepared via various thermal deposition techniques is shown in Table 3 [14-16,41-43]. Interestingly, the device performance is comparable

to those high-efficiency devices, especially with the highest V_{OC} value of 430 mV. To scrutinize its development incitement, capacitance-voltage (*C-V*) measurements were carried out to study the junction quality of the devices. Figure 6a illustrates the $1/C^2$-V curves, from which the V_{bi} was extracted through the linear fitting of the curve and extrapolated to the x-axis. The resulted V_{bi} values for D0 and D6 solar cells were 493 and 590 mV, respectively. The upgraded V_{bi} backed the high built-in electric field, inferring an improved Sb_2Se_3/CdS heterojunction for D6 [40], thus leading to an obvious increase in the V_{OC}. *C-V* and deep-level capacitance profiling (*DLCP*) characterizations were also performed to examine the interfacial defects of D0 and D6 (Figure 6b), where the interfacial defect density of both the devices were calculated by subtracting N_{DLCP} from N_{C-V} [13]. The plots of N_{C-V} and N_{DLCP} against the profiling depth (width) were obtained, where N_{C-V} symbolize the responses from free carriers, bulk defects and interfacial defects, while N_{DLCP} reveals the responses from free carriers and bulk defects. For D6, the difference between the two curves is smaller as compared to D0, suggesting lower interfacial defects, and suppressed recombination loss at the Sb_2Se_3/CdS interface. Temperature-dependent open-circuit voltage (V_{OC}-T) measurement was also carried out to further inspect the recombination center of the devices by comparing the activation energy (E_a). The test was performed under a dark condition in the temperature range of 150 K-330 K (Figure 6c). E_a for both the devices was calculated by extrapolating the V_{OC} to the y-axis, and it was lower than the optical bandgap of the Sb_2Se_3 absorber. E_a value of the D6 device was 0.96 eV, which was a bit closer to the bandgap. Thus, the less difference between E_a and E_g of D6 also authenticates suppressed recombination at the Sb_2Se_3/CdS interface. The electrochemical impedance spectroscopy (EIS) offers a simple strategy to extract the magnitude of recombination resistance and illustrate a solar cell interface information. A comparison of the Nyquist plots for D0 and D6 devices are portrayed in Figure 6d, along with an inset equivalent circuit diagram. The arc's diameter length is directly corresponding to the recombination resistance (R_{rec}), suggesting a suppressed charge

recombination at the Sb_2Se_3/CdS interface for D6 device [40]. The series resistance (R_s) value is the intercept on the ReZ, the extracted R_s values for D0 and D6 were 3.17 and 2.71 $\Omega \cdot cm^2$, respectively, the S diffused film would benefit the charge transport and thus decrease R_s. All the results obtained from $1/C^2$-V, *DLCP*, V_{OC}-T, and EIS were found consistent with the previous electrical analysis results (Figure 5). Our investigation revealed that S diffusion at the heterojunction interface upon ambient air storage improved the junction quality by enlarging the built-in electric field via the formation of graded bandgap type ($CdS/Sb_2(S,Se)_3/Sb_2Se_3$), reducing the interfacial defects, and suppressing the recombination loss at the interface. All these important parameters are summarized and listed in Table 4.

Besides various justification about the interface quality improvement for our champion D6 device, admittance spectroscopy was also applied to auxiliary understand the bulk defect properties of D6 film, including the thermal activation energy E_a and the defect density N_t based on temperature-dependent admittance analysis. The capacitance-frequency (*C-f*) spectra measured at various temperatures from 190 K to 330 K is presented in Figure 7a. With the variation of frequency, two distinguishable capacitance steps were witnessed, representing two different defect levels indicated as d1 and d2 (Figure 7b). The value of frequency (ω_0) was obtained from the angular frequency point ω at the maximum of the plot $\omega dC/d\omega$, while the defect activation energies (E_a) were extracted from the slopes of the Arrhenius plot using the Equation (5) [44]:

$$\omega_0 = 2\pi \upsilon_0 T^2 \exp\left(\frac{-E_a}{kT}\right) \quad (5)$$

where E_a is the defect activation energy, representing the average energetic depth of the defect relative to the conduction band minimum or valence band maximum, ω_0 is the inflection point frequency, and v_0 is the attempt-to-escape frequency. By utilizing the Kimerling model based on Equation (6) and (7) [45], the distribution of both the defect types were Gaussian fitted (Figure 7c and d).

$$E(\omega) = kT \ln\left(\frac{2\pi\nu_0 T^2}{\omega}\right) \quad (6)$$

$$N_t(E(\omega) = -\frac{V_d}{q\omega} \cdot \frac{dC}{d\omega} \cdot \frac{\omega}{kT} \quad (7)$$

where ω is the angular frequency, $N_t(E(\omega))$ is the defect density, and V_d is the built-in potential. Both the defect levels with such a low E_a values are acceptable and are in agreement with our findings, reflecting high efficiency [13]. The defect densities of the D6 device are 2.14×10^{15} and 1.37×10^{15} cm^{-3}, respectively. The order of the defect density (10^{15}) is also consistent with previously VTD processed high-efficiency Sb_2Se_3 solar cells [44,46]. Normally, a large number of deep defects produce severe recombination losses in bulk absorber layer as well as the heterojunction interface, declining the overall solar cell performance. However, our high-efficiency device possesses a low defect density, and it is assumed that some deep and interfacial defects are effectively suppressed upon S diffusion during ambient storage.

The interface of CdS/Sb_2Se_3 for D6 was finally characterized by transmission electron microscope (TEM) and energy dispersive spectra (EDS), as displayed in Figure 8a-e. Sb and Se elements are distributed evenly in the whole film. However, S was found to be diffused into Sb_2Se_3 film with a little high concentration near the interface. The unmatched pattern of S with the Cd (Figure 8d, e) authenticates our claim that a small amount of S atoms evaporated during the VTD processed Sb_2Se_3 deposition. Upon storage, the S atoms further diffused to modify the interface by forming a graded bandgap absorber layer with a S-diffused Sb_2Se_3 layer followed by Se-rich/pure Sb_2Se_3 film (Figure 8e). High-resolution transmission electron microscopy (HRTEM) imaging was further accomplished at Sb_2Se_3/CdS junction, middle and top of the film by selecting three different points in Figure 8a. A high-quality heterojunction with smooth interface was observed between the Sb_2Se_3 layer and CdS layer without any strict interfacial discontinuity (Figure 8f). The three chosen points across the absorber layer exhibited the lattice fringe with interplanar d-spacing of 0.310 nm, 0.314 nm and 0.319 nm, respectively (Figure 8f-h), which can be assigned to the (211) lattice plane of the

orthorhombic phase Sb_2Se_3 [35]. The obtained vertical preferred orientation (hk1) across the whole Sb_2Se_3 film would facilitate charge carrier transport and improve the device performance. Moreover, a slight decrease in d-spacing for Sb_2Se_3 near the CdS/Sb_2Se_3 interface are possibly caused by the diffused S atoms with smaller atomic radius. Thus, a smooth and adherent interface between CdS and Sb_2Se_3, leading to grow preferentially (hk1) oriented Sb_2Se_3 film without any harmful dislocation, amorphous layer formation, extra phase presence, and crystal lattice distortion.

Finally, thanks to the obtained graded bandgap structure, comparatively large bandgap $Sb_2(S,Se)_3$ at interface led to generate a high V_{OC}, while the pure high-quality Sb_2Se_3 film on the top harvested a wide spectrum of light to generate a high J_{SC}. A schematic representation of this explanation is presented in Figure 9, where the broadening of the bandgap with S incorporation is approximated from our previously published work [38]. Our champion device achieved one of the top values of J_{SC} (28.22 mA/cm^2) by optimizing the deposition condition, combined with the highest V_{OC} (430 mV) for superstrate CdS/Sb_2Se_3 thin film solar cells through interface modification, leading to an interesting PCE of 7.49%.

3. Conclusion

In summary, Sb_2Se_3 light absorbing films with large crystal grains and benign preferential orientation were prepared by an effective deposition-controlled VTD method. The S evaporation from CdS buffer layer during VTD process followed with a self-activated diffusion at the CdS/Sb_2Se_3 interface upon ambient air storage could induce an interesting gradient bandgap of the Sb_2Se_3 absorber layer. Subsequently, a superstrate thin film solar cell with architecture of ITO/CdS/$Sb_2(S,Se)_3$/Sb_2Se_3/Au was achieved. Where the large bandgap S-diffused $Sb_2(S,Se)_3$ film forms a junction with CdS to produce a high V_{OC}, while the narrow bandgap Se-rich/pure Sb_2Se_3 on the rear side of the film enables superior light-harvesting for high J_{SC}. Sulfur diffusion at the heterojunction interface could also efficiently improve the

CdS/Sb_2Se_3 junction quality with suppressing interfacial and/or bulk recombination losses, resulting in an obvious enhancement of V_{bi} from 493 to 590 mV. Consequently, the champion device delivers an interesting PCE of 7.49%, the corresponding V_{OC} (430 mV) represents the highest value for that of thermally deposited Sb_2Se_3 solar cells. These interesting results can pave the way for further enhancing the V_{OC} and PCE of chalcogenide-based solar cells.

4. Experimental Section

Preparation of Sb_2Se_3 thin film solar cells

The solar cells were fabricated based on industrial ITO (In_2S_3:Sn) transparent conductive glass purchased from Kaivo. The thickness of ITO is about 200 nm, with sheet resistance below 10 ohms/sq and transmittance above 83%. The ITO substrates were cleaned with ultrasonic cleaner for 5 min by soaking in detergent, clean water, ethanol, and clean water, respectively. Then the ITO substrates were dried with N_2 gas blow. Cadmium sulfide (CdS) buffer layer was deposited via chemical bath deposition. The aqueous solution of cadmium sulfate (0.015 M), thiourea (0.75 M) and ammonium hydroxide aqueous solutions (28%) were added to deionized water and the substrates (ITO) were suspended into the mixed salutation maintained at 80 °C water bath under continuous stirring for 9 min. The substrates were washed, dried and subjected to $CdCl_2$ treatment followed by annealing at 400 °C in open air. The Sb_2Se_3 films were deposited on the ITO/CdS substrates by VTD process, which operated in a double-chamber vacuum tubular furnace (Tianjin Zhonghuan Furnace Corp.). 0.5 g Sb_2Se_3 powder (99.999% purity, Jiangxi Ketai) was weighed and transferred into a quartz crucible, then placed at the center of the furnace heat zone, which was close to the extraction valve in a quartz tube. Both sides of the furnace zone were running during the deposition process with same program of a ramping rate of 23 ℃/min at 0.01 Torr pressure and kept for 3 min at 510 °C, 520 °C, 530 °C and 540 °C respectively to obtain a preferable film thickness. In this experiment, the distance was fixed at 5.9 cm, and the substrate was immobilized on the

graphite support. Upon cooling, the samples were collected and subjected to 90 nm thick gold back-contact electrodes with an effective area of 0.09 cm^2 in a vacuum chamber under a pressure of less than 5×10^{-4} Pa. Sb_2Se_3 thin film solar cell with superstrate structure of ITO/CdS/Sb_2Se_3/Au was fabricated and used for the subsequent performance measurements.

Thin film and device Characterizations

The crystal structure of Sb_2Se_3 thin film was characterized by X-ray diffraction (XRD, Ultima-iv) with CuKα radiation under 40 kV and 40 mA conditions. Surface and cross-sectional morphologies of the Sb_2Se_3 thin films were obtained from a Zeiss SUPRA 55 thermal field emission scanning electron microscope (SEM). Transmission electron microscopy (TEM) measurements were performed on FEI Titan Cubed Themis G2 300 microscope, and the sample was prepared by ablating a single thin film device by using a focused ion beam (FIB, FEI Scios). SEM/TEM-coupled energy dispersive X-ray spectroscope (EDS) was also used to analyze the chemical compositions and elemental distribution. Current density-voltage (*J-V*) curves were measured by using a millimeter (Keithley, 2000 Series) under AM 1.5G light illumination from a 3A solar simulator with intensity calibrated to 100 mW/cm^2 through a Si reference cell. The voltage was forwardly and backwardly scanned from -0.1 V to 0.5 V with a scan rate of 0.02 V/s. The external quantum efficiency (EQE) spectra were obtained using a Zolix SCS101 system with a monochromator and a Keithley 2400 source meter. Capacitance-voltage (*C-V*) measurements were applied at an AC amplitude of 30 mV and a frequency of 10 kHz under the dark at room temperature. The DC bias voltage during the *C-V* measurements was applied from -1 V to 0.3 V. Drive level capacitance profiling (*DLCP*) measurements were performed with an AC amplitude from 20 mV to 140 mV, and a DC bias voltage from -0.2 V to 0.2 V. Electrochemical impedance spectra (EIS) characterization was measured under a bias voltage of 0.2 V with frequency ranging from 0.01 Hz to 500 K Hz and AC amplitude of 0.01 V. Temperature-dependent capacitance-frequency (*C-f-T*) measurements were conducted within the frequency range of

1K Hz-10 M Hz. The devices were mounted inside a Janis VPF-100 cryostat and cooled with liquid nitrogen.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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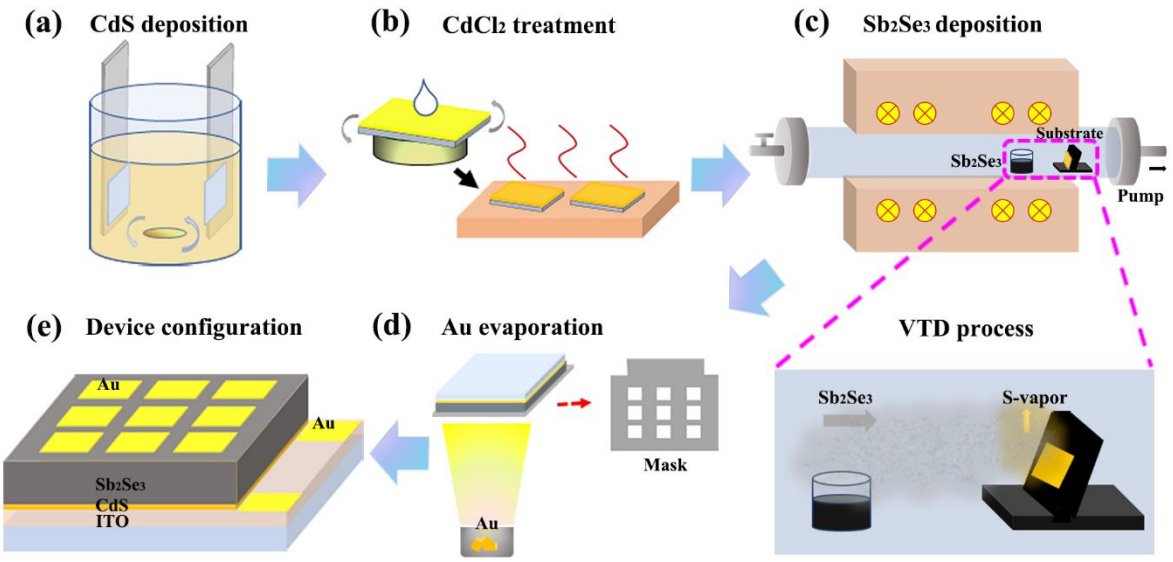


Figure 1. Schematic illustration of the preparation process of the superstrate structured Sb_2Se_3 thin film solar cell. (a) CdS buffer layer deposition via CBD method, (b) $CdCl_2$ treatment of CdS layer, (c) VTD process for Sb_2Se_3 deposition, including the illustration of the evaporation of S atoms from CdS, (d) Au evaporation as back contact, (e) Device architecture.

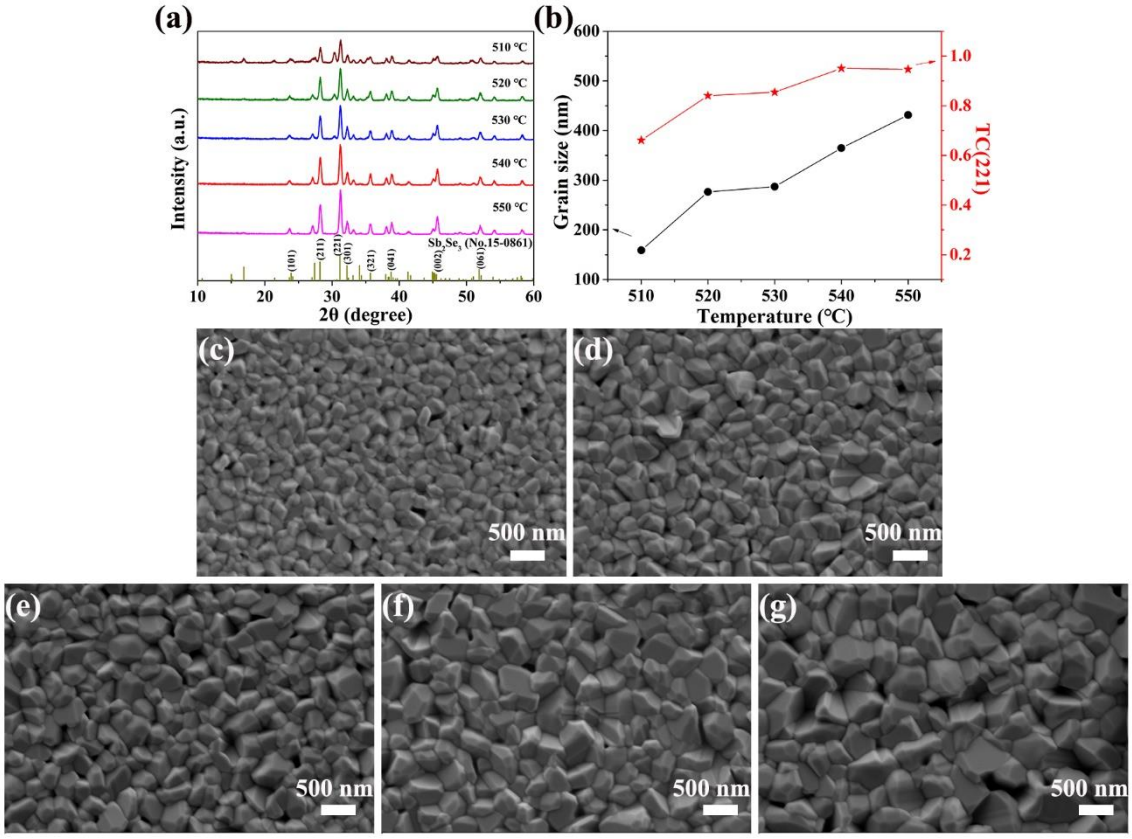


Figure 2. (a) XRD patterns of Sb_2Se_3 films prepared at different temperatures, (b) Temperature-dependent grain size and texture coefficient of (221) diffraction peaks, (c-g) SEM surface images of Sb_2Se_3 films deposited at different temperatures.

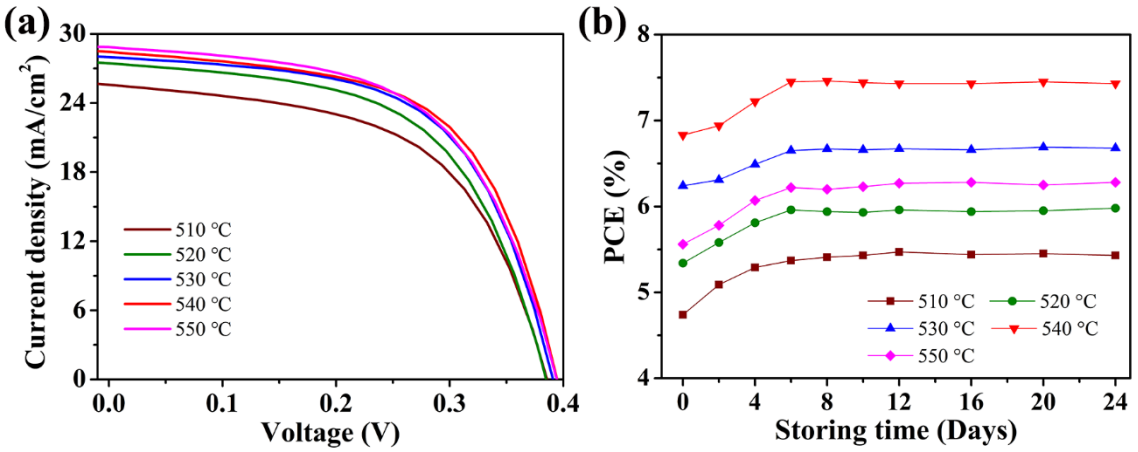


Figure 3. (a) *J-V* curves of the Sb_2Se_3 solar cells with Sb_2Se_3 films deposited at different temperatures, (b) PCE evolution of the solar cells upon different storage time.

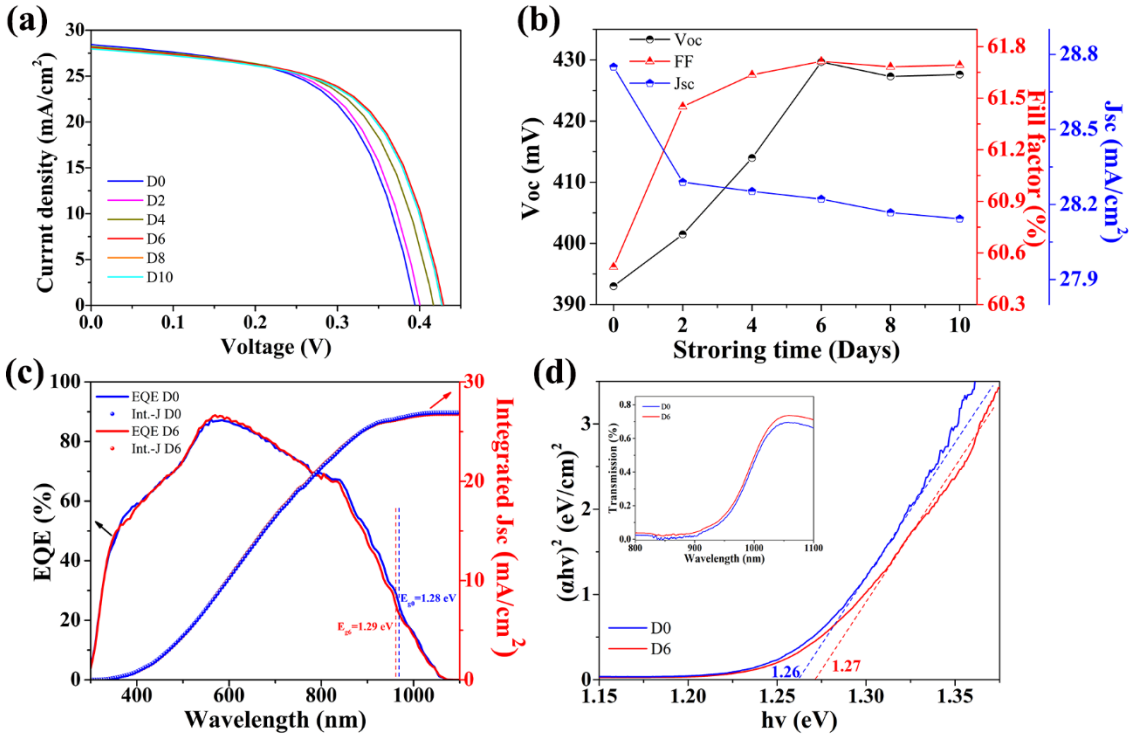


Figure 4. (a) *J-V* curves of the Sb_2Se_3 solar cells with different storage time, (b) Evolutions of the key performance parameters, (c) EQE and integrated J_{SC} for best performing device associated to D0 and D6, (d) Bandgap calculation of Sb_2Se_3 films for D0 and D6, with transmittance spectra (inset).

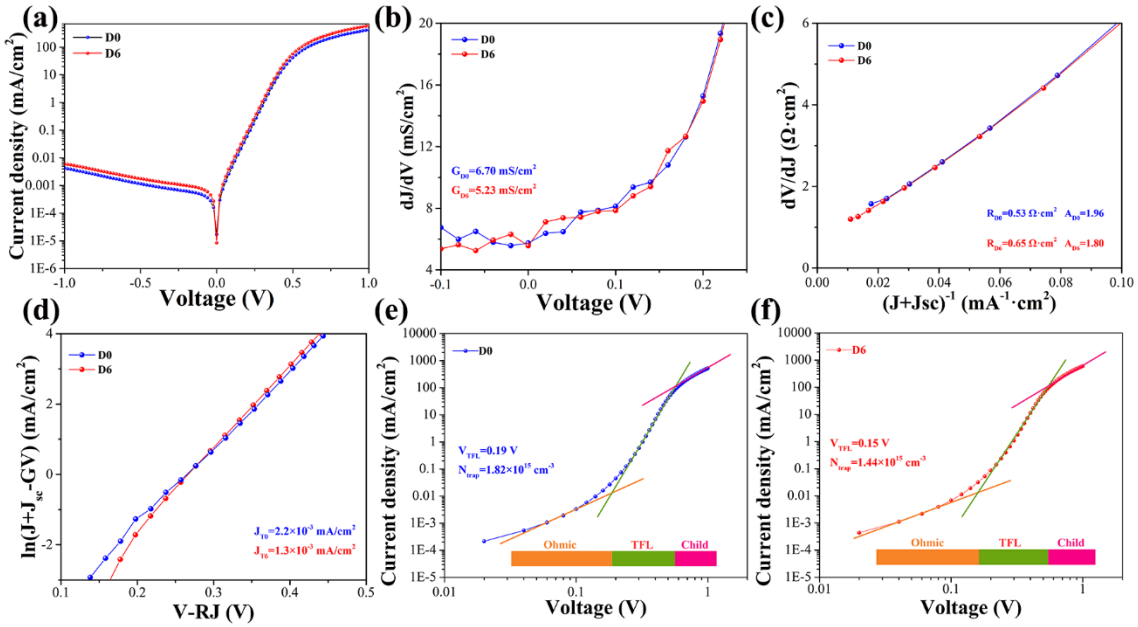


Figure 5. Electrical behaviors of the representative D0 and D6 devices: (a) Dark *J-V* curves, (b) shunt conductance *G* characterizations, (c) series resistance *R* and ideality factor *A* characterizations, (d) reverse saturation current density J_0 characterizations. (e) and (f) are logarithmic *J-V* curves of the D0 and D6 devices, respectively, showing Ohmic, TFL and Child region.

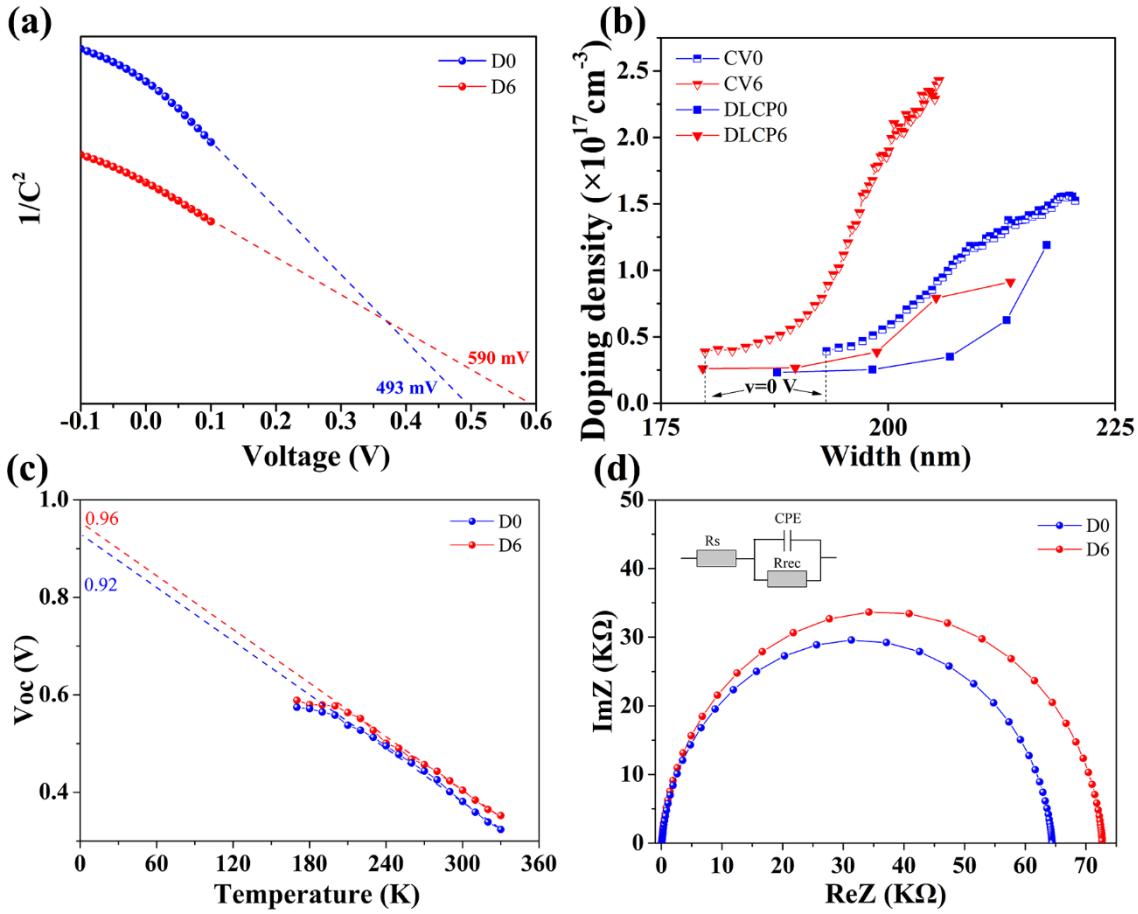


Figure 6. Sb_2Se_3/CdS heterojunction junction characterizations, (a) $1/C^2$–V plots, (b) *CV* and *DLCP* profiles, (c) Temperature-dependent V_{OC} measurements, (d) Nyquist plots for D0 and D6 devices, respectively.

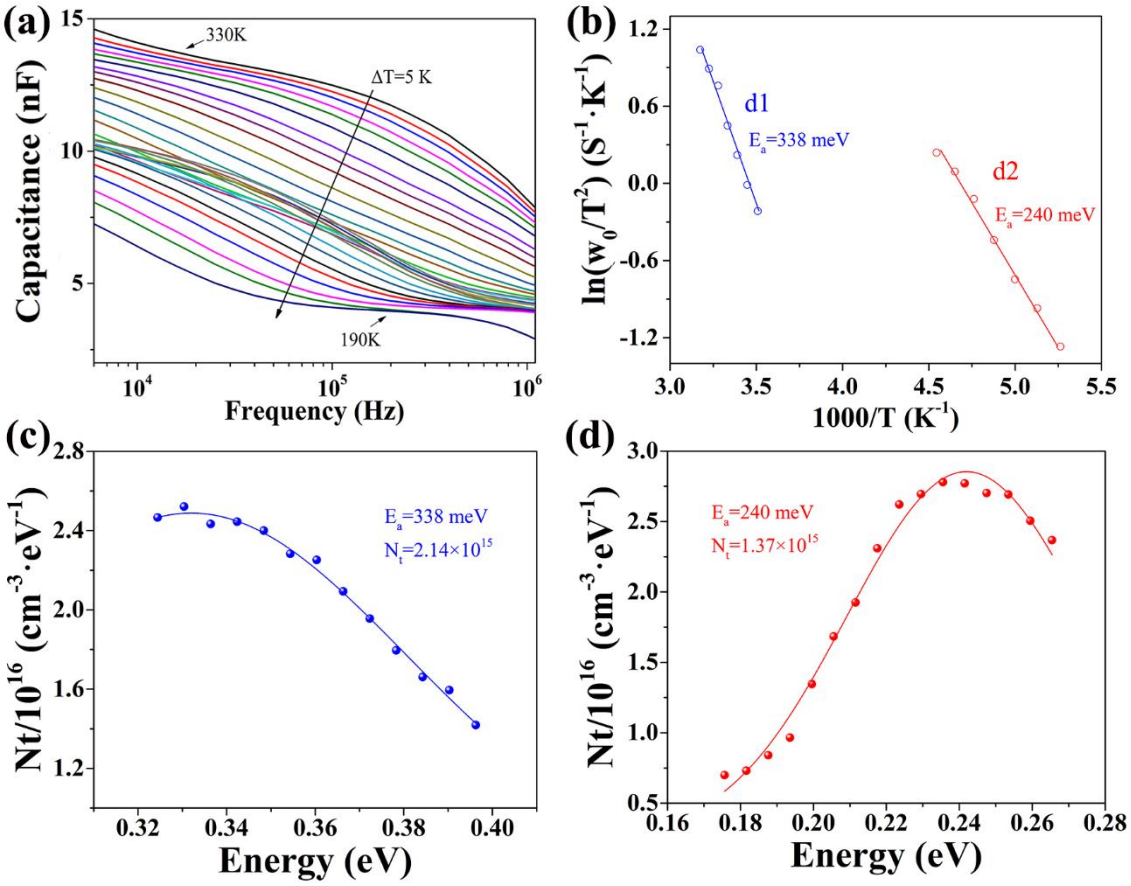


Figure 7. Temperature-dependent admittance analyses of the champion D6 device. (a) Capacitance-frequency-temperature (*C-f-T*) spectra, (b) defect activation energies. Defect distributions of (c) d1 and (d) d2 defects derived from the admittance spectra.

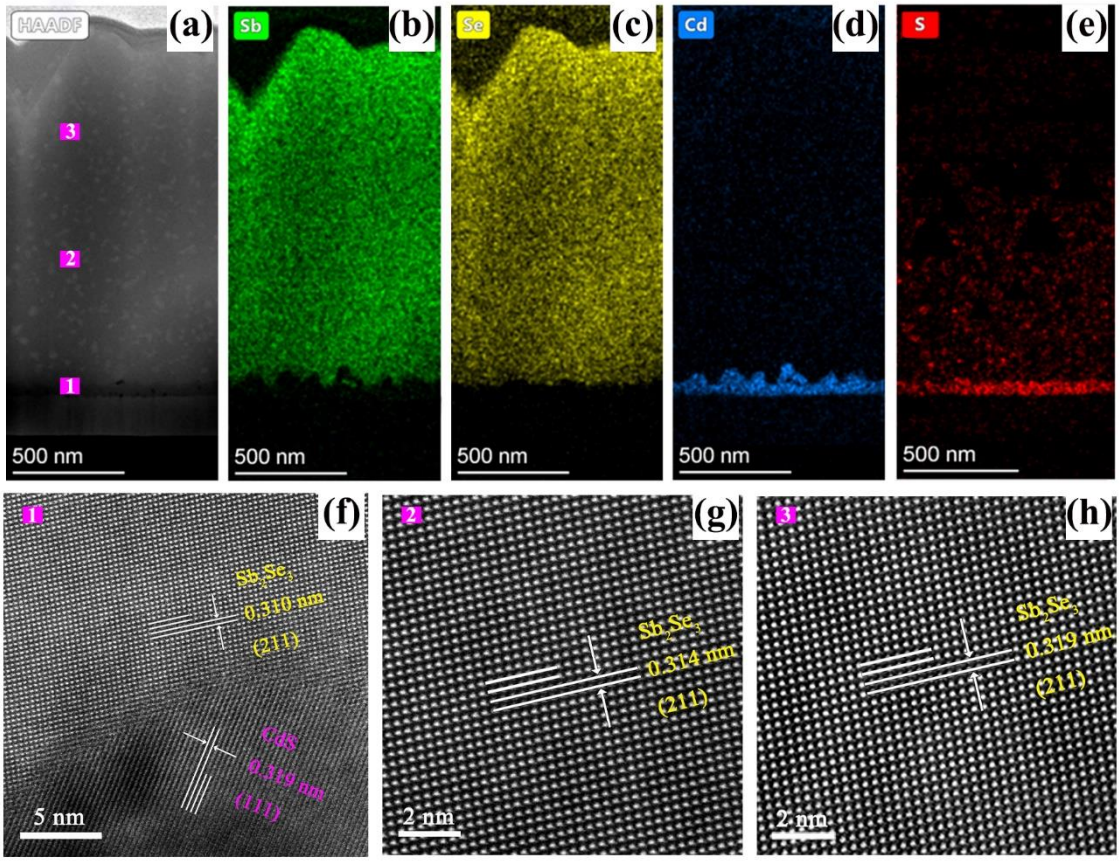


Figure 8. (a) Cross-sectional TEM image of D6 device, portion 1, 2 and 3 representing CdS/ Sb_2Se_3 interface, Sb_2Se_3 layer with S diffusion, and top pure Sb_2Se_3 layer, respectively. (b-e) The elemental EDS mappings of CdS and Sb_2Se_3 layers. HRTEM image of (f) CdS/Sb_2Se_3 interface (portion 1), (g) S diffused Sb_2Se_3 layer (portion 2), and (h) the top Sb_2Se_3 layer (portion 3).

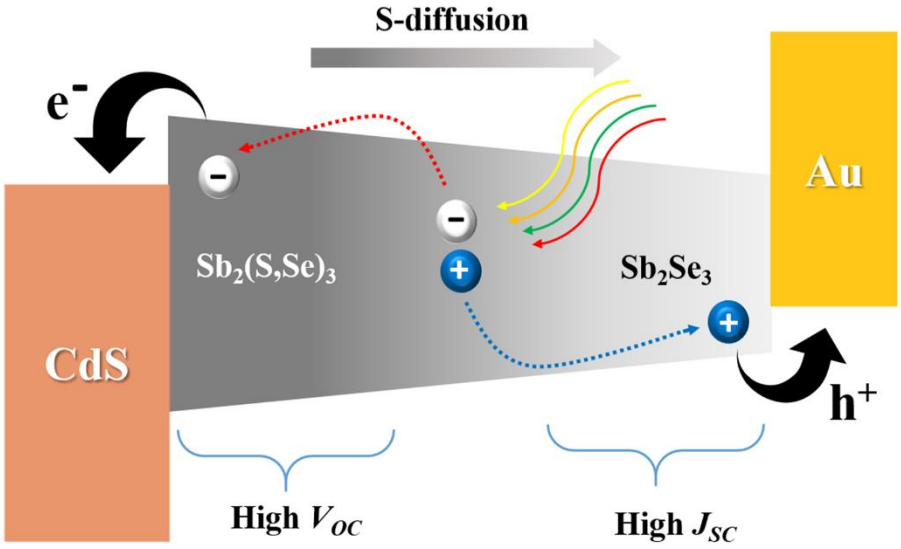


Figure 9. Schematic representation of the Sb_2Se_3 bandgap variation upon S diffusion.

Table 1. EDS determined elemental ratio of Sb_2Se_3 films prepared at different temperatures

Temperature (°C)	Sb (At %)	S (At %)	Se (At %)
510	40.92	5.09	53.99
520	40.74	1.59	57.68
530	34.04	0.72	65.24
540	39.96	0.09	59.96
550	36.11	0.39	63.49

Table 2. EDS characterizations of the surface and cross-sectional D0 and D6 films

Sample	Sb (At %)	S (At %)	Se (At %)
Cross-D0	39.24	2.12	58.64
Cross-D6	43.12	4.50	52.38
Surface-D0	39.96	0.09	59.96
Surface-D6	40.13	0.13	59.74

Table 3. A comparison of Sb_2Se_3 solar cells prepared via various thermal deposition methods

Method	Device configuration	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	PCE (%)	Ref.
CSS	Mo/Sb_2Se_3/CdS/TiO_2/ZnO/Ag	400	32.58	70.30	9.20	[15]
CSS	FTO/SnO_2/CdS/Sb_2Se_3/t-Se/Au	413	28.90	62.30	7.45	[41]
TE	ITO/SnO_2/CdS/Sb_2Se_3/Au	380	28.10	59.10	6.20	[42]
RTE	FTO/TiO_2/Sb_2Se_3/PbS/Au	386	32.60	60.60	7.62	[14]
VTD	ITO/CdS/Sb_2Se_3/Au	420	29.90	60.40	7.60	[16]
VTD	FTO/CdS/Sb_2Se_3/Al_2O_3/Au	405	31.02	58.52	7.35	[43]
VTD	ITO/CdS/Sb_2Se_3/Au	430	28.22	61.71	7.49	This work

Table 4. Summary of photovoltaic parameters for D0 and D6 devices

Device	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)	PCE (%)	R_S (Ω·cm^2)	J_0 (mA/cm^2)	V_{bi} (mV)	A	N_{trap} (cm^{-3})
D0	28.75	393	60.51	6.83	3.17	2.2×10^{-3}	493	1.96	1.82×10^{-3}
D6	28.22	430	61.71	7.49	2.71	1.3×10^{-3}	590	1.80	1.44×10^{-3}

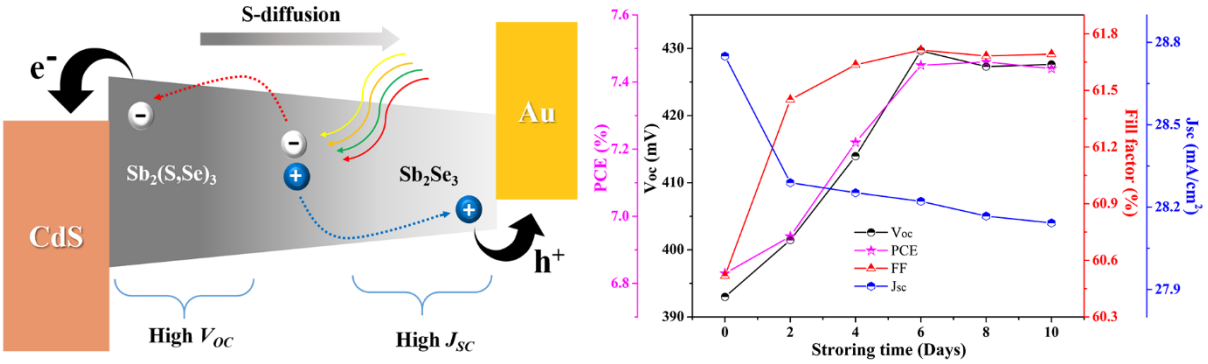
Table of contents: Sb_2Se_3 films with large crystal grains and benign orientation are prepared via a deposition-controlled VTD method. The sulfur evaporation from CdS followed with a self-activated diffusion at the CdS/Sb_2Se_3 interface upon ambient air storage can induce an interesting gradient structure of CdS/$Sb_2(S,Se)_3$/Sb_2Se_3. The champion device delivers an interesting PCE of 7.49%, a V_{OC} of 430 mV represents the highest value for that of thermally deposited Sb_2Se_3 solar cells.

Keyword: Sb_2Se_3 Solar Cell, Open-Circuit Voltage, Interface, Sulfur Diffusion, Gradient Bandgap

Shuo Chen, Muhammad Ishaq, Wei Xiong, Usman Ali Shah, Umar Farooq, Jingting Luo, Zhuanghao Zheng, Zhenghua Su, Ping Fan, Xianghua Zhang and Guangxing Liang**

Title: Improved Open-Circuit Voltage of Sb_2Se_3 Thin Film Solar Cells via Interfacial Sulfur Diffusion Induced Gradient Bandgap Engineering

ToC figure



Supporting Information

Improved Open-Circuit Voltage of Sb_2Se_3 Thin Film Solar Cells via Interfacial Sulfur Diffusion Induced Gradient Bandgap Engineering

Shuo Chen, Muhammad Ishaq, Wei Xiong, Usman Ali Shah, Umar Farooq, Jingting Luo, Zhuanghao Zheng, Zhenghua Su, Ping Fan, Xianghua Zhang and Guangxing Liang**

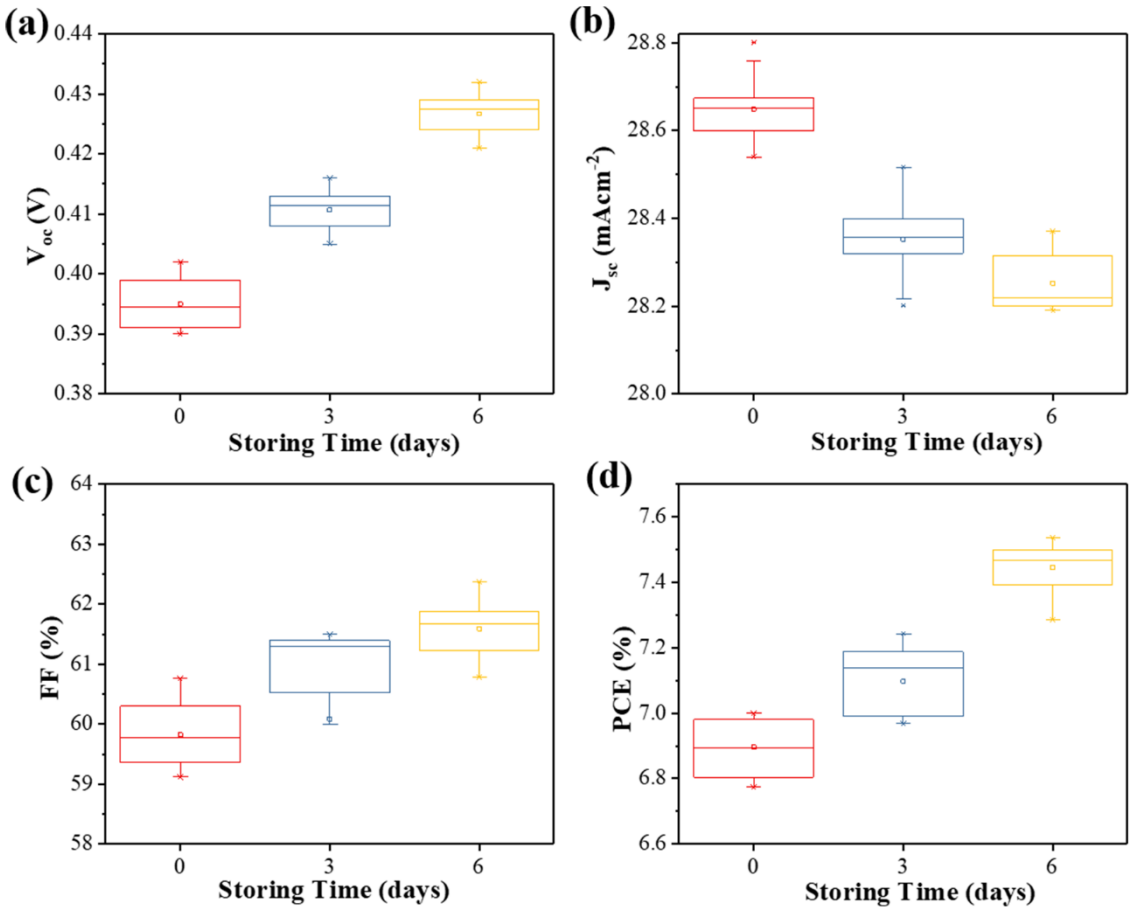
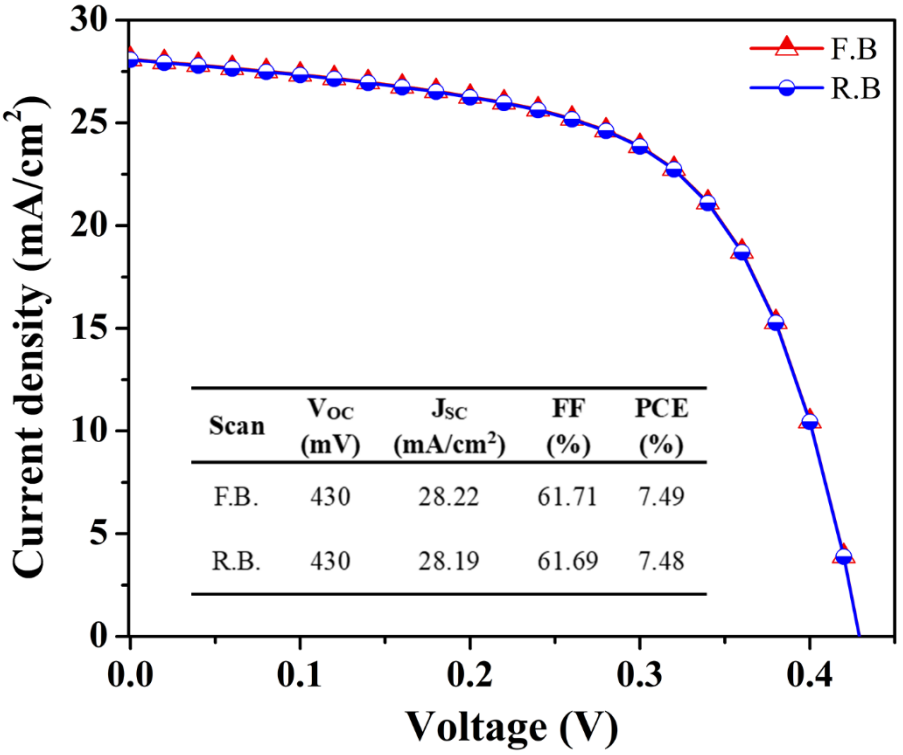


Figure S1. Statistical distribution of the performance parameters of the Sb_2Se_3 solar cells with different storage time, (a) V_{OC}, (b) J_{SC}, (c) FF, and (d) PCE. Error bars represent the reproducibility and standard deviation calculated over the performances of fifteen devices.



Scan	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	PCE (%)
F.B.	430	28.22	61.71	7.49
R.B.	430	28.19	61.69	7.48

Figure S2. Froward biased and reversed biased scanned *J-V* curves of the champion D6 device.

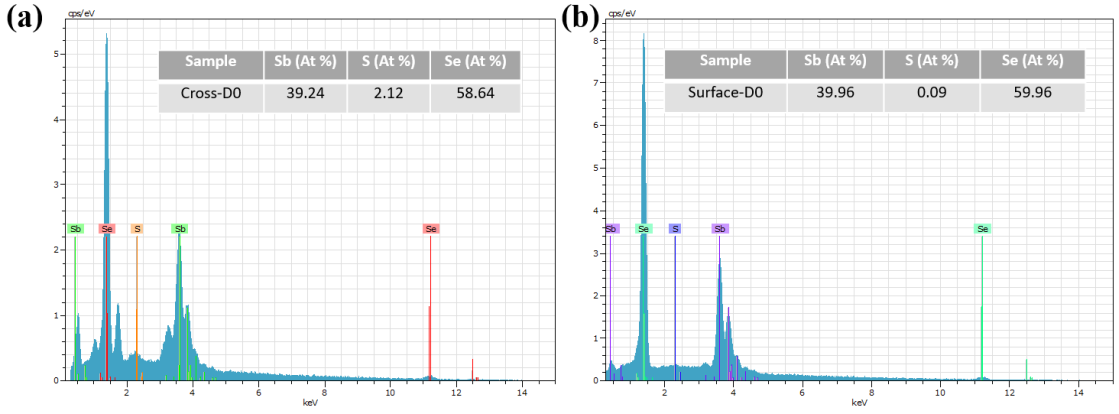


Figure S3. Energy dispersive spectroscopy of D0-Sb_2Se_3 film: (a) Cross-section, (b) Surface.

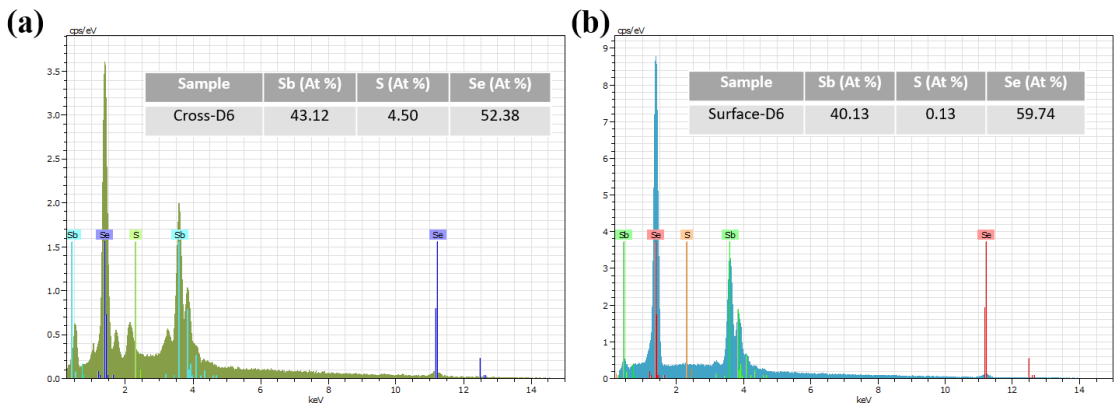


Figure S4. Energy dispersive spectroscopy of D6-Sb_2Se_3 film: (a) Cross-section, (b) Surface.

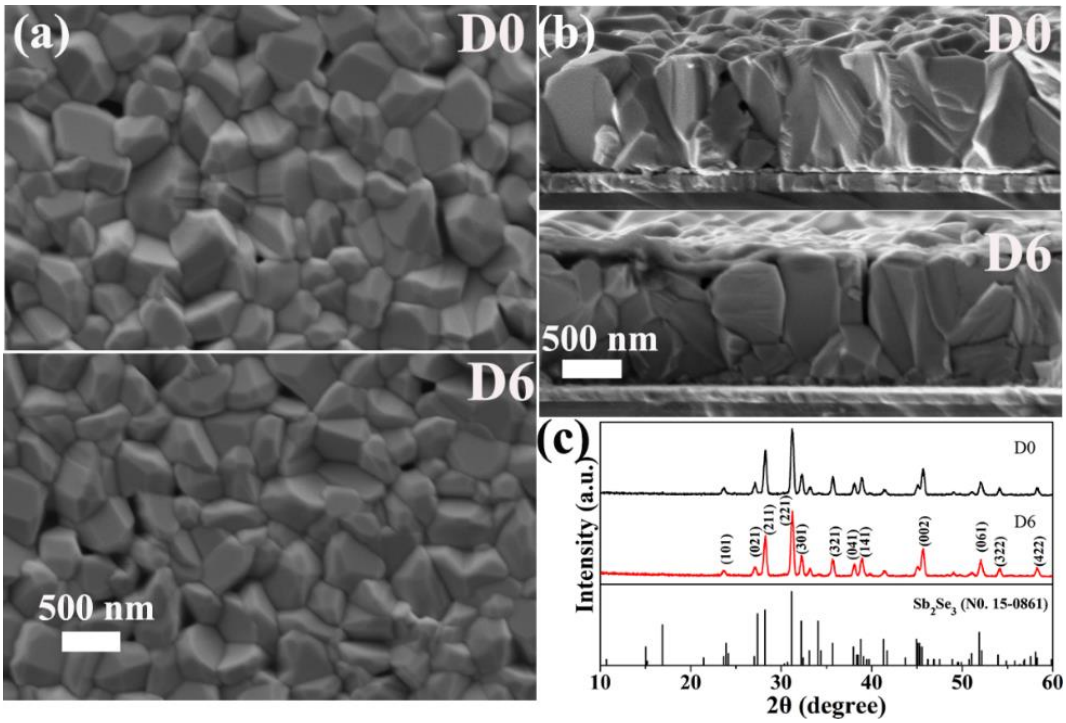


Figure S5. SEM images and XRD patterns of D0-Sb_2Se_3 and D6-Sb_2Se_3 films: (a) Surface morphologies, (b) Cross-sectional morphologies, (c) XRD patterns.