A 237 ppm / ◻ C L-Band Active Inductance Based Voltage Controlled Oscillator in SOI 0.18 μm

João R. Raposo de O. Martins, Francisco Alves, Pietro Maris Ferreira

A 237 ppm/$^{\circ}C$ L-Band Active Inductance Based Voltage Controlled Oscillator in SOI 0.18 μm

J. R. O. R. Martins[1,2], Francisco Alves[1,2], Pietro M. Ferreira [2,1]
[1]Université Paris-Saclay,CentraleSupélec,CNRS,Lab. de Génie Électrique et Électronique de Paris,91192,Gif-sur-Yvette,France
[2]Sorbonne Université, CNRS, Lab. de Génie Électrique et Électronique de Paris, 75252, Paris, France
email: joao-roberto.raposo@centralesupelec.fr, francisco.alves@u-psud.fr, maris@ieee.org

***Abstract*—Multi-frequency receivers have become a standard for Global Navigation Satellite Systems (GNSS) and Global Positioning Systems (GPS) applications. In smart vehicle applications, multi-frequency receivers need to work reliably in a large temperature variation. Even though literature has presented solutions for frequency stability over temperature, they usually rely on external control circuits or non-silicon solutions such as wide-bandgap materials or MEMS resonators, leading to higher production costs. This work proposes a temperature-aware design of an active-inductor-based, MOSFET only, voltage-controlled oscillator suitable for the L-Band. The temperature analysis is made based on a g_m/I_D methodology for the transistor biasing and MOSFET capacitors. Those analyses are validated from simulation models (-40 $^{\circ}C$ to 175 $^{\circ}C$) and transistor measurements up to 200 $^{\circ}C$. Monte-Carlo post-layout simulations present a mean first-order temperature coefficient of 237 ppm/$^{\circ}C$ and cover the entire L-Band.**

***Index Terms*—temperature-aware, L-band, Voltage Controlled Oscillator, gm/ID**

I. Introduction

Smart sensing and positioning have gained increasing attention in the last few years. Smart Vehicles sensing must efficiently locate, sense, and communicate with other nearby devices, considering the working environment [1]. For obvious reasons, circuit design and specification are regulated by many strict security and safety standards. The temperature range is arguably the most demanding environmental challenge for electronics in the automotive industry [2], and aircrafts [3].

Literature has proposed some solutions for low temperature coefficient oscillators. Ottaviani et al. evaluate temperature variations on inductors and capacitors components for high-frequency and high-temperature GaN-based oscillators [4]. However, wide band-gap materials having a higher production cost hinders the integration of digital circuits on-chip, an essential feature of smart sensing. Schwartz and Ponchak propose a 1 GHz SiC Clapp oscillator working at 200 $^{\circ}C$ [5]. However, no frequency temperature stabilization is proposed. Shanmugalingam et al. propose a digital supply voltage modulation scheme to compensate for the temperature effects on a 5-stage ring oscillator [6]. Shin et al. propose a diffusion doping-based method for controlling the frequency temperature coefficient for a MEMS resonator achieving smaller than dozens ppm/$^{\circ}C$ [7]. The result is validated at different resonant modes, and crystalline orientations maximum frequency variation on a reduced maximum surface are of 0.29 mm^2.

In [8], a passive LC-VCO with a low temperature coefficient is achieved using an additional PLL loop filter and auxiliary varactors. However, the analyzed temperature range is limited to 80 $^{\circ}C$. Besides, passive inductors and the high values of resistors and capacitors are a limiting factor for certain technology nodes and considerably increase the silicon surface. In [9], a PLL with a digital controlled oscillator is proposed with an external calibration circuit implement on an FPGA to compensate the temperature drift. Published works often rely on wide-bandgap transistors or feedback control systems to stabilize the VCO, increasing power consumption and silicon area.

This work proposes a temperature-aware design using the g_m/I_D methodology for a voltage-controlled oscillator on the L-Band communication. The proposed methodology allows temperature considerations in an early design stage. The development is done using the UICM model and temperature normalized g_m/I_D parameters. Validation is done on BSIM v4.6, factory-validated from -40 $^{\circ}C$ to 175 $^{\circ}C$, and measurement data for higher temperatures (up to 200 $^{\circ}C$). The analyzed circuit uses active inductors, allowing for a wider tuning range with a reduced area. The achieved results are compared with a more traditional design framework presenting a performance improvement ranging from 2.62 to 9.84 times better. A post-layout Monte Carlo is presented to evaluate the temperature sensibility in the presence of process and mismatch variations, presenting presents a mean figure of merit (FOM) of 131 dBc/Hz and a mean temperature coefficient of 237.8 ppm/$^{\circ}C$ over the entire temperature range.

This brief is organized as follows. Section II briefly presents the circuit topology and the analytical temperature model for the different circuit sub-blocks. Section III uses the previously developed temperature models to calculate transistors bias and sizing for achieving the oscillation frequency low temperature coefficient. Section IV concludes and summarizes this brief.

II. VCO Temperature Analysis

Oscillators are often classified into five main categories (RC, Ring, LC, Crystal, and MEMS). In [10], a survey indicates that LC-based oscillators present an overall better performance for L-band applications. Lu et al. presented a very wide tuning range LC-based oscillator with an active inductance and low noise performance [11]. Figure 1 illustrates the VCO under

analysis, composed by an active inductor (L_{active}), a MOS capacitor (C_{var}), and a negative impedance (G_{comp}).

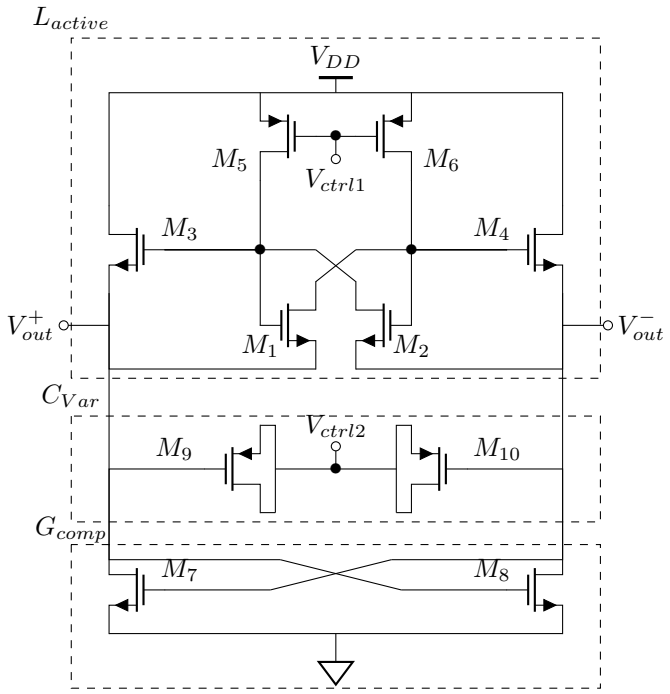


Fig. 1. Active Inductor Based VCO.

The active inductance L_{active}, controlled by V_{ctrl1}, allows a very wide tuning range. However, it can present a large temperature variation [12]. The tunable MOS varicap C_{Var} is controlled by V_{ctrl2}. The G_{comp} works as a negative resistance to nil the real part of the LC impedance and enforce oscillation. The LC tank resonance frequency gives the oscillation frequency:

$$F_{osc} = \frac{1}{2 \cdot \pi \sqrt{L_{eq} \cdot C_{var}}}. \tag{1}$$

To evaluate the oscillation frequency temperature sensitivity, one may use the sensitivity operator defined in [13] as $S_x^{f(x)} = \partial f(x)/\partial x \cdot x \ f(x)$

$$S_T^{F_{osc}} = S_T^{L_{eq}} + S_T^{C_{var}}. \tag{2}$$

It is clear from (2) that in order to have a zero temperature coefficient (ZTC) oscillation frequency the relation between $S_T^{L_{eq}}$ and $S_T^{C_{var}}$ must be:

$$S_T^{F_{osc}} = 0 \Longleftrightarrow S_T^{L_{eq}} = -S_T^{C_{var}}. \tag{3}$$

To further investigate the total temperature sensitivity in this oscillator, one may first study the different temperature behavior of C_{var} and L_{active}. For these matter sub-section II-A and II-B will be consecrated for the temperature analysis of the varicap and the active inductance respectively.

A. Varicap Temperature Analysis

To evaluate the variable capacitor implemented on the proposed oscillator, one may start by expressing C_{var} as a function of the intrinsic capacitors from the PMOS transistor as:

$$C_{var} = 2 \cdot (C_{gb_p} + C_{ds_p} + C_{ds_p}) \tag{4}$$

where C_{gb_p} is the capacitance between gate and bulk; C_{ds_p} the capacitance between drain and source; and C_{gd_p} the capacitance between gate and drain. Both transistors M_9 and M_{10} are assumed with same size and with a large enough gate area to consider the overlap capacitance negligible. In order to evaluate C_{var}, one may take the model used in [14]:

$$C_{gb_p} = \frac{\eta - 1}{\eta} (C_{ox} - C_{gs} - C_{gd}) \tag{5}$$

$$C_{gs_p} = \frac{2}{3} C_{ox} \frac{1 + 2\alpha}{(1+\alpha)^2} \frac{q_{IS}}{q_{IS} + 1} \tag{6}$$

$$C_{gd_p} = \frac{2}{3} C_{ox} \frac{\alpha^2 + 2\alpha}{(1+\alpha)^2} \frac{q_{ID}}{q_{ID} + 1} \tag{7}$$

$$\alpha = \frac{q_{ID} + 1}{q_{IS} + 1}, \tag{8}$$

where C_{ox} is the total oxide capacitance; q_{ID} the normalized inversion charge on the drain; q_{IS} the normalized inversion charge on the source. Since both drain and source are connected the channel voltage, one may assume $q_{IS} = q_{ID} = q_0 \rightarrow \alpha = 1$. By using this fact the total capacitance C_{var} can be expressed as:

$$C_{var} = C_{ox} \frac{\eta - 1}{\eta} \frac{1}{q_0 + 1}. \tag{9}$$

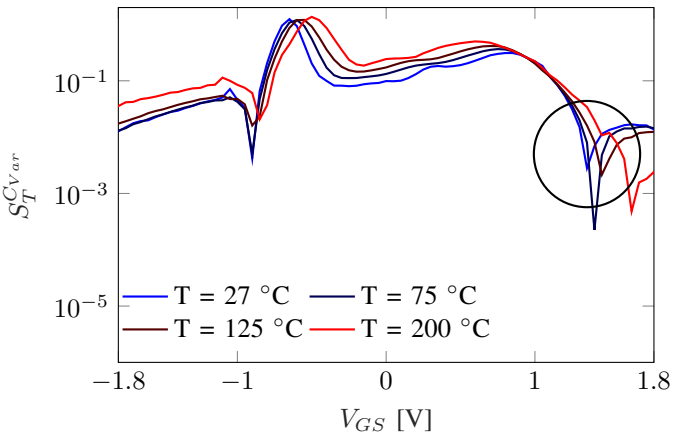
In most applications, transistors are biased in depletion and inversion regimes, since at those biasing condition the channel conductance decrease allowing the drain to source current. For this reason, most design-by-hand models usually consecrate more attention to those regimes to the detriment of the accumulation region [14]. For these reasons, hand analysis models can present less accurate results in accumulation. However, for RF application varicaps must be biased in accumulation since in this region the channel charge does not depend on recombination of carriers and therefore the capacitance does not suffer from non-quasi-static effects.

Fig. 2(a) highlights a second ZTC point that happens close to the accumulation region ($V_{GS} < V_{FB}$), in this region the pinch-off voltage approximation $V_p \approx (V_{GS} - V_{th})/\eta$ does not hold anymore. In order to further investigate this ZTC point, one may take the deep-accumulation approximation given by:

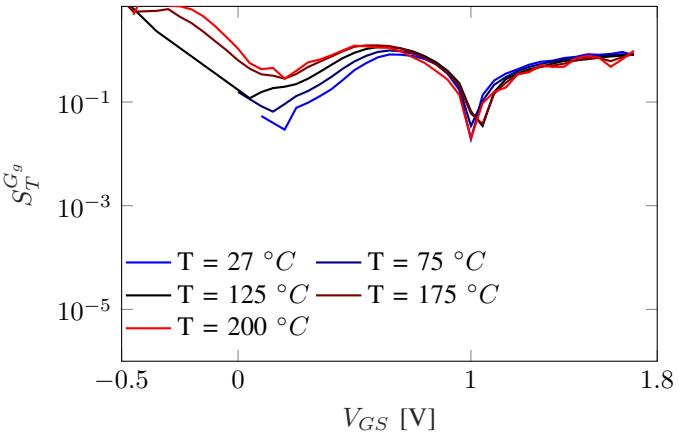
$$Q_b \approx -C_{ox} \gamma \phi_t e^{\frac{\psi_s}{2\phi_t}}, \tag{10}$$

$$C_b = \frac{\partial Q_b}{\partial \psi_s} = -\frac{Qb}{2}, \tag{11}$$

where Q_b is the bulk charge; C_b the bulk capacitance; C_{ox} the oxide capacitance; ϕ_t the thermal voltage; γ the bulk-effect parameter; and ψ_s the surface potential. By using this



(a)



(b)

Fig. 2. Extracted sensitivity extracted from measurement data for C_{var} (a) and G_g (b).

approximation, one may calculate the surface potential in relation to the $V_{GB_0} = V_{GB} - V_{FB}$ as:

$$\psi_s = 2\phi_t W_0\left(\frac{\gamma}{2}e^{\frac{V_{GB_0}}{2\phi_t}}\right) + V_{GB_0}, \tag{12}$$

where W_0 is the principal branch from the Lambert-W function. The total capacitance C_{Var} is given by the series association between C_b and Cox. A sufficient condition for the ZTC point at deep-accumulation can be obtained by:

$$\frac{\partial C_b}{\partial T} = 0 \tag{13}$$

Using the surface potential model and considering a linear flat-band voltage temperature dependency with a temperature coefficient α_{fb} one may find the ZTC condition for C_{var} in accumulation as:

$$V_{GB} = \alpha_{fb}T + V_{fb} - (2\ln(\gamma) + 1)\,\phi_t \tag{14}$$

$$\alpha_{fb} = \frac{1}{T}\left(\frac{E_G\,(T=0)}{2\cdot q} - \phi_F\right), \tag{15}$$

for Silicon, the extrapolated bandgap at 0 K $(E_G\,(T=0)\,/q)$ is 1.12 eV; for usual doping levels, the bulk Fermi level ϕ_F is not very apart from the middle gap $(E_G\,(T=0)\,/2\cdot q)$ making the flat-band voltage (V_{FB}) temperature derivative very low and therefore the accumulation ZTC point very close to V_{FB} and mostly dependent of the substrate doping.

Another ZTC point is illustrated on 2(a) it can be shown that the bias condition of this point is the same as in the G_g (temperature normalized g_m/I_D parameter) proposed in [13]. Figure 2 illustrates this similarity by presenting $S_T^{C_{Var}}$ 2(a) and $S_T^{G_g}$ 2(b) for two dies of the same PMOS standard V_{th} transistor at temperatures from 27 °C to 200 °C. Both results are obtained from measurement data, voltage derivatives are obtained by Euler differentiation and temperature gradients from a third order polynomial fitting.

B. Active Inductance Temperature Analysis

Active inductances usually do not present an inductive behavior over all biasing, frequency, and temperature, which at first glance may seem like a disadvantage when compared to passive inductors. However, passive inductor integration tends to occupy a large silicon area and does not present the reconfigurability capacity of their active counterparts, the latter being a major disadvantage for VCO's. The differential active inductance presented on Fig. 1 can be represented as a equivalent impedance of a parallel association of a inductor (L_{eq}) with a series resistor (R_s) and a conductance (G_p), where L_{eq},R_s and G_p are given by:

$$L_{eq} = \frac{2(C_{gs1} + C_{gs3})}{g_{ds5}(2g_{m1} + g_{m3} - g_{ds5})} \tag{16}$$

$$R_s = \frac{2(g_{ds5} - g_{m1})}{g_{ds5}(2g_{m1} + g_{m3} - g_{ds5})} \tag{17}$$

$$G_p = \frac{g_{ds5}}{2} \tag{18}$$

As highlighted in (16), the equivalent inductance value is given by 1) transistor capacitance's (C_{gs_1} and C_{gs_3}) and 2) transistor small-signal parameters. The temperature behavior of small-signal parameters can be evaluated by the technique proposed in [13]. However, the temperature sensitivity of the C_{gs} capacitor needs first to be calculated. By taking the temperature sensitivity from (6), one may find:

$$S_T^{C_{gs}} = 2\alpha S_T^{\alpha}\left(\frac{1}{1+2\alpha} + \frac{1}{1+\alpha}\right) + S_T^{q_{IS}}\left(1 - \frac{q_{IS}}{q_{IS}+1}\right) \tag{19}$$

$$S_T^{\alpha} = \frac{q_{ID}S_T^{q_{ID}}}{q_{ID}+1} - \frac{q_{IS}S_T^{q_{IS}}}{q_{IS}+1} \tag{20}$$

The α parameter can be interpreted as the linearity degree from the inversion charge density along the channel whereas it varies from $\alpha \approxeq 1$ in weak inversion and $\alpha \to 0$ in strong inversion. This asymptotic behavior of α entails a more important impact of the overall temperature sensitivity in weak and moderate inversion. Fig. 3(a) and 3(b) show the S_T^{α} for $V_D = 1V$ and $V_D = 0.6V$; it is noticeable that the ZTC point

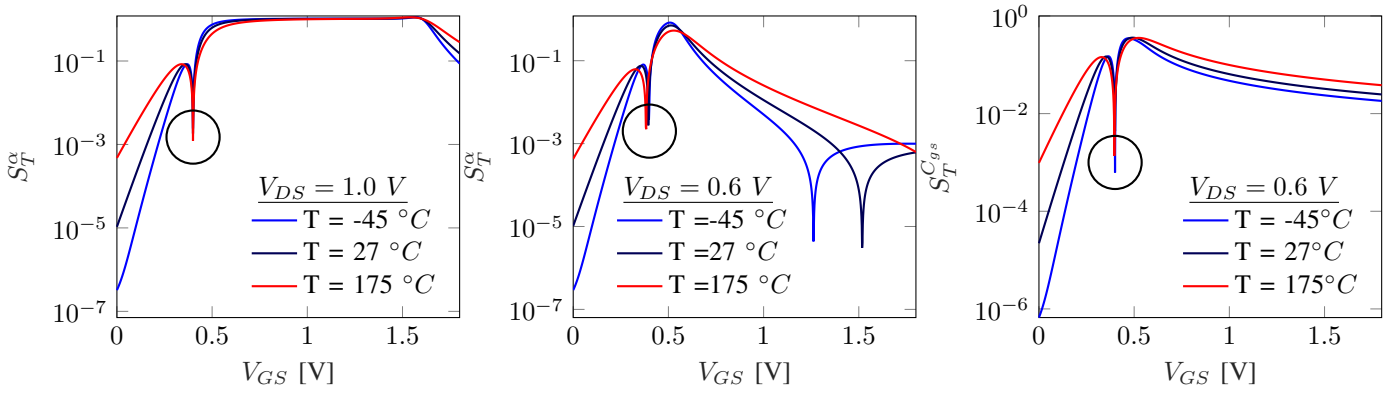


Fig. 3. Extracted sensitivity extracted from UICM model for transistors presenting the same physical parameters as low V_{th} transistor for α at V_D = 1 V (a), α at V_D = 0.6 V and C_{gs} at V_D = 0.6 V (c).

at V_{GB} close to V_{th} indicating a moderate inversion ZTC point. In moderate inversion, the source and drain normalized charges have almost the same value close making α close to unity, and nulling (20). At this condition of $\alpha \approx 1$ and $q_{is} \approx q_{id}$, one may find that the ZTC condition is given by:

$$S_T^{C_{gs}} \approx \frac{V_p \cdot \left(S_T^{V_p} - 1\right)}{\phi_t \left(q_{is} + 1\right)^2}. \tag{21}$$

The same behavior as discussed on Sec. II-A for the total gate capacitance, is found for C_{gs}. The C_{gs} sensitivity is shown in Fig. 3(c). The presence of the same ZTC points indicate a very close relationship between the G_g parameter and the MOSFET capacitors, making it a good starting point to bias transistors in which the capacitance interfere in the quantity of interest (in this case, the equivalent inductance) at this ZTC point.

Biasing transistors M_3 and M_1 ($g_m/I_{D_3} = 7.25$, $g_m/I_{D_1} = 7.15$ at $27°C$) at G_g ZTC, one may find that the equivalent inductance temperature sensitivity reduces to:

$$L_{eq} = \frac{(C_{gs1} + C_{gs3})/{I_D}^2}{(g_{ds}/I_D)_5 (2(g_m/I_D)_1 + r(g_m/I_D)_3 - (g_{ds}/I_D)_5)}, \tag{22}$$

$$S_T^{L_{eq}}(G_{d_5}) = S_T^{C_{tot}(G_{g9}, G_{g10})} - \left(S_T^{G_{d_5}} + \frac{S_T^{G_{g_1}} G_{g_1} - S_T^{G_{g_5}} G_{g_5}}{G_{g_1} - G_{g_5}}\right) + 2 - 2S_T^{J_{ds}}, \tag{23}$$

where I_D is the drain current of transistors M_1 and M_3; r the ratio between I_{D_5} and I_{D_3}. Even though, most of low-temperature sensitivity circuits rely on the ZTC biasing of all its components, a VCO requires a bias changing for frequency selection. For this matter, one may bias M_1 and M_3 on G_g ZTC and evaluate the change of mean, max and min temperature sensitivity of L_{eq} over V_{ctrl1}.

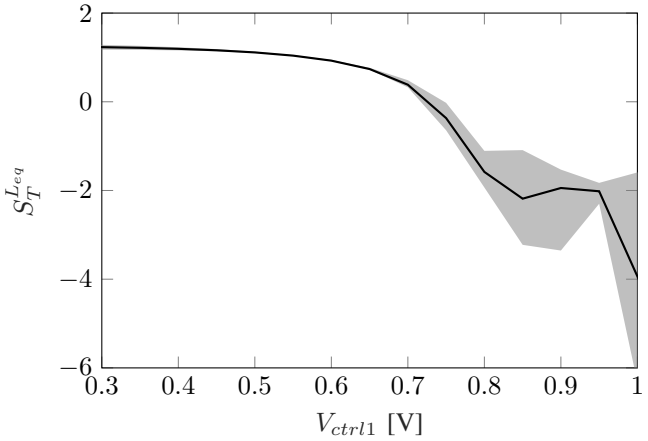


Fig. 4. Active Inductance equivalent inductance range (gray) and mean(solid) at different control voltages and temperature from -40 °C to 200 °C.

Fig. 4 illustrates the equivalent inductance sensitivity range from temperatures ranging from -40 °C to 175 °C. This figure shows a ZTC point of the average temperature sensitivity at $V_{ctrl1} \geq 0.7$ V. However by biasing M_5 in ZTC, the VCO loses its frequency control characteristics. Fig 4 show also an almost constant temperature sensitivity around 1.3 in the region from V_{ctrl1} between 0.3 and 0.6 V. This constant temperature sensitivity can be compensated by the C_{var} temperature sensitivity using (3) to achieve a frequency ZTC point and still allow for VCO control.

III. Results

To achieve F_{osc} ZTC while maintaining tuning range, the active inductance was biased with G_g ZTC for transistors M_1 and M_3, and the MOS varicap was biased with a V_{ctrl2} of 1.3 V, making the V_{BG} equal 0.4 V when the source voltage is $V_{DD}/2$ and temperature sensitivity is -1.3. The maximum real part of the equivalent impedance seen from the parallel of C_{var}

and L_{active} is shown on the Fig. 5, post-layout simulation results achieving a maximum value of 600 Ω.

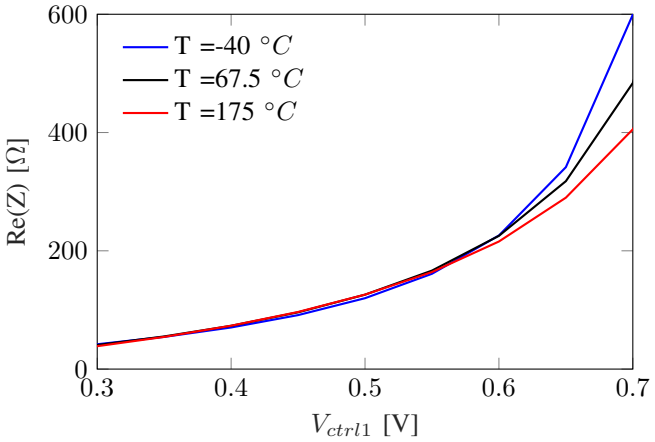


Fig. 5. PSL Real Part from active inductance impedance for V_{ctrl1} at the tuning range and different temperatures.

The G_{comp} network was designed to have a negative resistance bigger than 600 Ω ($g_m/I_{D_7} = 5.95$ at $27°C$) and the M_{10}, M_9 ($W \times L = 200\mu m \times 300nm$) sizes were adjusted for L-Band range. Fig. 6 presents the oscillation frequency and the temperature variation of the circuit.

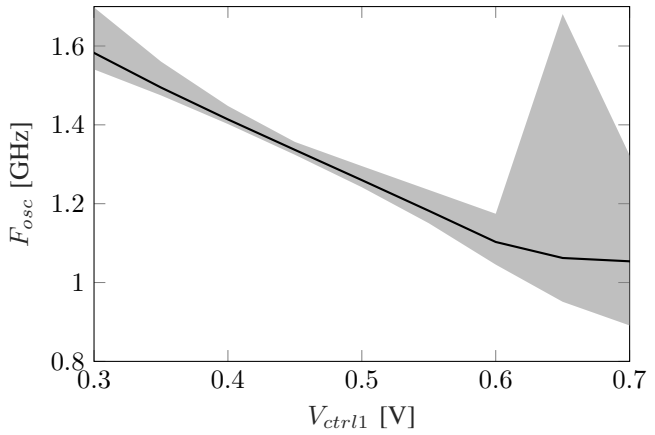


Fig. 6. PSL Oscillation frequency range (gray) and mean(solid) at different control voltages and temperature from -40 °C to 175 °C.

The frequencies presented in Fig. 6 are designed for a 10% head-up in order to account for the latter parasitic capacitors on the layout. The final circuit layout is presented in Fig. 7 having an area of 163.5 x 190 μm^2.

In order to compare the temperature-aware design with the proposition in [11], Fig. 8 shows the temperature coefficient of the circuit from [11] called "Traditional"($g_m/I_{D_1} = 9.9$, $g_m/I_{D_3} = 9.8$, $g_m/I_{D_7} = 7.8$ at $27°C$) and the results presented in this paper.

The presented work shows an overall zero temperature coefficient, with a temperature coefficient reduction between 2.62 to 9.84 times better than the more traditional design and a mean temperature coefficient of 237.8 ppm/°C. For

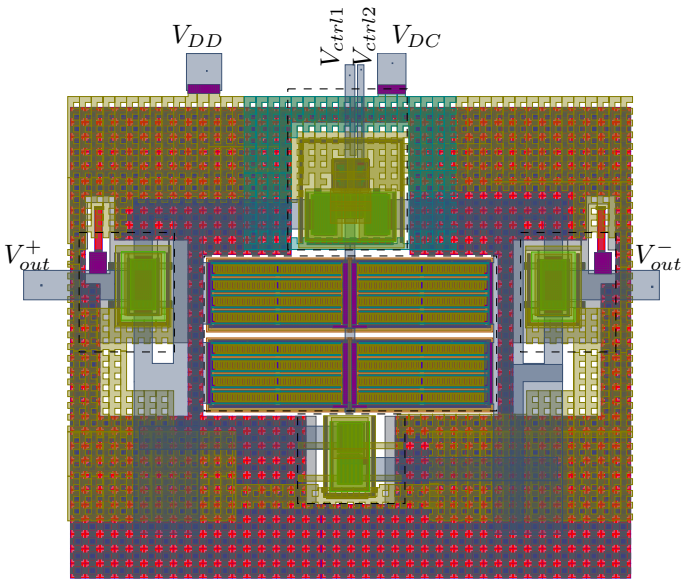


Fig. 7. Temperature-Aware VCO Layout presenting an area of 163.5 x 190 μm^2.

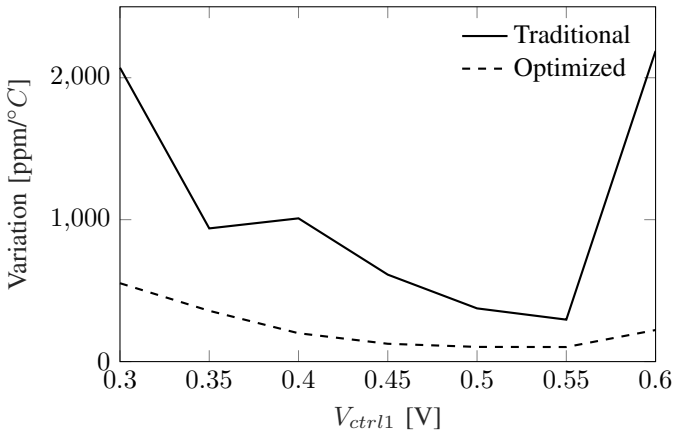


Fig. 8. Frequency Temperature coefficient comparison between [11] and this work.

impedance matching two common-source output buffers with 50 Ω drain P+ non-salicided poly resistors presenting its 40 ppm/°C resistance temperature coefficient, see details in Fig. 7. Power supply planes were made to decrease line resistance and increase bypass capacitance. All trace widths were constructed to minimize electromigration effects. It is important to point out that the traditional circuit does meet the oscillation condition for some V_{ctrl2} values at low-temperature and low V_{ctrl1} or high-temperature and high V_{ctrl1}.

To evaluate the process and mismatch variations and their consequences on the circuit temperature behavior, a 41 points Monte-Carlo simulation was made for 9 V_{ctrl1} points and 11 temperature points, in a total of 4059 simulations. Since this works goal is to acount for reliability all results will be presented on the worst-case Monte Carlo points. The mean

3σ variation over temperature and the maximum frequency temperature variation is shown in Fig. 9.

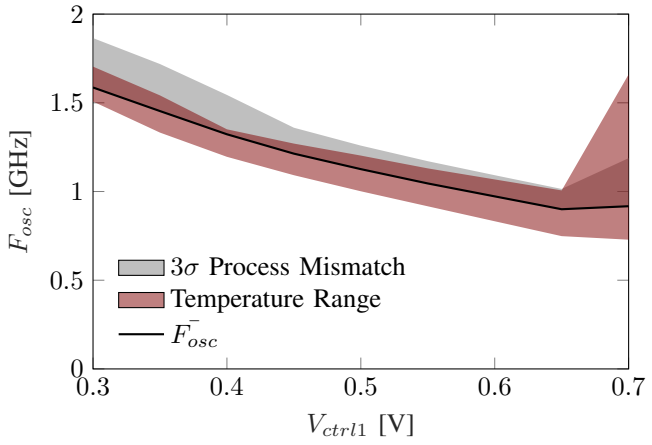


Fig. 9. Monte Carlo Results for the oscillation Frequency of the proposed VCO.

The Monte-Carlo results show a temperature variation smaller than the mean 3σ variation compatible with electric simulations indicating that the temperature awareness is kept even with process and mismatch variations. The final VCO present a worst case phase-noise of -60 dBc/Hz at a 100 kHz frequency offset, a worst case power consumption varying from 70 mW to 54 mW and a negative temperature coefficient. Since, the oscillator is target to be used in a transmitter, where it will operate in only one frequency per transmission, the figure of merit is given by:

$$\text{FOM} = \left| L(\Delta f) + 20\log\left(\frac{\Delta f}{f_0}\right) + 10\log\left(\frac{P}{1mW}\right)\right|, \quad (24)$$

where $L(\Delta f)$ is the phase noise with a frequency offset of Δf; f_0 is the oscillation frequency; and P the power consumption. The circuit presents a mean FOM over temperature and control voltage of 131 dB. Since the phase noise varies largely with temperature the mean FOM over temperature present a worst case value taken at 27 $^\circ C$ of 146 dB. The typical FOM values are compatible with the state of art.

IV. Conclusion

A low-temperature coefficient VCO suitable for L-band on aeronautical temperature range was proposed. The proposed circuit presents a mean temperature coefficient of 237.8 ppm/$^\circ C$ from -40 $^\circ C$ to 175 $^\circ C$ and V_{ctrl1} from 0.3 V to 0.6 V range. A circuit design was presented using a g_m/I_D methodology and can be adapted to other frequency ranges by sizing the circuit's varicap. This is the first demonstration of a temperature-independent oscillation frequency for an extended temperature range suitable for harsh environments applications to the best of our knowledge.

V. Acknowledgment

The authors would like to thank Rachid Hamani for the provided measurement data, that without it, the presented results would not be possible in this work.

References

[1] J. D. Cressler and H. A. Mantooth, Eds., *Extreme Environment Electronics*, 1st ed. CRC Press, Dec. 2017.

[2] R. Johnson, J. Evans, P. Jacobsen, J. Thompson, and M. Christopher, "The Changing Automotive Environment: High-Temperature Electronics," *IEEE Trans. Electron. Packag. Manufact.*, vol. 27, no. 3, pp. 164–176, Jul. 2004.

[3] C. Buttay, D. Planson, B. Allard, D. Bergogne, P. Bevilacqua, C. Joubert, M. Lazar, C. Martin, H. Morel, D. Tournier, and C. Raynaud, "State of the art of high temperature power electronics," *Materials Science and Engineering: B*, vol. 176, no. 4, pp. 283–288, Mar. 2011.

[4] A. Ottaviani, P. Palacios, T. Zweipfennig, M. Alomari, C. Beckmann, D. Bierbusse, J. Wieben, J. Ehrler, H. Kalisch, R. Negra, A. Vescan, and J. N. Burghartz, "Evaluation of High-Temperature High-Frequency GaN-Based LC-Oscillator Components," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4587–4591, Nov. 2020.

[5] Z. Schwartz and G. Ponchak, "1-GHz, 200/spl deg/C, SiC MESFET Clapp oscillator," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 11, pp. 730–732, Nov. 2005.

[6] K. Shanmugalingam, D. Liyanagama, R. Rubanathan, and S. Thayaparan, "Temperature Sensing and Data Transmission Mechanism for High Temperature Applications," in *2019 1st International Conference on Electrical, Control and Instrumentation Engineering (ICECIE)*, Nov. 2019, pp. 1–7.

[7] D. D. Shin, D. B. Heinz, H.-K. Kwon, Y. Chen, and T. W. Kenny, "Lateral diffusion doping of silicon for temperature compensation of MEMS resonators," in *2018 IEEE International Symposium on Inertial Sensors and Systems (INERTIAL)*. Moltrasio: IEEE, Mar. 2018, pp. 1–4.

[8] Q. Liu and C. Chai, "A 1.8 GHz temperature drift compensated LC-VCO for RFID transceiver," *Analog Integr Circ Sig Process*, vol. 105, no. 1, pp. 7–12, Oct. 2020.

[9] K. Okuno, K. Masaki, S. Izumi, T. Konishi, H. Kawaguchi, and M. Yoshimoto, "A 2.23 ps RMS jitter 3 Ms fast settling ADPLL using temperature compensation PLL controller," in *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Dec. 2014, pp. 68–71.

[10] S. Lu and Y. Liao, "A Low-Power, Differential Relaxation Oscillator With the Self-Threshold-Tracking and Swing-Boosting Techniques in 0.18- μ m CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 2, pp. 392–402, Feb. 2019.

[11] L. Lu, H. Hsieh, and Y. Liao, "A Wide Tuning-Range CMOS VCO With a Differential Tunable Active Inductor," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 9, pp. 3462–3468, Sep. 2006.

[12] J. Martins, E. Avignon-Meseldzija, and P. Maris Ferreira, "Temperature-Aware gm/ID-based Methodology for Active Inductor Design," in *São Paulo*, vol. 9, São Paulo, 2019, p. 6.

[13] J. Martins, A. Mostafa, J. Juillard, R. Hamani, F. Alves, and P. M. Ferreira, "A Temperature-Aware Framework on gm/ID-Based Methodology using 180 nm SOI from -40 ∘C to 200 ∘C," *IEEE Open J. Circuits Syst.*, pp. 1–1, 2021.

[14] M. Siniscalchi, "On the design of ultra low voltage CMOS oscillators," Ph.D. dissertation, Montevideo : Udelar. FI. IIE., 2020.