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Modeling of Fermi-Level Pinning Alleviation With MIS Contacts: n and pMOSFETs Cointegration Considerations—Part I

Julien Borrel, Louis Hutin, Olivier Rozeau, Marie-Anne Jaud, Sébastien Martinie, Magali Gregoire, Emmanuel Dubois, and Maud Vinet

***Abstract*— Aiming at overcoming the Fermi-level pinning (FLP) occurring at the metal/semiconductor interfaces, metal/insulator/semiconductor (MIS) contacts to n-Si and p-Si are usually treated in separate optimization studies, yet with no particular insight on their technological compatibility. In this paper, using 1-D analytical modeling of MIS contacts, it is shown that in order to fully benefit from FLP mitigation on both n- and p-type Si, a single-insertion/single-metallization scheme cannot be considered. In addition, it is demonstrated that associating given numerical values of contact resistivity with MIS contacts results in a thorny problem, since their I–V characteristics are nonsymmetric nonlinear.**

***Index Terms*— 1-D modeling, CMOS, metal/insulator/semiconductor (MIS) contacts, nFET and pFET cointegration, T_{WKB} approximation.**

I. Introduction

As we reach the end of the scaling years, the development of the ultimately scaled digital logic CMOS nodes is no longer driven by the gate length (L_{gate}) shrinking. The contacted poly pitch (CPP) scaling is reflected on the contact length (T_{cont}) decrease rather than on that of L_{gate} in order to preserve well-behaved MOSFET characteristics as well as a reliable operation.

As a consequence, meeting the performance requirements for the upcoming MOSFET generations implies the addition of a key enabling process integration booster in order to decrease the contact resistance value while simultaneously scaling the contact surface area. As a matter of fact, as shown in Fig. 1(a) [1], reducing CPP while keeping a specific contact resistivity (ρ_c) of 10^{-8} $\Omega \cdot \mathrm{cm}^2$ would make the contact resistance a major contribution of the total access resistance. According to ITRS 2013 [2], ρ_c of about 10^{-9} $\Omega \cdot \mathrm{cm}^2$ is required to ensure no significant degradation of the future nodes performance.

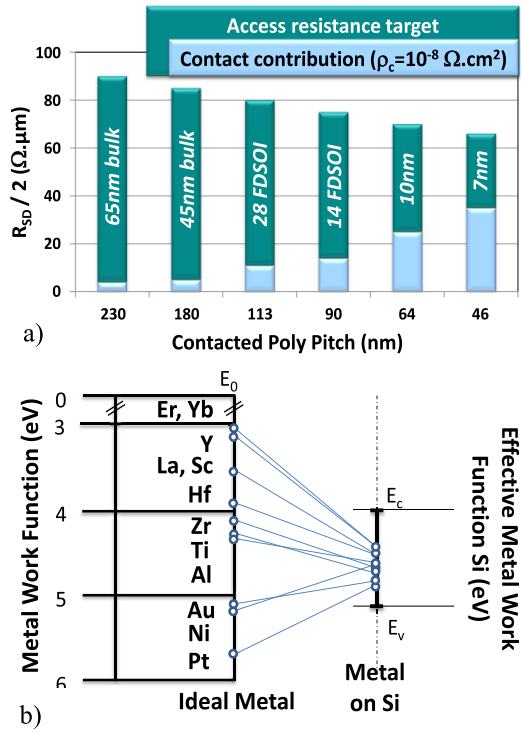

Fig. 1. (a) Access and contact resistance versus CPP assuming a contact resistivity of 10^{-8} $\Omega\mathrm{cm}^2$ [1]. (b) Reference metal work functions and their effective value on Si due to FLP [3].

However, due to Fermi-level pinning (FLP), most of the metals used in the microelectronics today, including Ni-based silicide, feature an effective metal work function almost independent of their reference value when contacted to silicon [Fig. 1(b)] [3]. This phenomenon hinders the proper optimization of the Schottky barrier height (SBH) at the interface and the induced depletion region which extends in Si. Lowering

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the contact resistivity can thus be achieved either by making this depletion region narrower or by mitigating the FLP.

The former can be performed using pulsed laser annealing. Allowing a 2-D uniform surface annealing, this process is expected to provide locally higher temperatures without damaging the underlying layers [4]. This would lead to the better ion implantation damage recovery and the higher dopant activation, hence enabling to stay within the silicidation paradigm i.e., tunneling through a tall but narrow Schottky barrier [5]. Recently, combining dopant activation by pulse laser annealing with Ge amorphization of the source and drain prior to the silicidation, the record low ρ_c of 1.5×10^{-9} $\Omega \cdot \text{cm}^2$ was obtained [6].

The latter approach based on alleviating the FLP could consist in inserting a dielectric layer between the metal and the semiconductor of the contacts [7], thus forming metal/insulator/semiconductor (MIS) junctions. Recently, the studies of subnanometric TiO_x insertions ([8], [9]) have shown promising results on n-type Si with the reports of contact resistivity values equivalent to, respectively, 3.12×10^{-8} and 9.1×10^{-9} $\Omega \cdot \text{cm}^2$. Yet it seems that most of the efforts thus far were focused on enhancing the symmetry of MIS contacts I–V on a [−1 V, +1 V] range; whereas the actual drop across MOSFET contacts should typically be at least an order of magnitude lower. Moreover, most of the previous studies intended to reduce the equivalent dc contact resistivity of stand-alone contact, with no insight on the constraints when cointegrating contacts to n- and p-Si as required in the CMOS technology.

In this paper, following on partially from our previous work [10], a protocol is presented in order to generate 1-D analytically simulated J–V characteristics of MIS contacts. After presenting the main features of this protocol, such J–V characteristics are performed for various metallizations and insertions on both n- and p-Si.

II. 1-D Analytical Algorithm

In order to simulate the dc performance of stand-alone n- and p-Si MIS contacts, J–V diode characteristics were analytically simulated. The calculation of the current density as a function of the contact bias (J–V) was performed using the algorithm described in Fig. 2.

A. Fermi-Level Pinning Mitigation

The FLP occurring at the metal/semiconductor (M/S) interface was found to be related to the density of states induced in the bandgap of the semiconductor. The physical origin of these states has been explained by the penetration of the tail of the metal electrons wave functions in the gap [11], hence the name of metal-induced gap states (MIGSs).

In order to calculate the effective work function of the contact metal, the FLP mitigation was evaluated via an MIGS attenuation model described initially by Monch [12]. This model was shown to predict results similar to those found experimentally and was more recently extended to MIS contacts on Ge in [13]. According to it, the density of MIGS at the

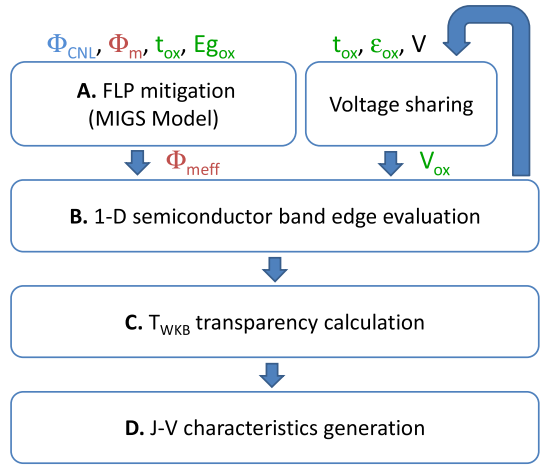

Fig. 2. Algorithm used for J–V calculations. The MIGSs attenuation-based FLP alleviation and the SBH image force lowering were considered.

metal/material (dielectric or semiconductor) interface is given in the following:

$$D^0_{\text{MIGS}} = \frac{2}{\pi a^2_{\text{Mat}} E_{\text{gMat}}} \tag{1}$$

where a_{Mat} is the lattice parameter of the material contacted to the metal and E_{gMat} is its energy bandgap. The metal electrons penetrating in the adjacent material as evanescent waves, the density of MIGS is expected to fall off exponentially with a characteristic decay length given in the following:

$$\delta_{\text{Mat}} = \frac{h^2}{2\pi m_0 a_{\text{Mat}} E_{\text{gMat}}} \tag{2}$$

where m_0 is the free electron mass and h is Planck's constant. The density of MIGS at a distance t from the interface is then given in the following:

$$D_{\text{MIGS}}(t) = D^0_{\text{MIGS}} e^{-\frac{t}{\delta_{\text{Mat}}}}. \tag{3}$$

When the metal is directly contacted to the semiconductor, the density of MIGS at the M/S interface can be evaluated by applying (1) with the parameters of the considered semiconductor. Contrastively, when a dielectric layer (noted IL below) is inserted between the metal and the semiconductor, a first drop of the MIGS density is observed in the insertion. Therefore, the actual density remaining at the insulator/semiconductor interface can be obtained by substituting the dielectric insertion thickness t_{IL} in (3). As an illustration, the densities of MIGS at the Si surface in the cases of TiO_2, Si_3N_4, and Al_2O_3 insertions are shown in Fig. 3. Considering (2), one can notice that the decay length of the MIGS density is inversely related to the bandgap of the dielectric insertion. Therefore, the interlayers with large E_g lead to better FLP mitigation for a given thickness. The numerical bandgap values used in this paper are taken from [13] and are represented in Fig. 4, positioned relatively to the bandgap of silicon.

Those MIGSs are responsible for the generation of an interface charge in the bandgap of energy of the semiconductor which is not taken into account in the ideal Schottky–Mott rule. Therefore, solving the Gauss law at the interface while

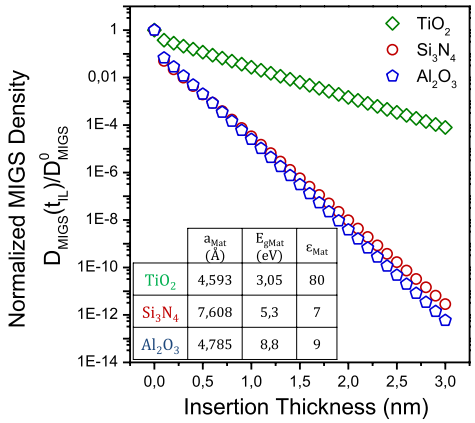

Fig. 3. Normalized MIGSs density at the Si surface depending on the insertion nature and thickness.

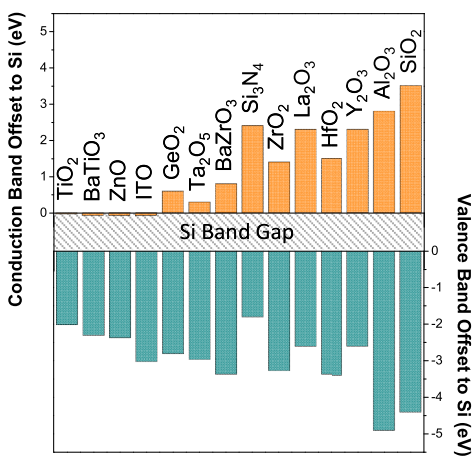

Fig. 4. Dielectric energy bandgaps referenced to the gap of Si. This bar chart materializes the conduction and VBOs of the dielectrics insertions [13].

considering this additional charge [12] results in expressing the metal work function as an effective one as presented in the following:

$$\phi_M^{\text{eff}} = S\phi_M + (1-S)\phi_{\text{CNL}}^{\text{Si}} \tag{4}$$

where ϕ_M is the ideal metal work function and $\phi_{\text{CNL}}^{\text{Si}}$ is the charge neutrality level in Si considered equal to 4.87 eV counted down from the vacuum level E_0 in this paper. S is referred as the resulting FLP factor and is given in the following:

$$S = \left(1 + q^2 \frac{D_{\text{MIGS}}(t_{\text{IL}}) \times (\delta_{\text{Si}}\varepsilon_{\text{IL}} + t_{\text{IL}}\varepsilon_{\text{Si}})}{\varepsilon_0(\varepsilon_{\text{IL}} \times \varepsilon_{\text{Si}})}\right)^{-1} \tag{5}$$

where q is the electronic charge, ε_0 is the vacuum permittivity, ε_{IL} is the relative permittivity of the interlayer, and ε_{si} is the relative permittivity of Si.

B. 1-D Semiconductor Band Edge Evaluation

In Section II.B, equations are presented for the case of an n-type Si substrate. For the sake of simplicity, the case of p-Si is not exposed. Nevertheless, similar development can be applied to both configurations.

Once the effective metal work function is obtained, the effective contact potential difference $\Delta\phi^{\text{eff}}$ is evaluated using the following:

$$\Delta\phi^{\text{eff}}(V) = \phi_M^{\text{eff}} - \phi_{\text{Si}} + V \tag{6}$$

where ϕ_{Si} is the work function of Si and V is the bias applied between the metal and the semiconductor i.e., the contact bias.

This overall effective contact potential leads to a voltage sharing between the dielectric insertion and the semiconductor. As summed up in (7), the part dropped in the semiconductor causes the appearance of a charge at the IL/S interface which in turn establishes a voltage drop within the interlayer. Therefore, this problem is self-consistent and was solved using a proper module in the analytical algorithm.

$$\begin{cases} V_{\text{Si}} = \Delta\phi^{\text{eff}}(V) - V_{\text{IL}} \\ V_{\text{IL}} = \frac{t_{\text{IL}}}{\varepsilon_{\text{IL}}} Q_{\text{Si}} \\ Q_{\text{Si}} = F(V_{\text{Si}}) \end{cases} \tag{7}$$

where V_{Si} is the voltage drop in Si, V_{IL} is the voltage drop in the IL, and Q_{Si} is the surface charge at the IL/S interface. By solving Poisson's equation [14], the surface charge appears to be related to the voltage drop in Si via the F function presented in the following (8), as shown at the bottom of this page, where L_{Debye} is the Debye length, n_i is the intrinsic carrier concentration, and N_d is the doping concentration.

Solving the voltage sharing gives the actual voltage drop in the dielectric layer, the surface charge density in Si, and finally the resulting SBH in Si. This allows to generate the 1-D band structure of the contact as a function of the applied contact bias, the oxide thickness and the doping concentration of the semiconductor.

C. T_{WKB} Transparency Calculation

Once the energy band edge profile of the MIS junction is established, it is possible to calculate the transmission coefficient for each energy level using a T_{WKB} (Wentzel–Kramers–Brillouin) approximation, as shown in the following:

$$T_{\text{WKB}}^{\text{IL}}(E,V) = \begin{cases} e^{-2\int_{\text{IL}}\sqrt{\frac{2m_*^{\text{IL}}\left(E_C^{\text{IL}}(V,x)-E\right)}{\hbar^2}}dx} & \text{if } E < E_C^{\text{IL}}(V,x) \\ 1 & \text{if } E \geq E_C^{\text{IL}}(V,x) \end{cases} \tag{9}$$

$$T_{\text{WKB}}^{\text{Si}}(E,V) = \begin{cases} e^{-2\int_{\text{Si}}\sqrt{\frac{2m_*^{\text{Si}}\left(E_C^{\text{Si}}(V,x)-E\right)}{\hbar^2}}dx} & \text{if } E < E_C^{\text{Si}}(V,x) \\ 1 & \text{if } E \geq E_C^{\text{Si}}(V,x). \end{cases} \tag{10}$$

$$F(V_{\text{Si}}) = \frac{\sqrt{2}\varepsilon_{\text{IL}}kT}{qL_{Debye}}\sqrt{\frac{n_i^2}{N_d^2}\left[e^{\frac{q(V_{\text{Si}})}{kT}} - \frac{q(V_{\text{Si}})}{kT} - 1\right] + \left[e^{-\frac{q(V_{\text{Si}})}{kT}} + \frac{q\,(V_{\text{Si}})}{kT} - 1\right]} \tag{8}$$

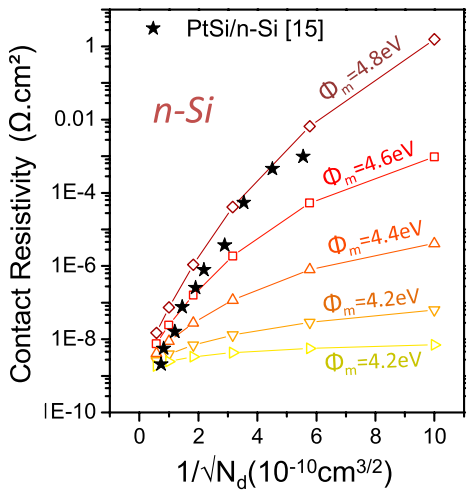

Fig. 5. Contact resistivity to n-Si as a function of the doping concentration for (colored) simulated system presenting various metal work functions for an extraction bias of 1 V, and (black stars) experimental PtSi/n-Si system [15].

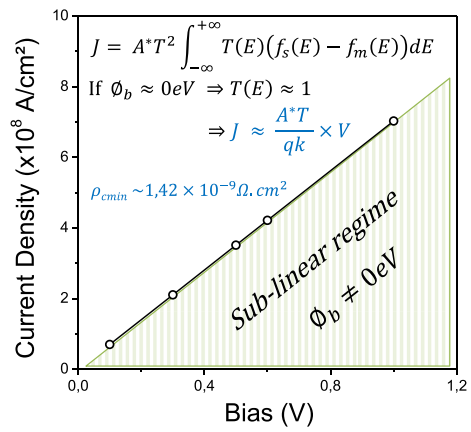

Fig. 6. Forward current density as a function of the bias voltage for an unpinned metal-based contact without any insertion. Inset: TWKB approximation applied for an ideal zero-barrier contact leading to fundamental contact resistivity limit.

For a given energy, the carriers can encounter the dielectric (9) and the depletion region in the Si (10) as a barrier. These two cases have been treated separately by splitting the total transparency in two spatial domains corresponding to each material and by considering proper tunneling masses m_* [14]. The resulting transparency is given by the product of the tunneling probabilities

$$T_{\mathrm{WKB}}^{\mathrm{Tot}}(E,V) = T_{\mathrm{WKB}}^{\mathrm{IL}}(E,V) \times T_{\mathrm{WKB}}^{\mathrm{Si}}(E,V). \tag{11}$$

D. J–V Characteristics Generation

The algorithm described in the previous parts allows the evaluation of the current density as a function of the applied voltage by using the following:

$$J(V) = \int_{-\infty}^{+\infty} \frac{A^* T}{k} T_{\mathrm{WKB}}^{\mathrm{Tot}}(E,V)(f_{\mathrm{Si}}(E,V) - f_{\mathrm{Met}}(E,V))dE \tag{12}$$

where A^* is the Richardson constant in which the densities of states are lumped, f_{Si} is the Fermi–Dirac distribution in the Si, and f_{Met} is the Fermi–Dirac distribution in the metal.

In order to evaluate the relevance of our simulation, the contact resistivity of silicon-based insertion free contact was evaluated as a function of the substrate doping concentration and the effective metal work function. The results are shown in Fig. 5 along with experimental measurements of a PtSi/n-Si contact taken from [15]. The PtSi metal work function varying between 4.8 and 5.1 eV depending on the fabrication process conditions [16], simulated results seem consistent with the experimental values.

The ideal case of zero barrier contact without insertion was simulated using the algorithm. The results obtained for a forward biasing are presented in Fig. 6. The minimum contact resistivity was found to be equal to 1.42×10^{-9} $\Omega \cdot \mathrm{cm}^2$ for an n-type Si substrate. As shown in Fig. 6 (inset), the same value can be found by simplifying the supply function difference by a rectangular function equal to 1 between the Fermi level of the metal and that of the Si and equal to zero otherwise; and by assuming a $T_{\mathrm{WKB}}(E,V)$ value of 1 due to the lack of barrier. Therefore, using this simplified model, the value of $\rho c = 10^{-9}$ $\Omega \cdot \mathrm{cm}^2$ appears to be the fundamental limit value of the contact resistivity scaling in Si. However, it has to be noted that using full band ballistic quantum transport approach, the intrinsic lower limit of contact resistivity in 10^{20} at/cm^3 doped n-Si was actually found to be around 2×10^{-10} $\Omega \cdot \mathrm{cm}^2$ [17].

III. J–V Characteristics Generation

Using the algorithm described earlier, J–V plots were thus generated for Ti and Ti/TiO_2 layers on top of p- and n-type Si considering, respectively, a doping concentration of $N_a = N_d = 10^{20}$ at/cm^3, as presented in Figs. 7 and 8. The reference cases of perfectly linear ohmic contacts with $\rho c = 10^{-7}$ $\Omega \cdot \mathrm{cm}^2$, $\rho c = 10^{-8}$ $\Omega \cdot \mathrm{cm}^2$, and $\rho c = 10^{-9}$ $\Omega \cdot \mathrm{cm}^2$ are also plotted along in Figs. 7 and 8.

One can notice that the Ti liner contacts are slightly better on p-type Si due to the FLP being closer to the valence band [Fig. 1(b)]. Yet, Ti being an n-type metal [Fig. 1(b)], the FLP alleviation allowed by the TiO_2 insertion results in a current increase on n-type Si but diminishes the conductivity of the contact on the p-type substrate.

Therefore, in order to fully benefit from the FLP mitigation on both n- and p-type Si, a dual metallization was considered. The Pt/TiO_2(5Å)/p-Si J–V characteristic was generated and is plotted along with the former ones in Fig. 8. Despite the Pt work function being more adapted to p-Si, the TiO_2 valence band offset (VBO) (Fig. 4) induces a significant tunnel resistance for holes leading to a poor current i.e., below that of the $\rho c = 10^{-7}$ $\Omega \cdot \mathrm{cm}^2$ reference.

As a consequence, regardless of the negative impact on the process complexity, the optimal configuration was thus to consider a dual metallization on the top of a dual dielectric insertion. J–V characteristics of Pt/Si_3N_4(5Å)/p-Si and Zr/TiO_2(15Å)/n-Si were thus generated and are added in Figs. 7 and 8. Despite the reduction of VBO obtained by replacing TiO_2 by Si_3N_4, the resulting optimal MIS contact

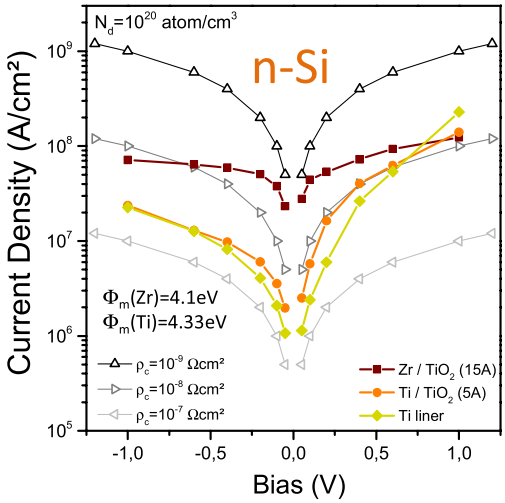

Fig. 7. J–V characteristics for n-type-based contacts presenting Ti and Zr metallizations with TiO2 interlayer.

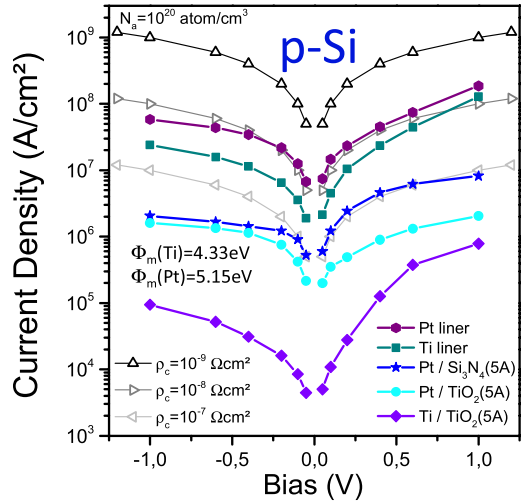

Fig. 8. J–V characteristics of p-type-based contacts presenting Ti and Pt metallizations with various interlayer natures and thicknesses. The scale is different form Fig. 5.

on p-type semiconductor has still poor contact properties. By extension, considering the VBO in Fig. 4, using any of the other insertions represented on this graph on p-type Si would irrevocably lead to poor contact conductivity.

Therefore, the J–V characteristic curve of a contact consisting of a Pt liner directly on p-Si was simulated and is added to Fig. 8. Despite a nonmitigated FLP, the 0.82 eV difference between Ti and Pt nominal work functions induces a nonnegligible effective work functions difference between these two metallizations. The resulting effective SBH is consequently lowered leading in turn to a significant increase in current density.

It is worth noting that inserting a dielectric layer between the metal and the semiconductor not only acts on the contact conductivity but also on its symmetry. When applying a positive bias, the Si being in the accumulation regime features a significant surface charge. Considering (7) i.e., the self-consistent voltage sharing between the Si and the dielectric, this surface charge results in an extensive voltage drop in the dielectric, as shown in Fig. 9. Consequently, the actual bias applied to the Si which is responsible to the band bending and the carrier injection is found to be only a fraction of the applied bias. Notably, the Pt/TiO_2(5Å)/p-Si contact features a forward current lower that its reverse one. To the best of our knowledge, this can only occur in MIS contacts.

Finally, by looking at Figs. 7 and 8, the optimal cointegration configuration emerging from the analytical simulations is Pt/p-Si and Zr/TiO_2(15Å)/n-Si. On can notice that the comparison of this optimum with the ideal ohmic references is not straightforward. As a matter of fact, some contacts may appear to perform poorly at first glance on a [-1 V, $+1$ V] interval, yet feature very low resistivity at low biases. For example, Zr/TiO_2(15Å)/n-Si contact has a conductivity close to the $\rho c = 10^{-8}\ \Omega \cdot \mathrm{cm}^2$ reference at $+1$ V while it appears to be closer to the $\rho c = 10^{-9}\ \Omega \cdot \mathrm{cm}^2$ ideal ohmic contact around zero. For this reason, it seems that associating a given contact resistivity to such nonlinear nonsymmetric contacts is a sensitive problem.

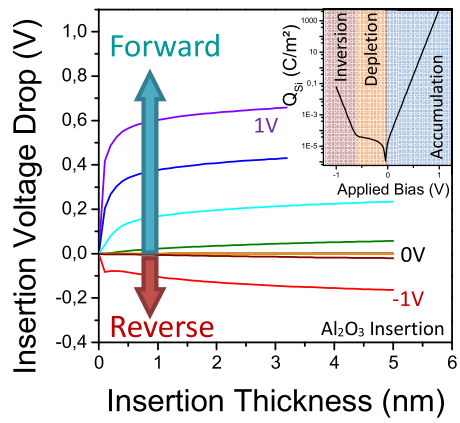

Fig. 9. Voltage drop occurring in the Al2O3 insertion as a function of the insertion thickness and the applied bias. Inset: semiconductor surface charge as the function of the applied bias. The insertion voltage drop is linked to the surface charge, and thus is more important in the accumulation regime.

IV. Conclusion

The study of the MIS contacts cointegration on both n- and p-type Si was carried out. Because of 1-D analytical simulations, it was found that no MIS contact configuration enabled conductivity improvement on p-type Si compared with a Ti liner contact reference. Even a change in metallization scheme was found to be inefficient on p-Si if associated with a dielectric insertion, since their theoretical VBO to Si were too important. Therefore, the optimal contact on p-Si was found to perform roughly around ideal $10^{-8}\ \Omega \cdot \mathrm{cm}^2$ ohmic contact. However, the optimal junction on n-type Si was found to include a dielectric insertion and was approximately equivalent to a $10^{-9}\ \Omega \cdot \mathrm{cm}^2$ ohmic contact around 0 V approaching the resistivity value recommended by the ITRS.

Nevertheless as stated previously, these junctions J–V characteristics are neither perfectly linear nor symmetrical in a [-1 V, $+1$ V] range of bias. For this reason, it seems to be tricky to associate a given contact resistivity with

such junctions. To do so, one needs at least to provide the extraction bias of this resistivity. To be relevant, this bias of extraction should ideally match the effective operative bias the contact encounter when contacting to a MOSFET.

Nevertheless, finding this bias arises from solving the voltage sharing between contacts and MOSFET when applying a supply voltage V_{dd}. This problem boils down to treating diodes and resistors in series, which is famously known to be a self-problem. This problem can be solved using SPICE simulation and is discussed in part 2 of this paper [18]. Elementary SPICE compact models are fitted on the previously presented analytically simulated I–V characteristics and then wired on each side of 10-nm p and nMOSFET SPICE blocks. The efficiency of the MIS contacts to improve the conductive property is thus evaluated via their impact on dc and ac performances.

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