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Modeling of Fermi-Level Pinning Alleviation With MIS Contacts: n and pMOSFETs Cointegration Considerations—Part II

Julien Borrel, Louis Hutin, Olivier Rozeau, Marie-Anne Jaud, Sebastien Martinie, Magali Gregoire, Emmanuel Dubois, and Maud Vinet

Abstract—In this paper, the insertions of dielectric in metal/insulator/semiconductor contacts are considered via their associated impact on the dc and ac performances. Based on dc output characteristics projections, we found that single insertion and/or single-metal integration schemes are unlikely to result in simultaneously successful Fermi-level pinning alleviation on both n and pFETs. We show that the added C_{MIS} contributes to a significant extra improvement in terms of intrinsic inverter delay. In particular, an optimal configuration consisting of Pt-liner/p-Si and Zr/TiO₂(15Å)/n-Si contacts can lead to a ring oscillator frequency higher than that of p and nFETs each flanked by ideal ohmic contacts with $10^{-9} \Omega \cdot \text{cm}^2$ resistivity.

Index Terms—Metal/insulator/semiconductor (MIS) contacts, n and pFETs cointegration, ring oscillators (ROs) frequency.

I. INTRODUCTION

MEETING the performance requirements for the upcoming MOSFET generations implies the addition of a key enabling process integration booster in order to decrease the contact resistance value while simultaneously scaling the contact surface area.

As a matter of fact, reducing the contacted poly pitch while keeping a specific contact resistivity (ρ_c) of $10^{-8} \Omega \cdot \text{cm}^2$ induces a significant increase of the contribution of the contact resistance in the total access resistance [1]. According to the International Technology Roadmap for Semiconductors (ITRS) 2013 [2], obtaining ρ_c of about $10^{-9} \Omega \cdot \text{cm}^2$ has to be achieved to ensure future nodes performances.

L. Hutin, O. Rozeau, M.-A. Jaud, S. Martinie, and M. Vinet are with University Grenoble Alpes, Grenoble 38000, France, and also with the Commissariat à l'Énergie Atomique-Laboratoire d'Électronique des Technologies de l'Information, Grenoble 38054, France (e-mail: louis.hutin@cea.fr; olivier.rozeau@cea.fr; marie-anne.jaud@cea.fr; sebastien.martinie@cea.fr; maud.vinet@cea.fr).

E. Dubois is with the Centre National de la Recherche Scientifique, Institut d'Électronique, de Microélectronique et de Nanotechnologie, Villeneuve-d'Ascq 59652, France (e-mail: emmanuel.dubois@isen.iemn.univ-lille1.fr).

However, Fermi-level pinning (FLP) prevents proper optimization of the Schottky barrier height at most of the metal/semiconductor (MS) interfaces [3]. Therefore, lowering the contact resistivity has to be achieved by either making the induced depletion region narrower or by mitigating the FLP.

For current silicided contact, the former can be performed using pulsed laser annealing. Indeed, allowing a 2-D uniform surface annealing, this process is expected to provide better ion implantation damage recovery and higher dopant activation without damaging already manufactured buried layers [4], [5].

The latter, i.e., alleviating the FLP could consist in inserting a dielectric layer between the metal and the semiconductor of the contacts [7] resulting in metal/insulator/semiconductor (MIS) contacts. Recently, the studies of subnanometric TiO_x insertions [8], [9] have shown promising results on n-type Si reporting contact resistivity values equivalent to, respectively, 3.12×10^{-8} and $9.1 \times 10^{-9} \Omega \cdot \text{cm}^2$. However, most of the efforts thus far were focused on reducing the equivalent dc resistivity of stand-alone contact, with no insight on neither the n and pMOSFETs cointegration scheme nor the impact on MOSFET ac performance when contacted with MIS contacts.

In our previous study (part I [10]), protocol to analytically simulated I - V characteristics of MIS contacts as a function of the metallization and the insertion nature and thickness was presented. Based on these nonlinear nonsymmetrical generated I - V characteristics, it was found that the comparison of such contacts with ohmic references is not immediate by looking to the $[-1 \text{ V}, +1 \text{ V}]$ range.

In this part (part 2), the efficiency of the MIS contacts is evaluated via the prism of their impact on both the dc and ac performances of MOSFETs. Evaluating the conductive property impact is performed by fitting elementary SPICE compact models on analytically simulated I - V characteristics generated in part I, then wiring them on each side of 10-nm p and nMOSFET SPICE blocks and finally looking at the impact on resulting I_D - V_{DS} characteristics. Subsequently, the capacitive effects caused by the dielectric are taken into account for both nonconformal and conformal insertions. As shown in Fig. 1, while the former configuration consists in a dielectric only covering the bottom of the contact cavity, the latter features a dielectric following the topography, i.e., also covering the side of the contact cavity. The actual gauging of

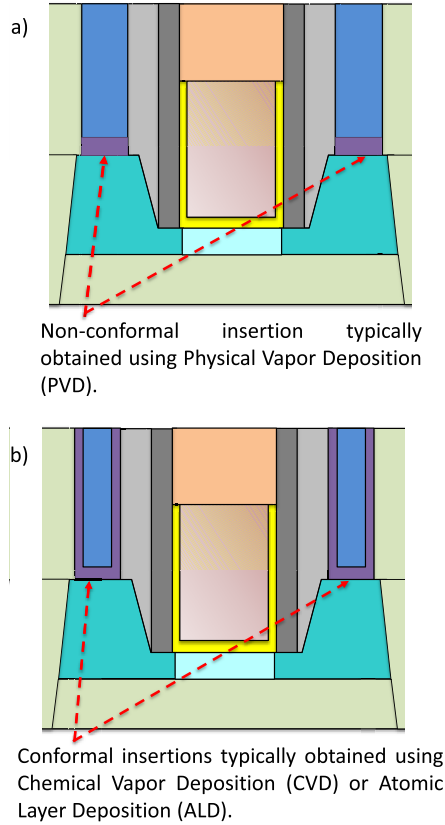


Fig. 1. Structure of a transistor presenting an insertion between the metal of the contact and the semiconductor of the source and drain for (a) nonconformal and (b) conformal dielectric deposition.

the MIS contacts is then performed regarding their impact on ac performance via the extraction of the inverter delay from seven stages ring oscillators (ROs).

II. p AND nMOSFETs DC PERFORMANCE

As stated in part 1, in the overwhelming majority of cases, the junctions $J-V$ characteristics are neither perfectly linear nor symmetrical in a $[-1 \text{ V}, +1 \text{ V}]$ range of bias. For this reason, a contact resistivity associated with such contacts has to be provided with its bias of extraction. Nevertheless, the effective contact resistivity value cannot be evaluated at one arbitrary bias voltage. The effective operative contact bias to be considered arises from solving the voltage sharing between contacts and MOSFET when applying a supply voltage V_{dd} . This problem boils down to treating diodes and resistors in series, which is famously known to be a self-consistent problem and can be evaluated using simulation.

Toward this goal, compact models were built using elementary SPICE components, i.e., resistors and diodes in order to reproduce the electrical behavior of all the analytically calculated MIS diodes $J-V$ characteristics of part 1. These SPICE contact compact models were then plugged on each side of 10FDSOI p and nMOSFET SPICE blocks. The resulting $I_D - V_{DS}$ values at $V_{GS} = 0.7 \text{ V}$ are presented in Fig. 2(a) and (b) and compared with MOSFETs with $\rho_c = 10^{-7} \Omega \cdot \text{cm}^2$, $\rho_c = 10^{-8} \Omega \cdot \text{cm}^2$, and $\rho_c = 10^{-9} \Omega \cdot \text{cm}^2$ linear resistors emulating the contacts.

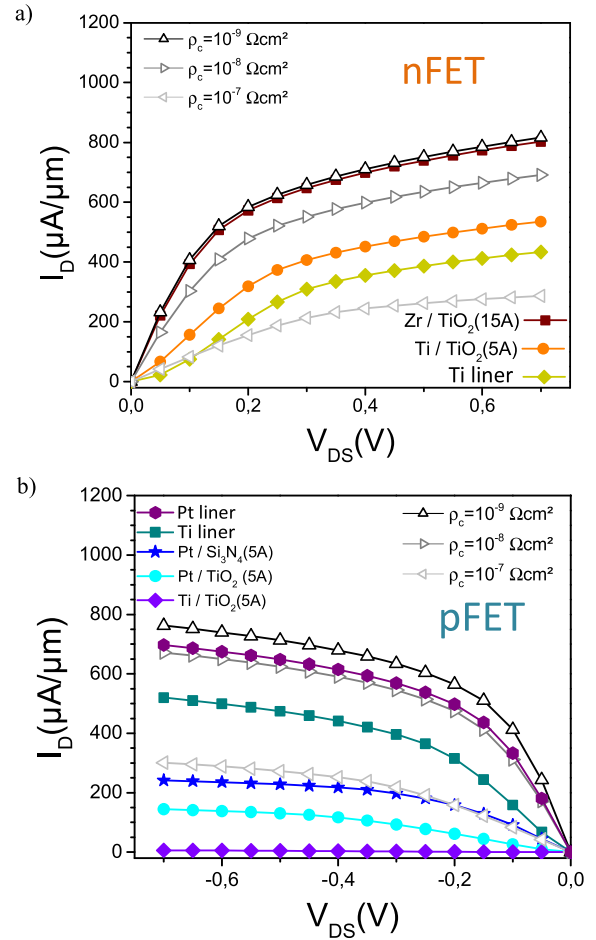


Fig. 2. Simulated drain current as a function of V_{DS} for ohmic and MIS contacts assuming $q\Phi_m(\text{Zr}) = 4.1 \text{ eV}$, $q\Phi_m(\text{Ti}) = 4.33 \text{ eV}$, and $q\Phi_m(\text{Pt}) = 5 \text{ eV}$ for scaled (a) nMOSFET and (b) pMOSFET ($L_g = 18 \text{ nm}$ and $W = 130 \text{ nm}$).

Whereas the comparison of the studied contacts performance with the ohmic references was not immediate by looking to the $J-V$ characteristics on $[-1 \text{ V}, +1 \text{ V}]$ range, considering their impact on $I_D - V_{DS}$ ensures a proper ranking of the different MIS junctions with the references. It appears that the optimal contact configurations Pt/p-Si and Zr/TiO₂(15Å)/n-Si perform, respectively, slightly above the $10^{-8} \Omega \cdot \text{cm}^2$ and below the $10^{-9} \Omega \cdot \text{cm}^2$ ideal contacts.

The results obtained on nFETs suggest that the effective contact resistivity value recommended by the ITRS can be approached using the MIS contact paradigm. Nevertheless, pFETs performance suffer from the lack of low valence band offset (VBO) dielectrics and judging solely from the impact on static output current, it seems that the equivalent contact resistivity on pFETs is capped around $10^{-8} \Omega \cdot \text{cm}^2$.

III. RING OSCILLATOR FREQUENCY

The dc characteristic improvement relying on equivalent contact resistivity reduction is a first figure of merit, which can be used to evaluate the suitability of a MIS contact. Nevertheless, a nonconformal dielectric insertion also results in what can be modeled by a capacitor (C_{MIS}) in parallel with the contact diode (R_{MIS}), as shown in Fig. 3. Though irrelevant

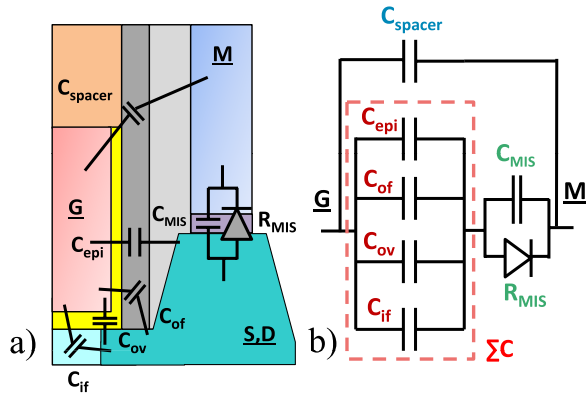


Fig. 3. (a) Structure of a transistor presenting the usual parasitic capacitances and the one induced by the dielectric insertion. (b) Equivalent electric block diagram for nonconformal dielectric deposition.

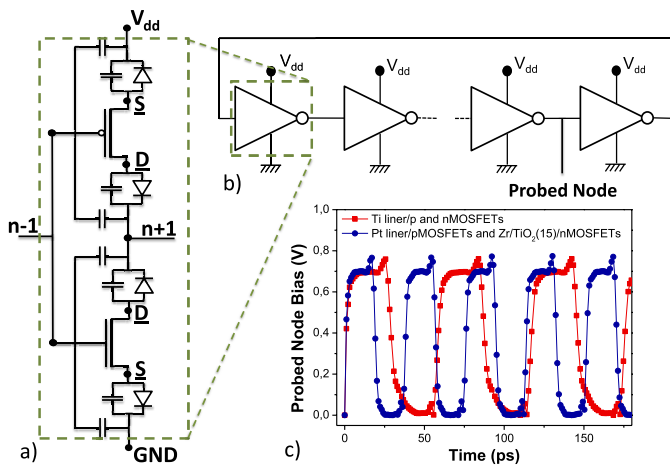


Fig. 4. (a) Elementary inverter presenting MIS contacts. (b) Seven stages ROs were simulated. (c) Resulting probed node bias as a function of the time.

in the dc regime, this capacitor may have a significant impact on the dynamic response of a transistor featuring MIS contacts.

As stated previously, the equivalent resistivity R_{MIS} has to be considered at the actual operative contact bias, since the $I-V$ characteristics of the majority of MIS contacts are neither perfectly linear nor symmetrical. Already important in the dc study, this assertion is even more relevant in the ac regime, since the applied bias V_{app} periodically varies between $-V_{dd}$ and $+V_{dd}$. Therefore, the actual contact bias arises from the sharing of a varying bias between the MOSFET and the contacts.

Consequently, studying the impact of the MIS contacts on the 10-nm node ac performance was achieved generating ROs using SPICE simulation and taking in account both the capacitive and the nonlinear resistive properties of the studied contact. The ranking of the junctions was performed by correlating the ROs frequency with the type of contacts flanking the MOSFETs of the inverters. It should be noted that the considered MIS contacts being based on ultrathin high-k dielectric insertions, the resulting capacitors are substantial, i.e., their impact on the contacts complex impedance is expected to be considerable.

As shown in Fig. 4(a), inverters based on p and nMOSFETs flanked by MIS contacts were thus generated using the

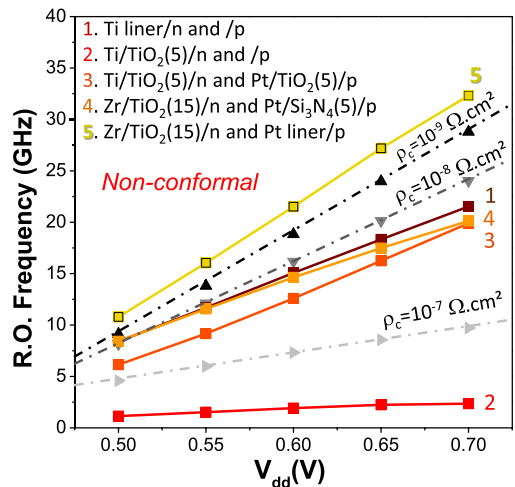


Fig. 5. Seven stages RO oscillation frequency as a function of the supply voltage for nonconformal dielectric insertions.

SPICE blocks defined previously. Seven-stages ROs were implemented with various combinations of dielectric insertions and metallizations [Fig. 4(b)]. In order to compare the ac results with the dc ones, the different configurations of n- and p-type Si-based MS and MIS contacts are the same as the ones presented in [10] and in Fig. 2(a) and (b). The RO oscillation frequencies are presented in Fig. 5 for the considered combinations of contacts along with that of ROs composed by p and nMOSFETs flanked by $\rho_c = 10^{-7} \Omega \cdot \text{cm}^2$, $\rho_c = 10^{-8} \Omega \cdot \text{cm}^2$, and $\rho_c = 10^{-9} \Omega \cdot \text{cm}^2$ ohmic contacts.

The reference case of insertion-free Ti contacts on both p and nFETs performs in the ac regime slightly below the $\rho_c = 10^{-8} \Omega \cdot \text{cm}^2$ ideal case. Since these contacts do not present any insertion, there is no additional capacitive contribution to consider. Therefore, the ac and dc results are in concordance.

As stated in [10], pFETs performance suffering from the lack of low VBO dielectrics, all the combination of contacts involving an insertion on the pFETs feature poor oscillation frequency. Thus, a single-insertion single-metallization scheme cannot be considered. Finally, the optimal configuration was found to be the same as in dc, i.e., the combination of Pt/p-Si and Zr/TiO₂(15Å)/n-Si. It is worth noting that while separated n & pFETs respectively presenting Zr/TiO₂/Si and Pt/Si junctions both perform in dc under the ideal case of $10^{-9} \Omega \cdot \text{cm}^2$, their association results in ROs outperforming this same reference in ac. Therefore, the nonconformal insertion implemented in the nFETs contacts which was initially chosen to optimize the contact resistivity seems to feature an additional impedance reduction in the ac regime.

IV. CONTACTS COMPLEX IMPEDANCE

Sacrificing some degree of accuracy for the sake of qualitative understanding, notional contacts made of an ideally linear resistor in parallel with a capacitor were connected to p and nMOSFETs. Those RC blocks were not fitted on analytically simulated MIS contacts as before. Instead, the R and C parameters were considered arbitrarily tunable and unrelated. Delays of ROs based on 10FDSOI plugged with these contacts are shown in Fig. 6.

Single Inverter Delay (ps) @ V_{dd}=0.7V

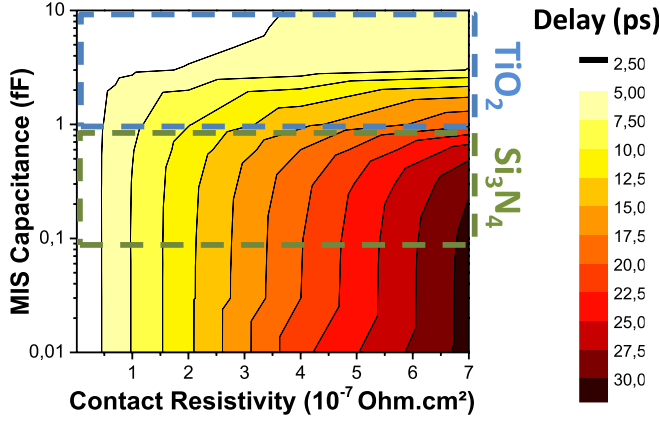


Fig. 6. Delay of a single inverter versus contact resistivity and MIS capacitance in the notional case of a nonconformal insertion-based MIS contact presenting ohmic I - V characteristic.

In order to highlight the effect of the capacitance, the range of the resistance was intentionally chosen high compared with the intrinsic MOSFET resistance, and thus to the ITRS target of $\rho_c = 10^{-9} \Omega \cdot \text{cm}^2$. Doing so, the ROs delay is dominated by the contact impedance if no capacitance is added to the contact. Results of Fig. 6 suggest that for a given resistance, increasing the contact capacitance reduces the inverter delay.

As a matter of fact, the complex impedance of a contact composed by a capacitor in parallel with a resistor is expressed in the following:

$$Z_{\text{eq}} = \frac{R}{1 + jRC\omega} \quad (1)$$

where R is the equivalent resistivity of the contact, C is its capacitance, and ω is the frequency of the applied bias. It is worth noting that the complex impedance is equivalent to R if $\omega = 0$, i.e., if the transistor is used in dc regime.

The magnitude of this complex impedance, i.e., its modulus is therefore expressed in the following:

$$|Z_{\text{eq}}| = \frac{R^2}{1 + R^2C^2\omega^2}. \quad (2)$$

Therefore, the capacitance primarily acts as a shunt capacitor reducing the conduction path impedance in the ac regime. For a given frequency, if the resistance is nonnegligible, this modulus tends to $|Z_{\text{eq}}| \approx (1/C^2\omega^2)$. Then, a low capacitance will lead to the high impedance while a high capacitance will lead to the low impedance.

Nevertheless, the single inverter delay was calculated using independently varying R and C . This configuration could not occur in practice, since the variation of either the resistance or the capacitance of a MIS contact leads to the variation of its counterpart. Moreover, the dielectric layer necessarily introduces current-voltage nonlinearity, which is not taken in account in this ideal case.

V. CONFORMAL DIELECTRIC INSERTION

Aiming at investigating all the foreseeable integration schemes, the case of a conformal deposition of the dielectric insertion was simulated. This conformal deposition presents

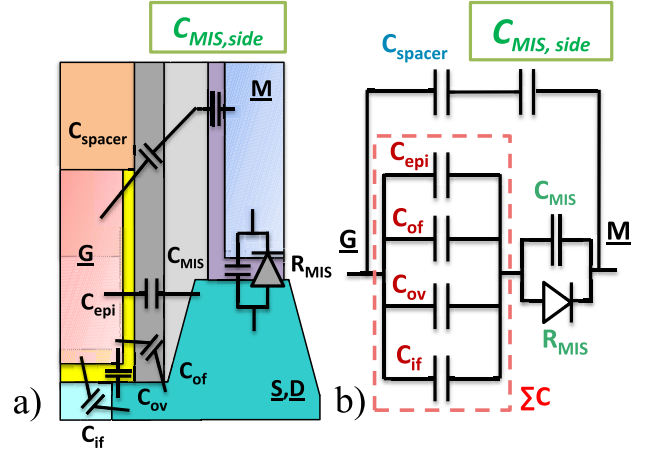


Fig. 7. (a) Structure of a transistor presenting the usual parasitic capacitances and the ones induced by the conformal dielectric insertion. (b) Equivalent electric block diagram for conformal dielectric deposition.

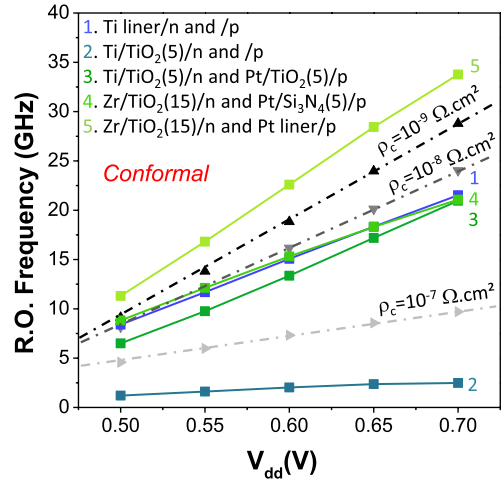


Fig. 8. Seven stages RO oscillation frequency as a function of the supply voltage for conformal dielectric insertions.

	Contacts		Single Inverter Delay (ps) @ V _{dd} =0.7V		Conformal vs. Non-Conformal Gain
	p-side	n-side	Non-Conformal	Conformal	
Ohmic	1e-7	1e-7	7.357		
Single MIS	Pt/TiO ₂ (5Å)	Ti/TiO ₂ (5Å)	3.589	3.407	5.1%
Dual MIS	Pt/Si ₃ N ₄ (5Å)	Zr/TiO ₂ (15Å)	3.549	3.389	4.5%
Reference	Ti liner	Ti liner	3.319		
Ohmic	1e-8	1e-8	2.973		
Ohmic	1e-9	1e-9	2.481		
Hybrid	Pt liner	Zr/TiO ₂ (15Å)	2.210	2.116	4.3%

Fig. 9. Single inverter delay extracted from the RO frequency as a function of the contacts used to plug the transistors. The gain obtained by a conformal deposition is also evaluated for the configuration presenting at least one dielectric insertion. The color code refers to the conduction efficiency of the contact.

an additive sidewall capacitance ($C_{\text{MIS,side}}$) in series with the spacer one (C_{Spacer}), as shown in Fig. 7.

For similar reasons that C_{MIS} is expected to be large, i.e., the considered MIS contacts are based on ultrathin high-k

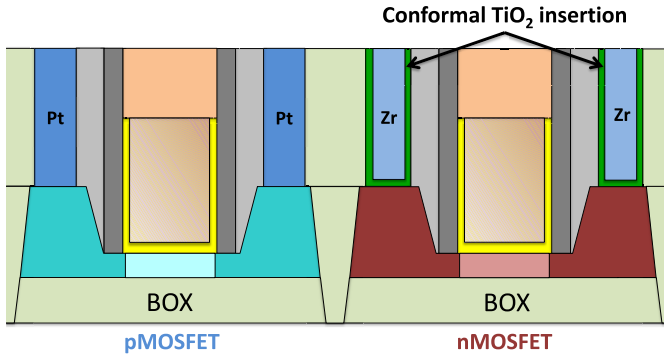


Fig. 10. Predicted optimal integration scheme. Considering commonly available metals and dielectrics, taking full advantage of the FLP alleviation in planar cointegration of n and pFETs requires a dual-metal/dual-insertion scheme, i.e., Pt/no insertion/p and Zr/TiO₂(15Å)/n.

dielectric insertions, $C_{\text{MIS,side}}$ is also expected to be extensive. Nevertheless, being in series with C_{spacer} , its high value will result in a poor impact on the ROs frequency.

The modified RO oscillation frequencies are presented in Fig. 8. Featuring the same ranking of the different contacts configurations as in the nonconformal case, a slight gain is observed when using a conformal deposition. The net effect is equivalent to slightly lowering the lateral parasitic C_{spacer} for little to no penalty on the dc current flow. A summary of all the single inverter delays versus integration scheme and type of deposition is shown in Fig. 9. Finally, a sketch representing the electrically optimal cointegration is represented in Fig. 10.

VI. CONCLUSION

The study of the MIS contacts effective impact on aggressively scaled transistor dc and ac performances was carried out. In part 1, it was found that no MIS contact configuration enabled conductivity improvement on p-type Si compared with a Ti liner contact reference. Even a change in metallization scheme was found to be inefficient on p-Si if associated with a dielectric insertion, since their theoretical VBO to Si were too important.

In part 2, evaluating the impact of MS and MIS contact on the MOSFETs dc performance, the optimal contact on p-Si was found to be roughly performing above ideal $10^{-8}\text{-}\Omega\cdot\text{cm}^2$ ohmic contact while the optimal MIS junctions on n-type Si were equivalent to a $10^{-9}\text{-}\Omega\cdot\text{cm}^2$ ohmic contact.

Complementarily, also in part 2, we highlighted that the shunt capacitor induced by a nonconformal dielectric insertion on the conduction path has a significant impact on ac performances, allowing an extra improvement beyond the $10^{-9}\text{-}\Omega\cdot\text{cm}^2$ ideal case. An additional improvement of the ac performances was found to arise from the use of a conformal insertion. Nevertheless, this improvement was found to be only a fraction of the prime enhancement.

In conclusion, even though the implementation of the optimal integration scheme remains nontrivial, the study of ac regime response has led us to positively reassess our initial projections on the possible impact of MIS contacts obtained by only considering the dc impact.

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