



HAL
open science

Thermoelectric energy conversion: How good can silicon be?

Maciej Haras, Valeria Lacatena, François Morini, J.F. Robillard, Stephane Monfray,
Thomas Skotnicki, Emmanuel Dubois

► **To cite this version:**

Maciej Haras, Valeria Lacatena, François Morini, J.F. Robillard, Stephane Monfray, et al.. Thermoelectric energy conversion: How good can silicon be?. *Materials Letters*, 2015, 157, pp.193-196. <10.1016/j.matlet.2015.05.012>. <hal-03325003v2>

HAL Id: hal-03325003

<https://hal.science/hal-03325003v2>

Submitted on 28 Aug 2024

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



HAL Authorization

Thermoelectric energy conversion: How good can silicon be?

Maciej Haras^{a,b}, Valeria Lacatena^{a,b}, François Morini^a, Jean-François Robillard^a, Stéphane Monfray^b, Thomas Skotnicki^b, Emmanuel Dubois^{a,*}

^a IEMN/ISEN, UMR CNRS 8520, Avenue Poincaré, Cité Scientifique, 59652 Villeneuve d'Ascq, France

^b STMicroelectronics, 850 rue Jean Monnet, 38920 Crolles, France

ABSTRACT

Lack of materials which are thermoelectrically efficient and economically attractive is a challenge in thermoelectricity. Silicon could be a good thermoelectric material offering CMOS compatibility, harmlessness and cost reduction but it features a too high thermal conductivity. High harvested power density of 7 W/cm² at $\Delta T=30$ K is modeled based on a thin-film lateral architecture of thermo-converter that takes advantage of confinement effects to reduce the thermal conductivity. The simulation leads to the conclusion that 10 nm thick Silicon has 10 × higher efficiency than bulk.

Keywords:

Thin films

Energy storage and conversion

Simulation and modeling

Semiconductors

Electrical properties

Thermal properties

1. Introduction

Spurred by the pervasive spreading of mobile, network-connected and energetically autonomous devices pertaining to the so-called *Internet-of-Things*, the development of low cost, sustainable, and efficient micro-power harvesting sources has received an increasing attention over recent years [1]. Thermal wastes represent one of the most available resource, including heat from the human body area for e.g. feeding wearable electronics [2]. Although thermoelectric conversion holds significant advantages over mechanical one, its practical use is limited to niche applications such as automotive [3], spatial [4] medical [5] or sophisticated industrial use [6]. The main reason of this deficiency is connected to the performance at the material level and can be analyzed by considering the dimensionless figure-of-merit zT that needs to be maximized [7] to step-up conversion efficiency η [8]:

$$zT = \frac{S^2 \cdot \sigma}{\kappa} \cdot T = \frac{S^2 \cdot \sigma}{\kappa_e + \kappa_{ph}} \cdot T \quad (1)$$

$$\eta = \frac{P_{el}}{|Q|} = \frac{T_{HOT} - T_{COLD}}{T_{HOT}} \cdot \frac{\sqrt{1+zT} - 1}{\sqrt{1+zT} + \frac{T_{COLD}}{T_{HOT}}} \quad (2)$$

where S , κ and σ are material-dependent parameters corresponding to thermopower, thermal and electrical conductivities, respectively.

P_{el} is the generated electric power density while $Q = -\kappa(T) \cdot \nabla T$ is the heat flux that depends on the temperature difference ($T_{HOT} - T_{COLD}$) across the material. It is also worth noting that the thermal conductivity originates from both phonons propagation through the lattice κ_{ph} and from heat transported by charge carriers κ_e . Eq. (1) reveals that good thermoelectric materials are therefore expected to feature a large, *electron-crystal*, electrical conductivity and a poor, *phonon-glass*, thermal conductivity, two conditions difficult to conciliate [9]. To complete the analysis, Fig. 1 shows how η relates to zT , with a selection of state-of-the-art materials [10–12]. Majority of used materials are complex, harmful, expensive, incompatible with CMOS technologies and toxic e.g. bismuth, telluride, lead, antimony. In contrast, silicon does not suffer from the aforementioned drawbacks but features, so far, a too large bulk thermal conductivity (148 W/m/K) for being useful in thermoelectric generation.

Recent strategies to boost conversion efficiency rely on the use of low-dimensional systems such as thin films, superlattices, quantum dots or nanowires which confine thermal phonons and thus to increase zT [13,14]. A further reduction of lattice thermal conductivity (κ_{ph}) can also be obtained by enhanced phonon scattering using phononic engineering with a negligible side effect on S and σ [15,16]. In this context, it appears legitimate to evaluate the conversion efficiency of thermo-generators based on a thin-film architecture that fully exploit confinement effect on thermal conductivity. Surprisingly, despite numerous publications describing the interest of nanostructured silicon for thermoelectricity at the material level, there is still lack of studies presenting a performance evaluation at the thermoelectric converter level. This letter therefore provides a detailed

* Corresponding author. Tel.: +33 320 19 79 16.

E-mail addresses: Maciej.Haras@isen.iemn.univ-lille1.fr (M. Haras), Emmanuel.Dubois@isen.iemn.univ-lille1.fr (E. Dubois).

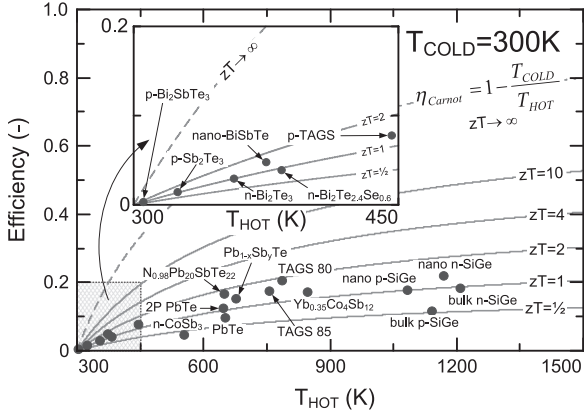


Fig. 1. Conversion efficiency for different zT values. Data points refer to the highest efficiency for given material [10–12].

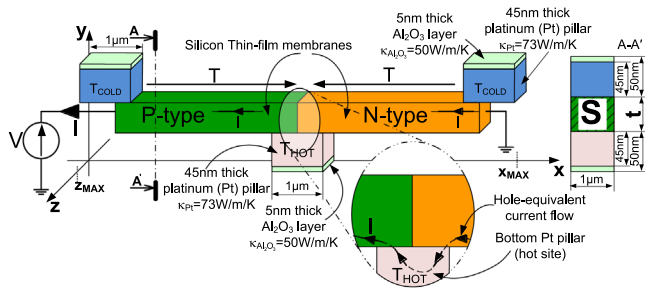


Fig. 2. Generic silicon based thermoelectric generator used for performance evaluation. The membrane length and width are $x_{MAX} = 10 \mu\text{m}$, $z_{MAX} = 1 \mu\text{m}$ while the membrane thickness is varied $t = 10 \text{ nm}$; 20 nm ; 30 nm ; 40 nm or 50 nm .

analysis of a thermo-generator based on Si membranes emphasizing the impact of confinement on the harvesting capabilities.

2. Converter structure and modeling approach

Fig. 2 depicts the generic converter structure based on a silicon thin film in which the primary bottom-up temperature gradient is laterally redirected using top and down contacts alternately disposed in a staggered arrangement [17]. The distinctive advantage of this architecture comes from its ability to guide heat and current in a thin film in which 2D phonon confinement and surface scattering can reduce thermal conductivity by one order of magnitude [15]. The electro-thermal behavior of the generator geometry is described by a non-isothermal drift-diffusion model as given by Eq. (3) [18]. equations for both carriers types are self-consistently solved with Poisson equation. The variations of the quasi-Fermi levels (ϕ_{Fn} , ϕ_{Fp}), Eq. (3a) thermopower coefficients (S_n , S_p) Eq. (3b), electrical conductivities (σ_n , σ_p) Eq. (3c), carrier mobilities (μ_n , μ_p), carrier concentrations (n , p), effective density of states in conduction N_C and valence N_V band are implicitly considered as dependent on the local lattice temperature (T_L).

$$\begin{cases} \vec{j}_n(T_L) = -\sigma_n(T_L) \cdot [\vec{\nabla} \phi_{Fn}(T_L) - S_n(T_L) \cdot \vec{\nabla} T_L] \\ \vec{j}_p(T_L) = -\sigma_p(T_L) \cdot [\vec{\nabla} \phi_{Fp}(T_L) - S_p(T_L) \cdot \vec{\nabla} T_L] \end{cases} \quad (3)$$

where:

$$\begin{cases} \phi_{Fn}(T_L) = \varphi - \frac{k \cdot T_L}{q} \ln \left[\frac{n(T_L)}{n_i(T_L)} \right] \\ \phi_{Fp}(T_L) = \varphi + \frac{k \cdot T_L}{q} \ln \left[\frac{p(T_L)}{n_i(T_L)} \right] \end{cases} \quad (3a)$$

$$\begin{cases} S_n(T_L) = -\frac{k}{q} \cdot \left[3/2 + \ln \left(\frac{N_C(T_L)}{n(T_L)} \right) \right] \\ S_p(T_L) = \frac{k}{q} \cdot \left[3/2 + \ln \left(\frac{N_V(T_L)}{p(T_L)} \right) \right] \end{cases} \quad (3b)$$

$$\begin{cases} \sigma_n(T_L) = q \cdot \mu_n(T_L) \cdot n(T_L) \\ \sigma_p(T_L) = q \cdot \mu_p(T_L) \cdot p(T_L) \end{cases} \quad (3c)$$

Complementarily to electrical transport in the silicon body, contact resistances are carefully modeled by accounting for transport through the metal/semiconductor interface. Following [19], we assumed a specific contact resistivity of $\rho_{contact} = 5 \times 10^{-7} \Omega \text{ cm}^2$ for a doping level of 10^{19} cm^{-3} , a figure representative of Pt or Ni-based silicides. Alternatively, the Schottky nature of the metal/semiconductor contact at low doping level was modeled by thermionic injection **Fig. 2** gives a schematic representation of a single thermocouple. In the final generator assembly, those thermocouples are electrically connected in series to elevate the output voltage. The edges of each thermocouple consists in metallic contacts made of 45 nm thick platinum (Pt) pillars with $\kappa_{Pt} = 73 \text{ W/m/K}$ [20]. The metal pillars are in direct contact with silicon membranes to ensure the current continuity between neighboring thermocouples. The electric insulation between the silicon membrane and the top/bottom metallic plates is assured by a 5 nm thick layer of Al_2O_3 ($\kappa_{\text{Al}_2\text{O}_3} = 50 \text{ W/m/K}$ [20]) deposited at the bottom (resp. top) of the hot (resp. cold) contact.

The adoption of thin membranes calls for a proper treatment of the size effect that reflects thermal conductivity reduction with film thickness. Based on a resolution of the Boltzmann transport equation in the relaxation time approximation, Sondheimer [21] have described the size effect through the incorporation of an adequate diffusive phonon boundary scattering model. They reported the exact expression of a reduction factor $F(t, \lambda_{av})$ that accounts for the decrease of the relaxation time with film thickness t and depends on an average mean free path λ_{av} :

$$F(t, \lambda_{av}) = 1 - \frac{3}{2} \cdot \frac{t}{\lambda_{av}} \int_1^\infty \left(\frac{1}{z^3} - \frac{1}{z^5} \right) \cdot \left[1 - \exp \left(-\frac{t}{\lambda_{av}} \cdot z \right) \right] dz \quad (4)$$

where z denotes a dummy integration variable. For single-crystal silicon, λ_{av} of 300 nm is representative of dominant phonons over the frequency spectrum. In a simplified picture, thermal conductivity is here assumed to follow the same size effect law $\kappa_{film} = \kappa_{bulk} F(t, \lambda_{av})$. The electro-thermal measurement of thermal conductivity in thin-film Si was possible thanks to measurement platform [22] **Fig. 3(a)**. In this topology the characterized thin-film membrane is thermally insulated from surroundings, improving the precision of the measurement. In addition, to limit convection losses, the measurement is performed in vacuum. Thermal conductivity is measured knowing the membrane's dimensions, heater's and sensor's temperatures and electric power released in heater. The thermal conductivity for 70 nm thick Si was measured to be 55 W/m/K which is marked in **Fig. 3(b)** by square data marker.

Fig. 3(b) reports the variation of κ as a function of Si thickness at room temperature. It can be first observed that the model accuracy is validated through a comparison with measured values published in the literature over a broad range of thicknesses [15,16,22–27]. Second, an overall $10 \times$ reduction in thermal conductivity is obtained for a 10 nm membrane compared to bulk material. It is also worth noting that the dependence of κ_{film} with temperature is taken into consideration under the form prescribed by [28]:

$$\kappa_{film}(T) = \kappa_{film}(300\text{K}) \cdot \left(\frac{T_L}{300} \right)^\beta \quad (5)$$

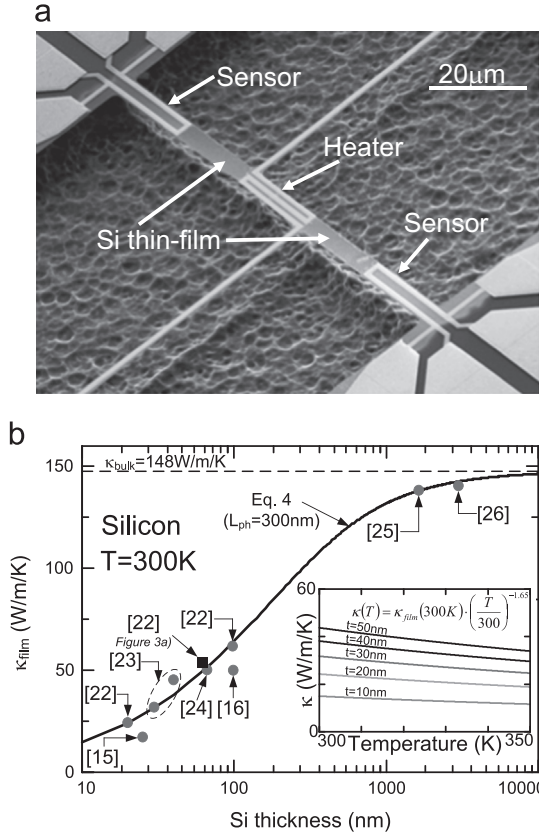


Fig. 3. (a) Micro-meter measurement platform for thermal conductivity measurement in thin-film silicon. (b) Model of thermal conductivity as a function of Si thickness. Distinguished square data point presents the measurement obtained in structure from (a). Insert depicts the temperature dependency.

where $\beta = -1.65$. The insert in Fig. 3(b) shows a typical 20% reduction in κ_{film} in the 300–350 K temperature range.

3. Discussion and results

Assuming that the temperature gradient is constant, the current-voltage and the temperature-dependent power density can be calculated using Eq. (3) without resorting to the thermal conductivity. Fig. 4(a) depicts the power and current densities as a function of the output voltage for doping level of 10^{19} cm^{-3} .

The harvested peak power density amounts to 7 W/cm^2 for a 30 K temperature difference across the generator, thereby placing Si in a competitive position when compared to thermo-generators based on thin-film $\text{Sb}_2\text{Te}_3/\text{Bi}_2\text{Te}_3$ alloys [5]. Unlike current and power densities, the conversion efficiency is directly impacted by the thermal conductivity of the core thermoelectric material. To quantify the added-value of thin-film architectures, Fig. 4(b) presents the efficiency (η) versus temperature difference (ΔT) curves parameterized by the film thickness. Note that for the evaluation of η , the peak electrical power was calculated under load matching condition. The inspection of Fig. 4(b) reveals that the reduction of thermal conductivity due to the size effect is integrally translated into a corresponding gain in conversion efficiency. Although apparently evident, this result more precisely ensues from the different orders of magnitude of the charge carrier and phonon scattering mean free paths. As pictured in Fig. 3(b), κ starts to decay when the film thickness approaches 300 nm that corresponds to λ_{av} . Conversely, carriers mobility in thin SOI is weakly affected by confinement effects for doped silicon films thicker than 10 nm [29].

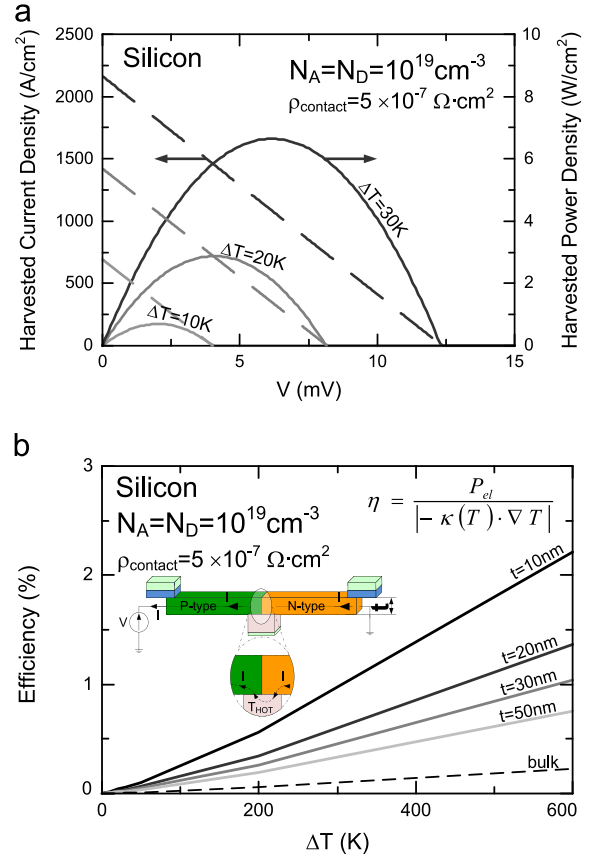


Fig. 4. (a) Power (continuous line) and current (dashed line) densities versus output voltage at different temperature drops for a doping of 10^{19} cm^{-3} (b) calculated efficiency of thin-film generators versus temperature difference for different Si thicknesses. The doping level is 10^{19} cm^{-3} for both the n- and p-type branches and the specific contact resistivity $\rho_c = 5 \times 10^{-7} \text{ } \Omega \cdot \text{cm}^2$.

4. Conclusions

Owing to an excellent electrical conductivities and a high Seebeck thermopower, Si is a good candidate for thermoelectric conversion capable to generate a harvested power density up to 7 W/cm^2 for $\Delta T = 30 \text{ K}$. In this letter, we have precisely quantified the thermal conductivity reduction associated to confinement effects to enhance conversion efficiency. Using a 10 nm Si thick film results in a $10 \times$ higher efficiency when compared to bulk. Further efficiency improvement is expected through the use of phononic crystals [15] able to reduce κ by an additional decade.

Acknowledgment

The research leading to these results has received funding from the STMicroelectronics-IEMN Common Laboratory and the European Research Council (Grant agreement no. 338179). This work was partly supported by the French RENATECH Network.

References

- [1] Gorlatova M, Kinget P, Kymissis I, Rubenstein D, Wang X, Zussman G. Energy harvesting active networked tags (EnHANTS) for ubiquitous object networking. IEEE Wirel Commun 2010;17:18–25. <http://dx.doi.org/10.1109/MWC.2010.5675774>.
- [2] Kim SJ, We JH, Cho BJ. A wearable thermoelectric generator fabricated on a glass fabric. Energy Environ Sci 2014;7:1959–65. <http://dx.doi.org/10.1039/C4EE00242C>.
- [3] Yang J, Caillat T. Thermoelectric materials for space and automotive power generation. MRS Bull 2006;31:224–9. <http://dx.doi.org/10.1557/mrs2006.49>.

- [4] Rowe DM. Applications of nuclear-powered thermoelectric generators in space. *Appl Energy* 1991;40:241–71. [http://dx.doi.org/10.1016/0306-2619\(91\)90020-X](http://dx.doi.org/10.1016/0306-2619(91)90020-X).
- [5] Francioso L, De Pascali C, Farella I, Martucci C, Creti P, Siciliano P, et al. Flexible thermoelectric generator for ambient assisted living wearable biometric sensors. *J Power Sources* 2011;196:3239–43. <http://dx.doi.org/10.1016/j.jpowsour.2010.11.081>.
- [6] Nenninger P, Marco U. Harvest time. *ABB Rev* 2011;1:47–51.
- [7] Rowe DM. Thermoelectric power generation. *Proc IEE* 1978;125:1113–36.
- [8] Min G, Rowe DM. Cooling performance of integrated thermoelectric micro-cooler. *Solid-State Electron* 1999;43:923–9. [http://dx.doi.org/10.1016/S0038-1101\(99\)00045-3](http://dx.doi.org/10.1016/S0038-1101(99)00045-3).
- [9] Slack GA. *New materials and performance limits for thermoelectric cooling*. Boca Raton, FL: CRC Press; 1995 *CRC Handb. Thermoelectr.*
- [10] Minnich AJ, Dresselhaus MS, Ren ZF, Chen G. Bulk nanostructured thermoelectric materials: current research and future prospects. *Energy Environ Sci* 2009;2:466–79. <http://dx.doi.org/10.1039/B822664B>.
- [11] Carmo JP, Goncalves LM, Correia JH. Micro and nanodevices for thermoelectric converters. In: Bhushan B, editor. *Scanning Probe Microsc. Nanosci. Nanotechnol.* 2. Heidelberg: Springer; 2010. p. 791–811.
- [12] Snyder GJ, Toberer ES. Complex thermoelectric materials. *Nat Mater* 2008;7:105–14. <http://dx.doi.org/10.1038/nmat2090>.
- [13] Boukai AI, Bunimovich Y, Tahir-Kheli J, Yu J-K, Goddard III WA, Heath JR. Silicon nanowires as efficient thermoelectric materials. *Nature* 2008;451:168–71. <http://dx.doi.org/10.1038/nature06458>.
- [14] Venkatasubramanian R, Siivola E, Colpitts T, O'Quinn B. Thin-film thermoelectric devices with high room-temperature figures of merit. *Nature* 2001;413:597–602. <http://dx.doi.org/10.1038/35098012>.
- [15] Yu J-K, Mitrovic S, Tham D, Varghese J, Heath JR. Reduction of thermal conductivity in phononic nanomesh structures. *Nat Nano* 2010;5:718–21. <http://dx.doi.org/10.1038/nnano.2010.149>.
- [16] Tang J, Wang H-T, Lee DH, Fardy M, Huo Z, Russell TP, et al. Holey silicon as an efficient thermoelectric material. *Nano Lett* 2010;10:4279–83. <http://dx.doi.org/10.1021/nl102931z>.
- [17] Strasser M, Aigner R, Lauterbach C, Sturm TF, Fransosch M, Wachutka GKM. Micromachined CMOS thermoelectric generators as on-chip power supply. *Sens Actuators Phys* 2004;114:362–70. <http://dx.doi.org/10.1016/j.sna.2003.11.039>.
- [18] Wachutka GK. Rigorous thermodynamic treatment of heat generation and conduction in semiconductor device modeling. *IEEE Trans Comput Aided Des Integr Circuits Syst* 1990;9:1141–9. <http://dx.doi.org/10.1109/43.62751>.
- [19] Stavitski N, van Dal MJH, Lauwers A, Vrancken C, Kovalgin AY, Wolters RAM. Systematic TLM measurements of NiSi and PtSi specific contact resistance to n- and p-type Si in a broad doping range. *IEEE Electron Device Lett* 2008;29:378–81. <http://dx.doi.org/10.1109/LED.2008.917934>.
- [20] CRC. *CRC materials science and engineering handbook*. 3rd ed.. Boca Raton, FL: CRC Press; 2001.
- [21] Sondheimer EH. The mean free path of electrons in metals. *Adv Phys* 1952;1:1–42. <http://dx.doi.org/10.1080/00018735200101151>.
- [22] Haras M, Lacatena V, Morini F, Robillard J-F, Monfray S, Skotnicki T, et al. Fabrication of integrated micrometer platform for thermoelectric measurements. In: *Electron devices meet. IEDM 2014 IEEE Int., San Francisco: 2014*, 8.5.212–8.5.215.
- [23] Liu W, Asheghi M. Phonon-boundary scattering in ultrathin single-crystal silicon layers. *Appl Phys Lett* 2004;84:3819. <http://dx.doi.org/10.1063/1.1741039>.
- [24] Ju YS. Phonon heat transport in silicon nanostructures. *Appl Phys Lett* 2005;87:153106. <http://dx.doi.org/10.1063/1.2089178>.
- [25] Aubain MS, Bandaru PR. Determination of diminished thermal conductivity in silicon thin films using scanning thermoreflectance thermometry. *Appl Phys Lett* 2010;97:253102. <http://dx.doi.org/10.1063/1.3527966>.
- [26] Asheghi M, Leung YK, Wong SS, Goodson KE. Phonon-boundary scattering in thin silicon layers. *Appl Phys Lett* 1997;71:1798. <http://dx.doi.org/10.1063/1.119402>.
- [27] Asheghi M, Kurabayashi K, Kasnavi R, Goodson KE. Thermal conduction in doped single-crystal silicon films. *J Appl Phys* 2002;91:5079. <http://dx.doi.org/10.1063/1.1458057>.
- [28] Palankovski V, Schultheis R, Selberherr S. Simulation of power heterojunction bipolar transistors on gallium arsenide. *IEEE Trans Electron Devices* 2001;48:1264–9. <http://dx.doi.org/10.1109/16.925258>.
- [29] Ohata A, Cassé M, Faynot O. Electrical characteristics related to silicon film thickness in advanced FD SOI-MOSFETs. *Solid-State Electron* 2008;52:126–33. <http://dx.doi.org/10.1016/j.sse.2007.07.028>.