Optimal control allocation for the parallel interconnection of buck converters

Jérémie Kreiss, Marc Bodson, Romain Delpoux, Jean-Yves Gauthier, Jean-François Trégouët, Xuefang Lin-Shi

Optimal Control Allocation for the Parallel Interconnection of Buck Converters

Jérémie Kreiss[1,*], Marc Bodson[2], Romain Delpoux[3], Jean-Yves Gauthier[3], Jean-François Trégouët[3], Xuefang Lin-Shi[3]

Abstract

This paper presents a control algorithm for the parallel interconnection of heterogeneous power converters. A single resistive load is assumed to be fed by an arbitrary number of buck converters via a common DC bus. The approach is based on control allocation theory and a constrained quadratic optimization algorithm. The strategy achieves a fast voltage response with an optimal current distribution among the converters, while taking into account the current limits, the dynamic response, and the efficiency of the individual converters. An interesting by-product of the approach is the ability to put converters in and out of service through trivial adjustments of the code. The benefits of the approach are assessed through simulations and an experimental evaluation.

Keywords: Control allocation, quadratic optimization, constraints management, robust control, parallel interconnection of power converters

1. Introduction

Recent applications such as microgrids (see [1, 2, 3] for example) or low-voltage/high-current power supplies are composed of several power converters connected to a single load. This structure benefits from several advantages as a consequence of the distribution of the load current on multiple converters. Thereby, it is possible to improve the reliability [4], increase the ease of repair, improve the thermal management [5], reduce the output ripple by interleaving phases of the pulse-width modulation (PWM) [6], and increase the system efficiency [7].

The main control objective on such systems is to regulate the output voltage. This objective sets the steady-state value of the total current, while the current distribution between the converters remains free, even though the converters are coupled through the output voltage dynamics. One of the most widespread strategies for the determination of the current distribution is the so-called *droop-control method*. Although its implementation is straightforward, this approach deals with current distribution and voltage regulation as competing objectives. If priority is given to voltage regulation, the current distribution is deteriorated and *vice versa*. As a result, an optimal current distribution can only be obtained by allowing a static error on the output voltage (see [8]). A recent extension of such method for a DC microgrid and with a distributed architecture [2] still presents this static error for the output voltage.

Instead of compromising between voltage regulation and current distribution, the so-called *balanced current sharing* method gives priority to the voltage regulation and ensures an effective control of the output voltage. To this end, this well-known strategy imposes that every converter shares the same fraction of the total current (see [5, 6, 9, 10] for instance). If this strategy seems to be justified when the converters are identical, it is not expected to be optimal when the converters have different characteristics (in particular, in terms of rate of response and efficiency). Moreover, strategies used for balanced current sharing such as the master-slave or democratic architecture expose the system to a single point-of-failure risk [9, 11]. Finally, deriving conditions for closed-loop stability in this framework is not straightforward, as highlighted by [12] where a detailed anal-

∗. Corresponding author

1. Jérémie Kreiss is with Université de Lorraine, CRAN, UMR 7039, 2 avenue de la forêt de Haye, Vandœuvre-lès-Nancy Cedex, 54516, France. jeremie.kreiss@univ-lorraine.fr

2. Marc Bodson is with Department of Electrical and Computer Engineering, University of Utah, 50 S Central Campus Dr, Salt Lake City, USA. bodson@eng.utah.edu

3. Every author is with Laboratoire Ampère, INSA Lyon, Université de Lyon, 20, Avenue Albert Einstein, 69100 Villeurbanne, France. firstname.lastname@insa-lyon.fr

ysis of parallel interconnection of buck converters is provided.

Both droop-control and balanced current sharing methods consider voltage regulation and current distribution as competing objectives. However, the fact that current distribution remains free when the voltage value is set is an intrinsic property of the studied system. Then, it is possible to consider the two objectives as complementary and not competing ones. Consequently, it is possible to satisfy them simultaneously.

Recently, [7, 12, 13, 14] propose control methods for the parallel interconnection of buck converters that achieve simultaneously the two control objectives, i.e. the voltage regulation and the current distribution. Those results are based on the observation that the interconnection of multiple converters in parallel to a single load belongs to the class of over-actuated systems [15, 16].

Controlling over-actuated systems becomes challenging when constraints and optimization criteria are considered. *Control allocation theory* is an appealing solution for over-actuated systems (see [15, 16] for instance) and has recently been used for power electronics applications (see i.e. [17]). For the parallel interconnection of buck converters, this solution takes into account the distinct converter characteristics when distributing the total current. The resulting methods design the controller in two steps: (i) an external controller is designed to ensure the regulation of the output (or voltage in our case) using a global control variable or pseudo-effector, and (ii) a control allocation algorithm distributes the desired effort (or load current in our case) among the actuators, considering the constraints and other optimization criteria [15].

Several methods can be found in the control allocation literature and can be classified as follows: (i) the *static approach* for which the effort distribution is optimal instantly and at each time instant [15, 16], (ii) the *dynamic approach* where the effort distribution is only optimal for the steady state [18] and (iii) the *geometric approach* which separates the current distribution management from the total current generation by changes of coordinates [19, 20].

Typically, for the static approach, actuators are assumed to be fast enough to consider them as static devices in the design of the external loop ([15, 21, 16] to cite a few). However, [16, 22] extend this approach to take dynamical actuators into account, with an open-loop inversion approach where robustness is considered [16] and using model predictive control for [22], where state and input constraints are taken into account.

For the dynamic approach, dynamical actuators can be taken into account (see [23, 24] and also [7] for the case of parallel interconnection of converters) in a way that the total effort distribution converges slowly to the optimal value. Even though [23] deals with input constraints, incorporating state constraints is still an open problem.

The geometric approach has been applied to the parallel interconnection of buck converters in [12], extended in the Hamiltonian framework in [14], and combined with an input constraints management in [25]. Note that (i) the exact knowledge of parameters is required to perform the change of coordinates and (ii) dealing with state constraints is still an open problem.

For the studied system, since dealing with current constraints is essential for the system safety, the most relevant method for this paper is the static one. Furthermore, it provides an optimality of the current distribution not only for the steady state but also for transients.

As a new contribution regarding the control allocation theory, the strategy of this work optimizes the current distribution for all time by exploiting the specific actuator dynamics. Rate saturations are taken into account as suggested in [22, 26]. Stability proofs are also provided in this paper, considering constraints and uncertainties.

The main contribution of this paper is to propose a new method, based on the static approach of control allocation, to control multiple heterogeneous buck converters connected in parallel. Most of the existing methods are not able to deal freely with the current distribution, and consequently, performance is restricted. Furthermore, stability of the existing controllers is rather involved. Papers [7, 12, 25] provide stability conditions with a free management of current distribution, but the current limits are not taken into account. With respect to those methods, the one presented in this paper: (i) ensures a fast response while maximizing efficiency by a free distribution of currents, including transients unlike previous methods (ii) guarantees stability under certain conditions with consideration to load uncertainty, converter dynamics, and input and current limits, and (iii) facilitates the predictable connection and disconnection of converters in real-time to accommodate large load variations or for maintenance.

The paper is structured as follows. In Section II, the problem is formalized with suitable assumptions. In Section III, basics of the control allocation theory are presented as well as an overview of the controller structure used in the paper. Section IV provides control design related to the current loop. In Section V, regulation of the output voltage is performed for an unknown resistive load. Finally, Section VI gives simula-

tion results, Section VII compares the resulting control law with existing ones, and experimental results are presented in Section VIII.

Terminology and Notation. In the sequel, the terms *converters* and *actuators* will be used indifferently, such as *load* and *plant*. The first terminology comes from the electrical power community, whereas the second from the control allocation literature. The notation x_j refers to the j-th element of vector x, with 1 being the index of the first element. The symbol $\mathbf{I}_m$ stands for the identity matrix of size $m \times m$. The null matrix of size $m \times n$ is denoted by $\mathbf{0}_{m\times n}$. The vector (column matrix) of size m for which every entry is 1 (respectively 0) is denoted by $\mathbf{1}_m$ (respectively $\mathbf{0}_m$). The operator "diag" creates a diagonal matrix from entries of its (vector) argument. In optimization problems, variables with a hat such as $\hat{i}$ constitute the optimization variables.

2. Problem statement

This paper is about controlling the electrical circuit shown in Figure 1, which corresponds to the parallel interconnection of m heterogeneous buck converters sharing a single capacitor C and a common resistive load R. The load is assumed to belong to some interval $\mathbb{L} \subset \mathbb{R}_{>0}$. R is unknown, as happens in most practical cases, and is assumed to be constant, although the control algorithm will compensate for slow variations or stepwise changes. The converters are controlled

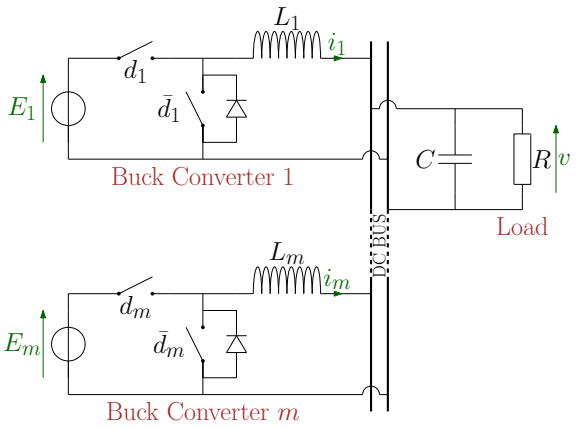

Figure 1: Electrical schematic of m buck converters.

via PWM signals where d_j refers to the duty cycle of the j-th converter. Index j belongs to the set $\mathcal{J} \coloneqq \{1, \dots, m\}$. The DC bus voltage is denoted v and the current in the j-th inductor, labelled L_j, is denoted i_j. The equivalent voltage sources of the converters have magnitudes E_j. Signals are sampled in the digital controller at a rate T_s and each output signal is converted by a zero-order hold.

Throughout this paper, it is assumed that (i) the switching period T_{PWM} is sufficiently small for the dynamics to be approximated by an average model, (ii) for each converter, the second switch is controlled in opposition with the first one, and (iii) electrical components and switches are ideals, i.e., parasitic elements (resistances, losses) can be neglected.

Considering the previous assumptions and using Kirchoff's laws, the dynamics of the circuit represented in Figure 1 are

$$\forall\, j \in \mathcal{J},\ L_j \frac{\mathrm{d}i_j}{\mathrm{d}t} = -v + E_j d_j, \tag{1a}$$

$$C\frac{\mathrm{d}v}{\mathrm{d}t} = \sigma - \frac{v}{R}, \tag{1b}$$

where

$$\sigma \coloneqq \sum_{j\in\mathcal{J}} i_j = \mathbf{1}_m^\intercal i, \tag{2}$$

refers to the total current. Eq. (1a) describes the dynamics of the inductor current produced by each converter, whereas (1b) describes the output voltage dynamics.

One way to consider the parallel interconnection of buck converters is to view each converter as an actuator, with the sum of the actuator outputs applied to a single-input single-output plant, or load. Eq. (1a) corresponds to the actuators model ($\mathcal{P}_a$), whereas ($\mathcal{P}$) constitutes the plant (1b). This decomposition (actuators/plant) is depicted on Figure 2.

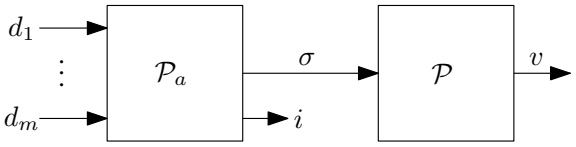

Figure 2: Actuators/plant decomposition.

The main control objective is to regulate the load voltage v to a reference value v_r. The previous decomposition (actuators/plant) shows that this voltage only depends on the total current σ. The way this current is distributed between the converters remains to be determined, and it is possible to choose the best distribution in order to satisfy the constraints and achieve a secondary objective. In this paper, the secondary objective is the minimization of converter losses. In [7], it was shown that the cost function associated with converter losses could be approximated by a quadratic function

$$J(i) \coloneqq \sum_{j=1}^{m} \left(r_{1,j} i_j^2 + r_{2,j} i_j\right), \tag{3}$$

where $\forall j \in \mathcal{J}$, $r_{1,j} \in \mathbb{R}_{\geq 0}$ and $r_{2,j} \in \mathbb{R}_{\geq 0}$ are coefficients depending on the converter and can be determined experimentally. Note that the larger $r_{1,j}$ or $r_{2,j}$ are, the less efficient the j-th converter is.

The problem addressed in this paper is to regulate the output voltage to the reference value v_r while minimizing the converter losses expressed by the cost function J. During the whole trajectory, input and state constraints must also be taken into account. One can express this problem as follows.

Problem 1. Design a load-robust state-feedback control law $(i, v) \mapsto d$ such that the closed-loop system admits a stable equilibrium for which $v = v_r$ holds, $J(i)$ is minimum and constraints $0 \leq d_j \leq 1$, $i_j^- \leq i_j \leq i_j^+$, $j \in \mathcal{J}$ are satisfied.

In the sequel, the controller design is carried out in discrete-time in order to get closer to the real application where a discrete-time controller is connected to the system.

3. Control allocation perspective

Control allocation methods consist in separating the control of the plant $\mathcal{P}$ from the distribution of effort among the actuators. The overall control scheme is represented in Figure 3 (see [15]) where:

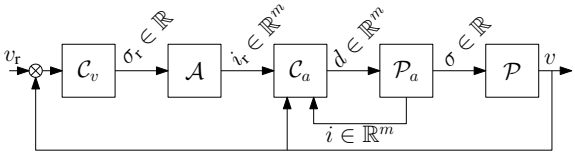

Figure 3: Schematic of the overall controller

- $\mathcal{C}_v$ is designed to control the output of the plant, or load voltage v in our case to its reference value v_r, by providing a global effort reference σ_r;
- $\mathcal{A}$ takes the total effort reference σ_r as an input and delivers suitable current references i_r to the actuators such that (i) the total current σ tracks σ_r and (ii) the converter losses are minimized according to (3);
- if needed, an internal controller $\mathcal{C}_a$ may be implemented to accelerate/stabilize the response of the actuators and delivers the duty cycle d by a internal feedback of currents i.

Following control allocation concepts [21], the control problem 1 is tackled in two parts:

Problem 2. Design a load-robust state-feedback control law $(i, v) \mapsto d$ such that, for all $R \in \mathbb{L}$

- a total current reference σ_r ensures the stable voltage tracking of a reference v_r,
- the total current reference is distributed to satisfy a criterion

$$
\begin{aligned}
i \in \underset{\hat{i} \in \mathbb{R}^m}{\operatorname{argmin}} \quad & \left(\sigma_r - \sum_{j \in \mathcal{J}} \hat{i}_j \right)^2 + \varepsilon J(\hat{i}) \\
\text{subject to} \quad & \forall j \in \mathcal{J}, \begin{cases} i_j^- \leq \hat{i}_j \leq i_j^+, \\ 0 \leq d_j \leq 1, \\ \text{(1a)}. \end{cases}
\end{aligned}
\tag{4}
$$

with $\varepsilon \in \mathbb{R}_{\geq 0}$, and where i_j^-, i_j^+ are the minimum and maximum currents that converter j is capable of delivering.

Note that the scalar ε has to be chosen sufficiently small in order to give priority to the first term. Indeed, the primary objective is to regulate the voltage v and is related to tracking by the total current σ of the total current reference σ_r (first term). When this first term is close to zero, the optimization will maximize efficiency as a secondary objective.

In the following sections, the designs of $\mathcal{C}_a$, $\mathcal{A}$ and $\mathcal{C}_v$ are presented. The controller $\mathcal{C}_a$ is designed to stabilize the actuators and make their response as fast as possible while considering input constraints [4]. Indeed, in our case, the goal is to stabilize the actuator dynamics which consist of integrators (1a). Then, an optimization algorithm is presented to solve (4) in the allocator block $\mathcal{A}$. Finally, the controller $\mathcal{C}_v$ is designed such that, without knowing the load value, the steady-state response satisfies $v^* = v_r$.

4. Current Control

Let T_s be the sampling period of the controller. For the sequel, the following assumption holds.

Assumption 1. *The output voltage v is constant over the period T_s.*

Indeed, because the output capacitor slows the voltage dynamics with respect to the currents, this is a realistic assumption. The approximation will be needed later for the incorporation of constraints.

4. Note that, in the case of static actuators, the internal controller $\mathcal{C}_a$ is not required because $\mathcal{P}_a$ reduces to an algebraic relationship.

4.1. Primary control $\mathcal{C}_a$

The discrete-time model for the converter dynamics is obtained from (1a) [5]

$$\mathcal{P}_{a,j}: \quad i_j[k+1] = i_j[k] + \frac{E_j}{L_j} T_s d_j[k] - \frac{T_s}{L_j} v[k]. \tag{5}$$

Note that (5) is not stable (the converters behave as integrators). The internal controller $\mathcal{C}_{a,j}$ aims to stabilize each converter while ensuring the convergence to a reference value $i_{r,j}$ such as in Figure 4. The concatenation of the internal controllers $\mathcal{C}_{a,j}$, $j \in \mathcal{J}$ forms the block $\mathcal{C}_a$ of Figure 3.

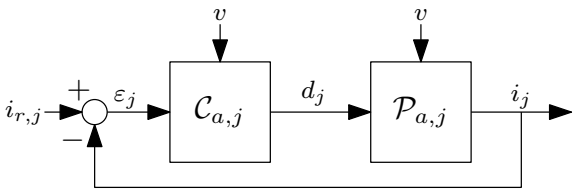

Figure 4: Primary controller.

To reach the reference value $i_{r,j}$ as rapidly as possible, a deadbeat controller is proposed. Reference values $i_{r,j}$ are updated at the period T_s. Hence, the objective for $\mathcal{C}_{a,j}$ is to make i_j reach exactly the reference value in one period T_s. The design problem of $\mathcal{C}_{a,j}$ consists in finding:

$$\mathcal{C}_{a,j}: \; i_{r,j}[k] \mapsto d_j[k] \text{ s.t. } \begin{cases} i_j[k+1] = i_{r,j}[k], \\ (5), \\ 0 \le d_j[k] \le 1. \end{cases} \tag{6}$$

Obviously, by assigning the value of $d_j[k]$ at 1 (respectively 0), the maximum attainable value $i_j[k+1]$ (respectively the minimum one) is obtained from an initial current $i_j[k]$. Since assumption 1 holds, those limits are given by

$$\Delta i_j^+ \coloneqq i_j[k+1] - i_j[k] = \frac{T_s}{L_j}(E_j - v[k]), \tag{7a}$$

$$\Delta i_j^- \coloneqq i_j[k+1] - i_j[k] = -\frac{T_s}{L_j} v[k], \tag{7b}$$

where (7a) and (7b) are deduced from (5) by setting $d_j = 1$ and 0, respectively.

The controller for the actuator, or primary controller, is designed as specified in the following lemma.

5. The discrete-time model of a continuous LTI model $\dot{x} = Ax + Bu$ is obtained by computing $x[(k+1)T_s] = e^{AT_s} x[kT_s] + \int_{kT_s}^{(k+1)T_s} e^{AT_s((k+1)T_s - \tau)} Bu(\tau) d\tau$ with a constant input because of the zero-order hold.

Lemma 1. Let the current control $\mathcal{C}_{a,j}$ be

$$d_j[k] = \frac{L_j}{E_j T_s} \varepsilon_j[k] + \frac{1}{E_j} v[k] \tag{8}$$

where $\varepsilon_j[k] \coloneqq i_{r,j}[k] - i_j[k]$.

The closed-loop transfer function of Figure 4 is such that the state i_j reaches the reference value $i_{r,j}$ in one sampling period T_s.

Proof. By using (8) with (5), one can obtain

$$i_j[k+1] = i_j[k] + \varepsilon_j[k] + \frac{T_s}{L_j} v[k] - \frac{T_s}{L_j} v[k].$$

Since $\varepsilon_j[k] \coloneqq i_{r,j}[k] - i_j[k]$, it follows that

$$i_j[k+1] = i_{r,j}[k],$$

which means that the state reaches the reference in one sampling period T_s.

4.2. Allocator $\mathcal{A}$

4.2.1. Principle

The aim of the allocator block (see Figure 3) is to distribute the total current reference σ_r among the available converters in such a way that: (i) every current reference is achievable for the primary controller $\mathcal{C}_a$ in one step and (ii) the cost function (3) is minimized. The problem to solve is (4) at the period T_s, with the solution providing the reference currents for the individual converters. In other words, for $k \in \mathbb{N}$,

$$\begin{bmatrix} i_{r,1} \\ \vdots \\ i_{r,m} \end{bmatrix} [k] \in \underset{\hat{i} \in \mathbb{R}^m}{\operatorname{argmin}} \left(\sigma_r[k] - \sum_{j=1}^{m} \hat{i}_j \right)^2 + \varepsilon J(\hat{i})$$
$$\text{subject to } \forall j \in \mathcal{J}, \begin{cases} i_j^- \le \hat{i}_j \le i_j^+, \\ 0 \le d_j[k] \le 1, \\ (5). \end{cases} \tag{9}$$

From the previous subsection and, in particular, from (7), constraints on duty cycles d_j are transferred to the currents, which are the decision variables of problem (9). This change makes it possible to gather the constraints via the following relationship $\forall j \in \mathcal{J}$,

$$\max\left(i_j^-, \Delta i_j^- + i_j[k]\right) \le \hat{i}_j \le \min\left(i_j^+, \Delta i_j^+ + i_j[k]\right)$$

where Δi_j^- and , Δi_j^+ are given by (7).

Algorithms can be found in the literature to solve quadratic problems with inequality constraints (see [27, Chapter 8], [28], [29], [30]). To apply these methods, J is rewritten as

$$J(i) = \sum_{j=1}^{m} r_{1,j} \left(i_j + \frac{r_{2,j}}{2 r_{1,j}} \right)^2 - \sum_{j=1}^{m} \frac{r_{2,j}^2}{4 r_{1,j}}.$$

Since $\sum_{j=1}^{m} \frac{r_{2,j}^2}{4r_{1,j}}$ is scalar, the minimum of J is reached for the same current values as the standard quadratic function (by setting their derivatives to zero)

$$\tilde{J}(i) \coloneqq \sum_{j=1}^{m} r_{1,j} \left(i_j + \frac{r_{2,j}}{2r_{1,j}} \right)^2 = \|W_r(i - i_p)\|_2^2$$

where

$$W_r \coloneqq \operatorname{diag} \left\{ \begin{bmatrix} \sqrt{r_{1,1}} \\ \vdots \\ \sqrt{r_{1,m}} \end{bmatrix} \right\}, \text{ and } i_p \coloneqq - \begin{bmatrix} \frac{r_{2,1}}{(2r_{1,1})} \\ \vdots \\ \frac{r_{2,m}}{(2r_{1,m})} \end{bmatrix}.$$

Furthermore, rewriting σ as in (2), problem (9) is transformed into the equivalent problem

$$\begin{bmatrix} i_{r,1} \\ \vdots \\ i_{r,m} \end{bmatrix} [k] \in \underset{\hat{i}}{\operatorname{argmin}} \left\| \begin{bmatrix} \mathbf{1}_m^\intercal \\ \sqrt{\varepsilon} W_r \end{bmatrix} \hat{i} - \begin{bmatrix} \sigma_r[k] \\ \sqrt{\varepsilon} W_r i_p \end{bmatrix} \right\|_2^2$$
$$\text{s.t. } \forall j \in \mathcal{J}, \max\left(i_j^-, \Delta i_j^- + i_j[k]\right) \leq \hat{i}_j \leq \min\left(i_j^+, \Delta i_j^+ + i_j[k]\right). \tag{10}$$

This equivalent problem can be solved using the active set methods presented in [31] and applied to control allocation in [27, Section 8.1]. An active set method solves a sequence of equality-constrained problems.

The first step of the sequence consists in solving the optimization problem without any constraints. If the given solution is achievable, i.e. the constraints are not violated, the solution is obtained and the algorithm stops. In the other case, a second step is necessary: the variables outside the constraints are set to the corresponding limits as equality constraints (corresponding to the working set $\mathcal{W}$ that specifies which actuators are saturated) and the algorithm solves the optimization problem on the remaining variables by disregarding the constraints. If the solution is still not feasible, the step is performed again, until a feasible solution is obtained. If the solution is feasible, the algorithm moves to the third step: some of the inequalities are now removed (one by one) to determine if the optimization can be improved with fewer variables at their limits. Note that this third step is only required if the previous step set at least two equality constraints at a time. The experiments of this paper use a Matlab toolbox available on-line in [32]. For the initialization of the algorithm, i^0 was chosen to be the zero vector at the first iteration, and the solution at the previous time step otherwise. The working set was initialized at $\mathcal{W} = \mathbf{0}_m$.

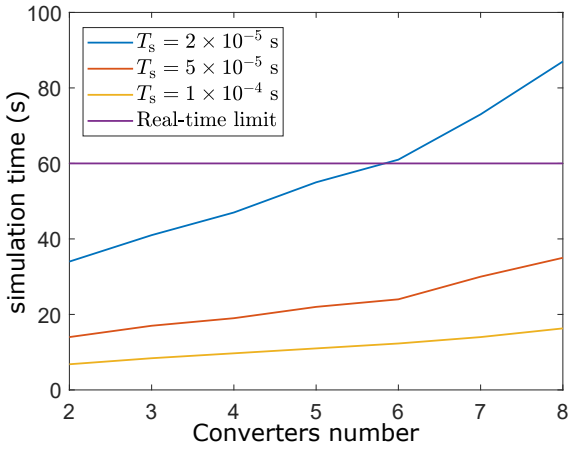

Figure 5: Simulation time evolution with respect to the number of converters.

4.2.2. Speed of convergence

In order to provide information about the possible implementation of this algorithm in real-time, the following simulations are given.

Environment. The following tests have been performed on a *Lenovo Yoga 710* having an *Intel Core i7* processor and a RAM of 8GB. The algorithm is implemented on *MATLAB/SIMULINK 2018a* using a *matlab-function* block.

Test. The simulation concerns the estimation of the mean time over a whole simulation for the computation of the algorithm. The simulation time is $T_f = 60$s, and the algorithm is computed for the following three sampling times : (i) $T_s = 2 \times 10^{-5}$s, (ii) $T_s = 5 \times 10^{-5}$s and $T_s = 1 \times 10^{-4}$s. For those three cases and for a number of converters growing from 2 to 8, the total simulation time of the controller is measured. Results are given on Figure 5. For a simulation time of T_f =60s, the computation time have to be less than 60s to use the algorithm in real time. This limit is depicted by the purple line. For the sampling time $T_s = 10^{-4}$s that will be used for the experiments, we see on this figure that it is possible to use more than 8 converters.

5. Voltage control $\mathcal{C}_v$

The voltage controller aims to regulate the output voltage v to its reference value v_r by specifying the total current reference σ_r (see Figure 3).

5.1. Internal loop behaviour

This subsection focuses on the characteristics of the internal loop, namely constraints and dynamic behavior, in order to take them into account when designing the voltage controller.

5.1.1. Internal loop constraints

The constraints of the allocator $\mathcal{A}$ are considered in two steps:

- the magnitude constraints, coming from the limits on the converter currents, specify that

$$\sigma_{\min} := \sum_{j=1}^{m} i_j^- \leq \sigma_r[k] \leq \sum_{j=1}^{m} i_j^+ =: \sigma_{\max}; \tag{11}$$

- the rate constraints, coming from duty cycle limits and converted into current limits assuming the deadbeat controller of Section 4, specify that (using (7))

$$\sigma^-(v) \leq \underbrace{\sigma_r[k] - \sigma_r[k-1]}_{=:\Delta\sigma_r[k]} \leq \sigma^+(v), \tag{12}$$

where

$$\sigma^+(v) := \sum_{j=1}^{m} \frac{T_s}{L_j}(E_j - v[k]) \text{ and}$$

$$\sigma^-(v) := -\sum_{j=1}^{m} \frac{T_s}{L_j} v[k].$$

By defining σ_c as the constrained reference value of the total current (see Figure 6), the constraints management provided by the allocator can be seen as a saturation block, such as on Figure 6.

Remark 1 (Rate constraints). *In the literature, sufficient conditions are given for the anti-windup problem with constant magnitude and rate constraints for discrete-time systems (see [33]). However, this problem is much more difficult when those constraints are state-dependent. This case applies here, since rate variations depend on the voltage v (see (12)). Giving a complete answer to this problem is out of the scope of this paper. Accordingly, the anti-windup scheme used here takes into account magnitude constraints only, even though the control allocator considers both the magnitude and rate constraints.*

5.1.2. Internal loop dynamics

Consider the internal dynamics ($\mathcal{C}_a$ and $\mathcal{P}_a$) at the sampling period T_s defined in section 4. The deadbeat controller presented in subsection 4.1 ensures that each current evolves linearly as a function of time. As a result, knowing that the total current σ is the sum of the currents i_j, the allocator ensures that $\sum_j i_{r,j}(kT_s)$ corresponds to $\sigma_c(kT_s)$. Furthermore, since σ needs a time T_s to reach its reference value, the recurrence relationship between σ and σ_c is

$$\sigma[(k+1)T_s] = \sigma_c[kT_s].$$

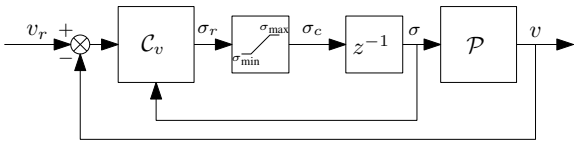

Figure 6: Outer voltage control loop.

Therefore,

$$\sigma(t) = \sigma(kT_s) + \frac{\sigma_c(kT_s) - \sigma(kT_s)}{T_s}(t - kT_s) \tag{13}$$

holds.

Considering σ as a virtual (not constant) input for the voltage dynamics, from (1b), the discrete-time model is given by

$$v[(k+1)T_s] = e^{-\frac{T_s}{RC}} v[kT_s] + \frac{1}{C}\int_{kT_s}^{(k+1)T_s} e^{-\frac{1}{RC}((k+1)T_s - \tau)}\sigma(\tau)d\tau.$$

With (13), one can obtain through integration by parts the discrete-time model at the period T_s described on Figure 6 with dynamics

$$\begin{bmatrix} v \\ \sigma \end{bmatrix}[k+1] = A(R)\begin{bmatrix} v \\ \sigma \end{bmatrix}[k] + B(R)\sigma_c[k] \tag{14}$$

where

$$A(R) := \begin{bmatrix} e^{-\frac{T_s}{RC}} & R\left(\frac{RC}{T_s} - e^{-\frac{T_s}{RC}}\left(1 + \frac{RC}{T_s}\right)\right) \\ 0 & 0 \end{bmatrix},$$

$$B(R) := \begin{bmatrix} R - \frac{R^2C}{T_s}\left(1 - e^{-\frac{T_s}{RC}}\right) \\ 1 \end{bmatrix},$$

together with (11) and where σ_c is the saturated input. The first row of the model corresponds to the time discretization of (1b) at the sampling period T_s with (13), whereas the second row corresponds to the delay introduced by the internal loop (the converter with its internal controller), as depicted on Figure 6.

5.2. Controller for the unsaturated system

First, a controller $\mathcal{C}_v$ is designed without taking saturations into account. Integral action is included in $\mathcal{C}_v$ in order to cope with errors coming from the internal controller and to compensate for load disturbances. Afterwards, a scheme is designed to prevent windup when the limits are reached.

The aim of this subsection is to design a controller for the voltage dynamics (14) which ensures the stability of the equilibrium point v_r for all $R \in \mathbb{L} := [R^-, R^+]$ where $R^- \in \mathbb{R}_{>0}$ and

$R^+ \in \mathbb{R}_{>0}$ correspond respectively to the lower and upper values that R can take. As a first step, saturation of the signal σ_r is disregarded, so that $\sigma_c = \sigma_r$.

The load-robust state-feedback control law with an output integrator is given by

$$\mathcal{C}_v : \begin{cases} \xi[k+1] &= \xi[k] + v_r - v[k] \\ \sigma_r[k] &= k_\xi \xi[k] + k_p\,(v_r - v[k]) + k_\sigma \sigma[k], \end{cases} \tag{15}$$

where $k_p \in \mathbb{R}$, $k_\xi \in \mathbb{R}$ and $k_\sigma \in \mathbb{R}$ are the proportional, integral and derivative gains of the control law, respectively. The model (14) with (15) corresponds to the following extended model

$$\begin{bmatrix} \tilde{v} \\ \tilde{\sigma} \\ \tilde{\xi} \end{bmatrix}[k+1] = \underbrace{\left(A_e(R) + B_e(R) \begin{bmatrix} -k_p \\ k_\sigma \\ k_\xi \end{bmatrix}^\intercal \right)}_{A_{BF}(R) := A_e(R) + B_e(R)K} \begin{bmatrix} \tilde{v} \\ \tilde{\sigma} \\ \tilde{\xi} \end{bmatrix}[k]. \tag{16}$$

with

$$A_e(R) \coloneqq \begin{bmatrix} A(R) & \mathbf{0}_{2\times 1} \\ [-1 \quad 0] & 1 \end{bmatrix}, \; B_e(R) \coloneqq \begin{bmatrix} B(R) \\ 0 \end{bmatrix}$$

and

$$\tilde{v} = v - v_r, \; \tilde{\sigma} = \sigma - \frac{v_r}{R} \text{ and } \tilde{\xi} = \xi - \frac{1 - k_\sigma}{R k_\xi} v_r.$$

The extended state matrices $A_e(R)$ and $B_e(R)$ depend on the unknown parameter, namely the load R. However, since R belongs to the compact set $\mathbb{L}$ and since the elements of $A_e(R)$ and $B_e(R)$ are continuous with respect to R, one can always find a convex hull in which $[A_e(R), B_e(R)]$ belong. In other words, for all $R \in \mathbb{L}$

$$[A_e(R), B_e(R)] \in \mathcal{H} \coloneqq \text{co}\left\{ [A_i, B_i]_{i \in \{1,\dots,n_v\}} \right\}$$

where n_v corresponds to the number of convex hull vertices. A possible choice of convex hull for our application is given in Appendix A.

Once $\mathcal{H}$ is computed, the following proposition shows that solving LMIs for the convex hull vertices ensures stability for the closed-loop system (16) for all $R \in \mathbb{L}$.

Proposition 1. If there exists a positive definite matrix $W = W^\intercal \in \mathbb{R}^{3\times 3}$ and $Y \in \mathbb{R}^{1\times 3}$ such that

$$\begin{bmatrix} -W & A_i W + B_i Y \\ (A_i W + B_i Y)^\intercal & -W \end{bmatrix} \prec 0 \tag{17}$$

holds for all the vertices $[A_i, B_i]$ of the convex hull $\mathcal{H}$, then the feedback gains satisfying

$$\begin{bmatrix} -k_p & k_\sigma & k_\xi \end{bmatrix} = Y W^{-1}$$

ensure that the fixed point

$$(v, \sigma, \xi) = (v_r, \frac{v_r}{R}, \frac{1 - k_\sigma}{R k_\xi} v_r)$$

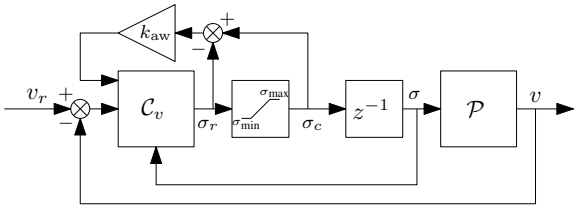

Figure 7: Anti-windup action.

is an exponentially stable equilibrium state of (16) for all $R \in \mathbb{L}$.

The proof is given in Appendix B.

Note that this proposition gives a sufficient condition. It is possible that some control gains which do not respect the LMI condition can still ensure stability of the equilibrium for all $R \in \mathbb{L}$.

5.3. Anti-windup design

The presence of magnitude constraints on the input signal not only reduces achievable performance, but could also destabilize the closed-loop system. One way to deal with this issue is to add an anti-windup scheme such as the one shown in Figure 7 (see [34]). The basic idea underlying this design is to introduce control modifications when a saturation is activated in order to recover, as much as possible, the performance achieved by the unsaturated system. Note that static and dynamic anti-windup methods exist but, for the sake of simplicity, we focus here on a static anti-windup approach. The controller (15) is modified as follows

$$\begin{cases} \xi[k+1] &= \xi[k] + v_r - v[k] + k_{\text{aw}}\,(\sigma_c[k] - \sigma_r[k]) \\ \sigma_r[k] &= k_\xi \xi[k] + k_p\,(v_r - v[k]) + k_\sigma \sigma[k], \end{cases}$$

From Figure 6 and Proposition 1, the following equalities hold at the equilibrium and in the unsaturated condition

$$\sigma_r = \sigma_c = \sigma = \frac{v_r}{R}.$$

As a result, let us define

$$\tilde{\sigma}_r[k] = \sigma_r[k] - \frac{v_r}{R} \text{ and } \tilde{\sigma}_c[k] = \sigma_c[k] - \frac{v_r}{R},$$

which is such that the closed-loop dynamics (16) become

$$\begin{bmatrix} \tilde{v} \\ \tilde{\sigma} \\ \tilde{\xi} \end{bmatrix}[k+1] = A_{BF}(R) \begin{bmatrix} \tilde{v} \\ \tilde{\sigma} \\ \tilde{\xi} \end{bmatrix}[k] + \begin{bmatrix} 0 \\ 0 \\ k_{\text{aw}} \end{bmatrix} (\tilde{\sigma}_c[k] - \tilde{\sigma}_r[k]). \tag{18}$$

Expressing the constraints on the modified control value $\tilde{\sigma}_r$ leads to the following relationship

$$\begin{aligned}\tilde{\sigma}_{\min}(R) \coloneqq \sigma_{\min} - \frac{v_r}{R} \\ \leq \tilde{\sigma}_r[k] \leq \\ \sigma_{\max} - \frac{v_r}{R} =: \tilde{\sigma}_{\max}(R).\end{aligned}$$

Note that the problem under consideration is such that $\tilde{\sigma}_{\min}(R) \neq -\tilde{\sigma}_{\max}(R)$. However, the anti-windup design problem is usually tackled in the literature for symmetric saturations. Stability conditions with asymmetric constraints can be obtained by reducing the achievable interval to the largest symmetric interval contained in $[\tilde{\sigma}_{\min}(R),\ \tilde{\sigma}_{\max}(R)]$, though doing so reduces the achievable performance.

Given v_r, denote by $\tilde{\sigma}_0$ the bound of the largest symmetric saturations contained in $[\tilde{\sigma}_{\min}(R),\ \tilde{\sigma}_{\max}(R)]$ for all $R \in \mathbb{L}$, i.e.

$$\tilde{\sigma}_0 = \min\left(-\sigma_{\min} + \frac{v_r}{R^+}, \sigma_{\max} - \frac{v_r}{R^-}\right)$$

In the sequel, $\tilde{\sigma}_r[k]$ is restricted to lie within the interval $[-\tilde{\sigma}_0, \tilde{\sigma}_0]$. From [35], if there exist a symmetric positive definite matrix $\Omega \in \mathbb{R}^{3\times3}$, a matrix $\Gamma \in \mathbb{R}^{1\times3}$, a scalar $Z \in \mathbb{R}$ and $S \in \mathbb{R}_{>0}$ satisfying the inequality

$$\begin{bmatrix} \Omega & -\Gamma^\intercal & -\Omega(A_i + B_iK)^\intercal \\ & 2S & SB_i^\intercal + Z^\intercal B_{\text{aw}}^\intercal \\ & * & \Omega \end{bmatrix} \succ 0 \\ \begin{bmatrix} \Omega & \Omega K^\intercal - \Gamma \\ K\Omega - \Gamma & (\tilde{\sigma}_0)^2 \end{bmatrix} \succeq 0, \tag{19}$$

with

$$B_{\text{aw}} \coloneqq \begin{bmatrix}0 & 0 & 1\end{bmatrix}^\intercal \text{ and } K = \begin{bmatrix}-k_p & k_\sigma & k_\xi\end{bmatrix}$$

for all $[A_i, B_i]$, $i \in \{1, \dots, n_v\}$ corresponding to the vertices of the convex hull $\mathcal{H}$, then the gain $k_{\text{aw}} = \dfrac{Z}{S}$ ensures that the ellipsoid $\Upsilon(P) = \left\{\zeta \in \mathbb{R}^{3\times3};\ \zeta^\intercal P \zeta \leq 1\right\}$, with $P = \Omega^{-1}$, is a region of exponential stability for the closed-loop system (18). The proof is based on summing the LMIs for $i \in \{1, \dots, n_v\}$ and on Schur complements in order to remove products of variables. The second inequality of (19) ensures that the dead-zone implies that the sector condition is verified. It can be proved using another Schur complement. The proof is detailed in [35, Theorem 1]. More information about the estimated basin of attraction are given in [36].

The maximization of the estimated basin of attraction in the direction of the integral state ξ is chosen in order to optimize the choice of anti-windup gain k_{aw}. The result is achieved by solving the optimization problem

$$\begin{aligned} \min_{\Omega,\Gamma,Z,S,\beta} \quad & -\beta \\ \text{subject to} \quad & (19) \text{ and } \begin{bmatrix} 1 & \beta\nu^\intercal \\ \beta\nu & \Omega \end{bmatrix} \succeq 0 \end{aligned} \tag{20}$$

where $\nu \coloneqq \begin{bmatrix}0 & 0 & 1\end{bmatrix}^\intercal$ corresponds to the direction of the integral state.

6. Simulations

6.1. Simulation setup

Two simulations are given where only the current limits are different in order to highlight their management to prioritize the voltage regulation. A system with six identical converters (i.e. $m = 6$) is considered with the following parameters:

- $(E_j)_{j\in\{1,\dots,6\}} = 24$ V;
- $(L_j)_{j\in\{1,\dots,6\}} = 2$ mH.

Furthermore, the capacitor is set to $C = 2$ mF, the resistive load is $R = 2\ \Omega$, the sampling period $T_s = 10^{-4}$ s, the simulation period $T_{\text{sim}} = 10^{-5}$ s and the simulation time $t_f = 24$ ms.

For the first simulation, current limits are set to

- $(i_j^-)_{j\in\{1,\dots,6\}} = 0$ A;
- $(i_j^+)_{j\in\{1,\dots,6\}} = 12$ A;

whereas they are set to

- $(i_j^-)_{j\in\{1,\dots,6\}} = 0$ A;
- $(i_j^+)_{j\in\{1,\dots,6\}} = 3$ A;

for the second simulation.

Primary controller:

According to Section 4, the duty cycles are given by the following relations for all $j \in \mathcal{J}$:

$$d_j[k] = \frac{10}{12}(i_{r,j}[k] - i_j[k]) + \frac{1}{24}v[k]$$

Allocator:

Problem (10) is implemented with $\varepsilon = 10^{-6}$. The script *wlsq_alloc.m* of the toolbox given in [32] computes the solution of this optimization problem at each time.

Voltage controller:

Following the approach of section 5, the control gains are

$$k_p = -4,\ k_\sigma = 1 \text{ and } k_\xi = 0.05$$

whereas the anti-windup gain was given the value of $k_{\text{aw}} = 6.8$.

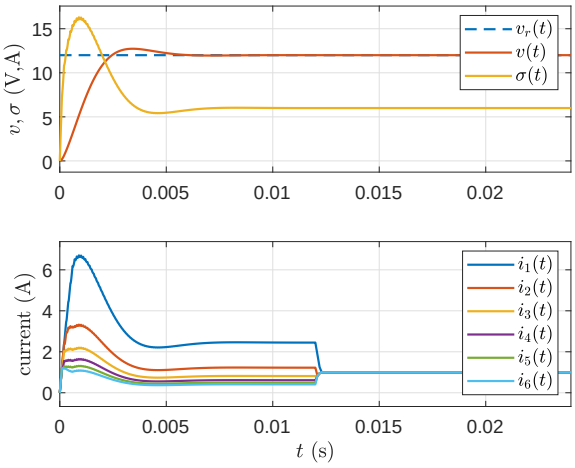

Figure 8: Voltage v with its reference, total current σ and currents i_k, when $(i_j^+)_{j\in\{1,\dots,6\}} = 12$ A holds.

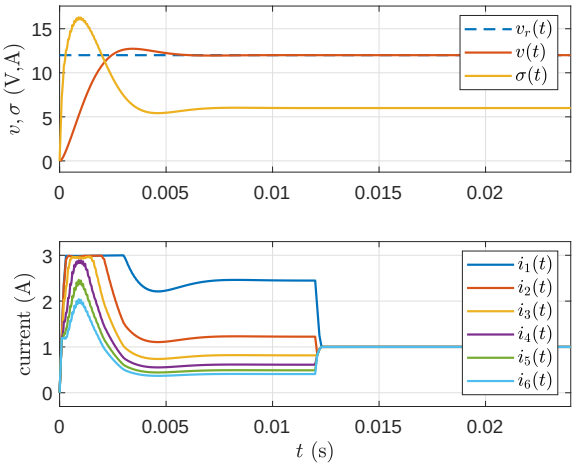

Figure 9: Voltage v with its reference, total current σ and currents i_k, when $(i_j^+)_{j\in\{1,\dots,6\}} = 3$ A holds.

6.2. Environment

The control objectives are the following: (i) regulate the output voltage v to the reference $v_r = 12$ V and (ii) impose an optimal current distribution through the branches with respect to the cost function J. For the simulations, J is not the expression of converters losses but an example chosen to highlight the convergence of the control algorithm to the optimal strategy. The parameters are defined as follows:

- $r_{1,j}(t)_{j\in\{1,\dots,6\}} = \begin{cases} j, & t \in [0; t_f/2) \text{ s} \\ 1, & t \in [t_f/2; t_f] \text{ s} \end{cases}$;
- $(r_{2,j})_{j\in\{1,\dots,6\}} = 0.1$.

As a result, for the first half of the simulations, the desired current distribution is to carry more current in the first converters than in the last one. This is due to the fact that $r_{1,j}$ is larger when j grows, meaning that priority is given to the first converters to carry the power. Conversely, for the second half of the simulation, the converters should share the same fraction of the total current, which is the expected behaviour since both $r_{1,j}$ and $r_{2,j}$ are identical for every converter. Thereby, those simulations highlight the convergence of the control law to the minimum value of J.

6.3. Results

Figures 8 and 9 show the output voltage, the total current and the currents in every converter when the upper current limits are set to 12 A and to 3 A, respectively. In the first half of the simulation, Figures 8 and 9 show that as long it is possible, the first converters are prioritized to feed the load, whereas the distribution is uniform in the second half, as expected. Even during the first transient, Figure 8 indicates that the current distribution is optimal with respect to J. This is not the case when the current constraints come into play, as in Figure 9. However, it is important to note that this current distribution is not optimal anymore in order to respect the voltage tracking imposed by $\mathcal{C}_v$. Indeed, the total current σ and the voltage v of Figure 9 have exactly the same trajectories as on Figure 8, when $(i_j^+)_{j\in\{1,\dots,6\}} = 12$ A, while respecting the current constraints.

Furthermore, for the whole simulation time, the output voltage v is properly regulated at the reference value $v_r = 12$ V. Observe that, at $t = t_f/2$ when the current distribution objective changes, the total current and voltage values are left unchanged.

Those observations clearly highlight that the secondary objective (current distribution) is achieved while always giving priority to the foremost objective: voltage regulation.

7. Comparison with [12, 25]

7.1. Simulation setup

A system with two identical converters (i.e. $m = 2$) is considered with the parameters given in Table 1.

7.2. Control law of [12, 25]

The control law of [12] is robust to load uncertainties but does not take input constraints into account. Conversely, the control law of [25] is not robust to load uncertainties but considers input constraints. To be fair, we provide here a load robust control law with input constraints management, putting each control law together

Table 1: Comparison bench parameters

Table 1-A: converters parameters

Parameters	$j=1$	$j=2$
E_j (V)	24	24
L_j (mH)	2	20
$r_{1,j}$	1	2
$r_{2,j}$	0	0
i_j^- (A)	0	0
i_j^+ (A)	8	8

Table 1-B: other parameters

Parameters	Values
Capacitor C	5 mF
Lower resistive bound R^-	1 Ω
Upper resistive bound R^+	3 Ω
Sampling period T_s	100 μs
Simulation period T_{sim}	10 μs
Sampling time t_f	24 ms

and adding an anti-windup scheme. The resulting control law is expressed by

$$\begin{aligned}
\dot{z} &= v_r - v + k_{\text{aw}}(\mu - \mu_s)\\
\mu &= k_i z + k_p(v_r - v) + k_d\sigma\\
\mu_s &= \begin{cases} 0, & \mu < 0\\ \mu, & 0 \le \mu \le 1\\ 1, & \mu > 1 \end{cases}\\
\lambda &= v - k_\delta\left(\frac{r_{1,2}-r_{1,1}}{r_{1,1}+r_{1,2}}\sigma - \delta\right)\\
\lambda_s &= \begin{cases} \underline{\lambda}(\mu_s), & \lambda < \underline{\lambda}(\mu_s)\\ \lambda, & \underline{\lambda}(\mu_s) \le \lambda \le \overline{\lambda}(\mu_s)\\ \overline{\lambda}(\mu_s), & \lambda > \overline{\lambda}(\mu_s) \end{cases}\\
d_1 &= \frac{L_2-L_1}{L_2}\frac{\lambda_s}{2E_1} + \frac{L_1+L_2}{L_2}\mu_s\\
d_2 &= \frac{L_1-L_2}{L_1}\frac{\lambda_s}{2E_1} + \frac{L_1+L_2}{L_1}\mu_s
\end{aligned}$$

where

$$\underline{\lambda}(\mu) = \max\left(-m\frac{E_2}{L_2} + E_1\frac{L_1+L_2}{L_1L_2}\mu, -E_1\frac{L_1+L_2}{L_1L_2}\mu\right)$$

$$\overline{\lambda}(\mu) = \min\left(m\frac{E_1}{L_1} - E_1\frac{L_1+L_2}{L_1L_2}\mu, E_1\frac{L_1+L_2}{L_1L_2}\mu\right)$$

and $k_i = -16.34$, $k_p = -0.062$, $k_d = -0.072$, $k_{\text{aw}} = 5.97$ and $k_\delta = -8.89$. For more details about this control law, the interested reader is referred to [12, 25].

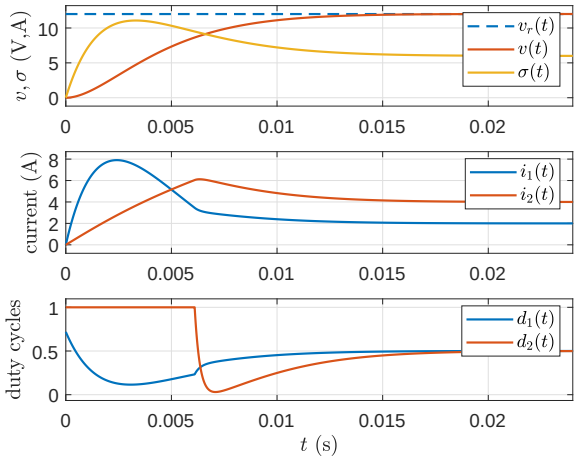

Figure 10: Simulation for the control law of [12, 25].

7.3. Proposed control law

Primary controller:

According to Section 4, the duty cycle commands are given by (8).

Allocator:

Problem (10) is implemented with $\varepsilon = 10^{-6}$. The script *wlsq_alloc.m* of the toolbox given in [32] computes the solution of this optimization problem at each time instant.

Voltage controller:

Following the approach of section 5, the control gains are

$$k_p = -4,\ k_\sigma = 1 \text{ and } k_\xi = 0.05$$

whereas the anti-windup gain was given the value of $k_{\text{aw}} = 1.44$.

7.4. Environment

The control objectives are: (i) to regulate the output voltage v to the reference $v_r = 12$ V and (ii) to impose an optimal current distribution through the branches with respect to the cost function J. As in section 6, for this comparison, J is not the expression of converter losses but an academic example designed to highlight the convergence of the control algorithm to the optimal value. Its parameters are given in Table 1.

7.5. Results

Figures 10 and 11 depict trajectories of the output voltage, the total current, the currents in every converter and the duty cycles for the control law of [12, 25] and the control law of this paper, respectively.

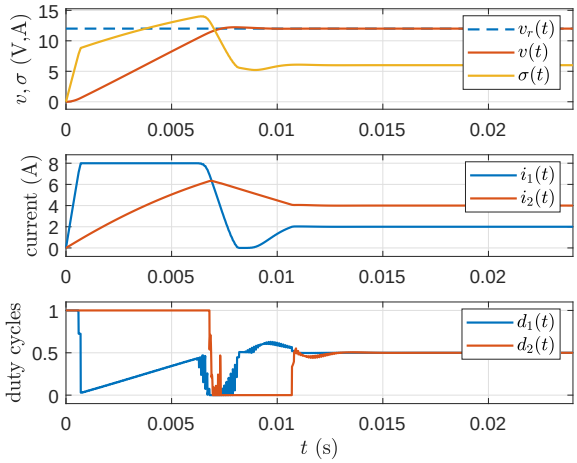

Figure 11: Simulation for the proposed control law.

About Figure 10

Note that gains of the control law of [12, 25] have been carefully chosen in order that (i) v converges as fast as possible to its reference value with a negligible overshoot and (ii) currents do not exceed 8A for the simulation environment. About (i), i.e. convergence speed, let us stress that the duty cycle of the second converter is set to one during the transient so that the current of the second converter cannot grow faster. For the first converter, applying a larger duty cycle at the very beginning will necessarily drive i_1 to exceed 8A in the transient. Thus, with this linear control law, it is not possible to accelerate the response fo the first converter while respecting the current constraint.

About Figure 11

Because the proposed control law is able to properly limit the current value, the speed of convergence of v can be substantially increased. Indeed, Figure 11 shows that d_1 is set to one as long as i_1 is smaller than its limit. So, i_1 cannot reach 8A faster than on Figure 11. Simultaneously, d_2 is set to 1 for all the transient, so that i_2 cannot grow faster. As a result, it does not seem possible for v to converge faster to its reference than as shown on Figure 11. Note that the anti-windup structure ensures a negligible voltage overshoot by rapidly decreasing i_1 to 0. This simulation also highlights that the lower limit of i_1 is respected.

To conclude, the trajectory of v shows that it reaches its reference around 0.0125s in Figure 10 and around 0.0075s in Figure 11. Thus, the proposed control law is faster than the one of [12, 25]. Furthermore, both current and input constraints are respected in the proposed control law, whereas it is not the case for the one of [12, 25]. Indeed, if the comparison environment changes (by setting $v_r = 16$V for instance), the current constraint for the method of [12, 25] will be violated whereas it will be satisfied in the case of the proposed control law.

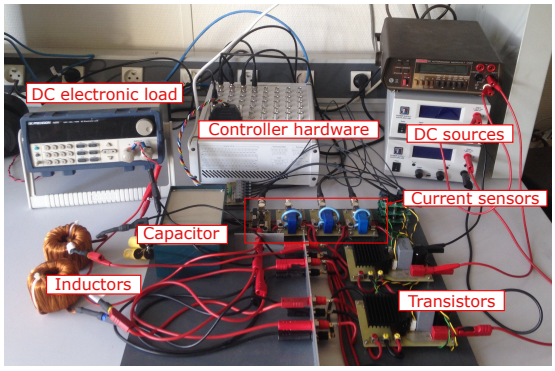

Figure 12: Experimental setup

8. Experiments

8.1. Experimental setup

Experiments were performed to demonstrate the effectiveness of the proposed approach. The experimental setup is shown on Figure 12 and is composed of 2 buck converters ($m = 2$) with different inductors connected to a single variable resistive load with a parallel capacitor. The inductors are such that $L_1 < L_2$. From (1a), it is clear that the first converter reacts faster than the second one (L_1 is smaller that L_2), but the latter has a higher efficiency. Indeed, for the same PWM period, the larger the inductor is, the less ripple it induces, so that its conduction losses are smaller.

The following observation is of major interest for the application and to understand the experiments. When none of the constraints are reached, the control algorithm tries to obtain the desire current distribution, i.e. the one that minimizes the losses and favors the slow converter. During transients, this slow converter is not able to provide the power sufficiently fast because of the constraints. By the optimal management of the constraints, the fast converter will automatically provide the desired power during transients. This feature allows one to use at the same time the efficiency of the second converter (for the steady state) and the capability of the first one (for the transient). Thereby, we obtain a fast device with a good efficiency. The expected result is that the second converter will be favored to deliver the output current in steady-state, but the first converter will be used to deliver the transient current needed to rapidly bring the output voltage to the reference.

The controller hardware is a dSPACE MicroLabBox. The control objectives are to: (i) regulate the output voltage v to the reference $v_r = 12$ V and (ii) impose an optimal current distribution through the branches with respect to the cost function J, reflecting the power losses. Load variations are commanded by a programmable DC electronic load BK Precision 8600 series with a maximum power of 150 W and controlled by the dSPACE board. The bench parameters are listed in Table 2.

Table 2: Experimental bench parameters

Table 2-A: converters parameters

Parameters	$j=1$	$j=2$
E_j (V)	24	24
L_j (mH)	0.4	4.13
$r_{1,j}$	4	1
$r_{2,j}$	0.1	0.1
i_j^- (A)	0	0
i_j^+ (A)	10	12

Table 2-B: other parameters

Parameters	Values
Switching period T_{PWM}	20 μs
Sampling period T_s	200 μs
Capacitor C	22 mF
Lower resistive bound R^-	1 Ω
Upper resistive bound R^+	12 Ω

Because $r_{1,1} > r_{1,2}$, the second converter is more efficient up to some current level depending on the quadratic term. The lower efficiency of the first converter is due to the fact that the ripple conduction losses are bigger for a smaller inductor.

Primary controller

According to Section 4, the duty cycle commands are given by the following equations

$$\begin{bmatrix} d_1 \\ d_2 \end{bmatrix}[k] = \begin{bmatrix} 1/E_1 \\ 1/E_2 \end{bmatrix} v[k] + \frac{1}{T_s}\begin{bmatrix} L_1/E_1 & 0 \\ 0 & L_2/E_2 \end{bmatrix}\begin{bmatrix} i_{r,1}[k]-i_1[k] \\ i_{r,2}[k]-i_2[k] \end{bmatrix}.$$

The value of L_1/E_1 was experimentally determined to fit the real behavior of inductor L_1 which is not well-known.

Allocator

Problem (10) is implemented with $\varepsilon = 10^{-6}$. The script *wlsq_alloc.m* of the toolbox given in [32] computes the solution of this optimization problem in real-time.

Voltage controller

Following the approach of Section 5, the controller gains are

$$k_p = 4,\ k_\sigma = 0.8 \text{ and } k_\xi = 0.4$$

whereas the anti-windup gain was given the value of $k_{\text{aw}} = 3$. The chosen controller gains solve Proposition 1. The anti-windup gain was chosen experimentally because (19) needed to be relaxed to improve closed-loop behavior. Furthermore, for the experiment, the constraint $\tilde{\sigma}_r \in [-\tilde{\sigma}_0, \tilde{\sigma}_0]$ was relaxed to $\tilde{\sigma}_r \in [\tilde{\sigma}_{\min}(R),\ \tilde{\sigma}_{\max}(R)]$ in order to optimize the system performance, even though the theoretical stability guarantees were lost. The chosen anti-windup gain is about ten times larger than the one given by the theory. Note that the one given is probably not the optimal value that satisfy (19).

8.2. Experiments

Two experiments are performed. The first one aims to demonstrate the controller performance in the transient and steady state regimes. The second experiment shows that this approach makes it possible to easily switch off a converter in order to unplug it while still supplying the load with the other converter.

8.2.1. Experiment 1

Starting from zero initial conditions, the experiment is divided in three parts.

1. $t \in [0, 0.05)$ s: the resistive load is set to $R = 1\ \Omega$.
2. $t \in [0.05, 0.1)$ s: the load suddenly switches to $R = 12\ \Omega$.
3. $t \in [0.1, 0.15]$ s: the load changes back to the value $R = 1\ \Omega$.

The controller aims to have the output voltage reach v_r as fast as possible at the start of the experiment, and to maintain this voltage afterwards. This experiment gives the responses for the system start and for step decrease and increase of the load value.

8.2.2. Experiment 2

At the beginning, the system is operating with a load value $R = 6\ \Omega$ and with the optimal current distribution with respect to J. At $t = 5$ ms, the first row in the cost function in the optimization problem (10) is replaced by $i_2 - \sigma_r$ so that i_1 is driven to zero. As a matter of fact, this modification implies that all the power required by the load is fed by the second converter. The current i_1 is now free to reach its preferred value

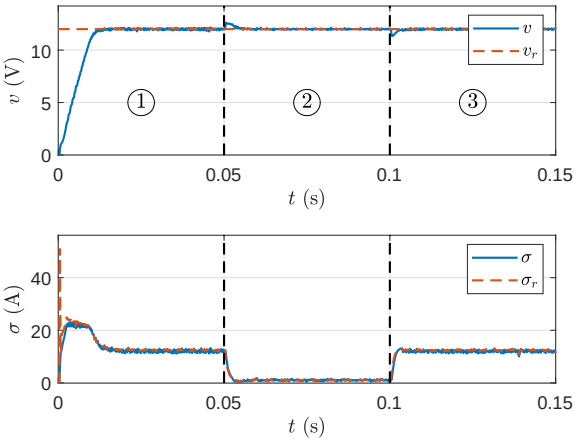

Figure 13: Voltage v and total current σ with their references.

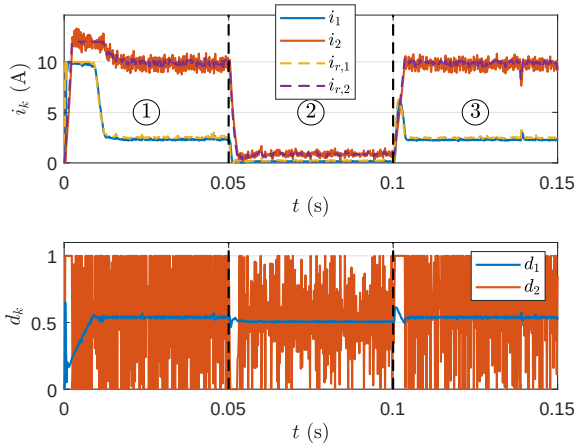

Figure 14: Currents i_k and duty cycles d_k with current references

$i_p = -[0.0125,\ 0.05]^\intercal$. However i_p is negative and the lower limit $i_{\min,1} = 0$ A. Consequently, i_1 is automatically brought to zero. This simple change in the algorithm makes it possible to unplug the first converter.

8.3. Results

8.3.1. Experiment 1

Figure 13 shows the output voltage, the total current reference and the total current. The blue line of the upper sub-plot corresponds to the voltage response whereas the red dashed line is the voltage reference value v_r. The blue line of the lower sub-plot shows the total current σ. The total current reference σ_r corresponds to the red dashed curve.

Due to the saturation management of the allocator, the total current is saturated to $\sigma_{\max} = 22$ A at the beginning. The anti-windup component prevents the voltage response from exceeding its limit. At $t = 0.05$ s, the voltage rises slightly due to the drop in load value, but the compensator rapidly returns the voltage to its reference value. At $t = 0.01$ s, the opposite situation occurs.

Figure 14 shows the currents, the current references and the duty cycles of each converter. The blue and red lines of the upper sub-plot show the currents i_1 and i_2, whereas the yellow and purple dashed curves represent the current references. On the lower sub-plot, the blue curve corresponds to the duty cycle d_1 and the red one to d_2.

It is worth mentioning that the current references given by the allocator can always be attained by the current controller (the slopes of the currents match the slopes of the references) and the current limits are respected. Consistent with the cost function, the current distribution in steady state is such that the second converter is favored. Yet, the first converter is used during the transient, due to the priority given to tracking of the voltage reference.

With regard to the duty cycles, there is a visible difference between d_1 and d_2, due to the difference between the two inductor values. The duty cycle needs to vary more widely in the case of a larger inductor to regulate the current. The ripple on the current is also larger.

Figure 15 shows the first 20 ms of the upper sub-plot of Figure 14. This figure highlights the fact that the controller takes advantage of the heterogeneity of the converters. The allocator uses the first converter which is faster to more rapidly reach the voltage reference. Note the one-step delay between the reference and the measured value.

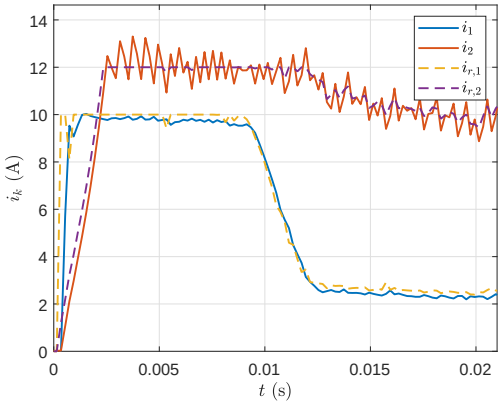

Figure 15: Currents i_k with their references during the first transient.

8.3.2. Experiment 2

Figure 16 shows the voltage, total current and currents responses for experiment 2. The blue line of the upper sub-plot shows the voltage response whereas the orange dashed line corresponds to its

reference. On the lower sub-plot, the blue line shows the total current and the orange and yellow lines are respectively the responses of i_1 and i_2.

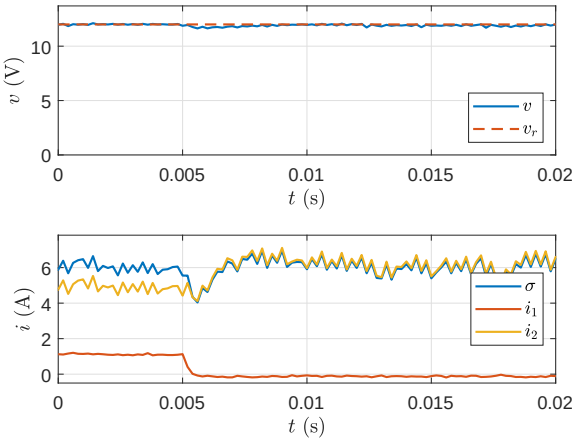

Figure 16: Voltage, currents and total current when switching off converter 1.

Observe that i_1 is driven to zero at $t = 0.005$ s. As a result, converter 1 can be taken out of service with minimal disturbance to the system. The current i_2 increases automatically to satisfy the power demand from the load. Aside from the benefit of control allocation in terms of optimized operation, the method also makes it possible to engage and disengage converters through trivial adjustments of the parameters of the algorithm.

9. Conclusions

An optimal control allocation strategy was proposed for the parallel interconnection of heterogeneous buck converters. In this manner, the regulation of the load voltage and the optimal distribution of the load current is achieved by separate components of the control algorithm. Converter dynamics and limits are taken into account. Dead-beat controllers are used for the current loops, which makes it possible to include the duty cycle constraints in the control allocator. The allocator computes current references via an active set quadratic optimization method. These references allow tracking of the total current reference while ensuring the feasibility of the commands and the optimization of efficiency as a secondary objective. The voltage controller is designed to regulate the voltage to its reference value, while taking into account the fact that load is unknown but lies within a known interval.

Experimental results validate the controller design and highlights the benefits of the proposed method, resulting in tight voltage control despite load variations and efficiency optimization in steady state. The second experiment shows that this type of controller can be used with minimal modifications to engage or disengage converters while supplying the load continuously. The latter is an interesting property for microgrids, related to the well known plug&play behaviour.

A possible topic of further research is the integration of other types of converters (such as boost converters) in the parallel interconnection. Non-linearities would be induced in the model and make the problem challenging. Furthermore, for the other control methods, recent results focus on distributed architecture (see [2, 37] concerning the droop-control method and [10] for current sharing). The extension of the control strategy of this paper to a distributed architecture is an appealing perspective.

Appendix A. Choice of the convex hull

To build the convex hull, polytopes that include each element of $A_e(R)$ and $B_e(R)$ for every $R \in \mathbb{L} = \left[R^-, R^+\right]$ are designed. Consider both elements

$$a_{11}{:}R \mapsto e^{-\frac{T_s}{RC}}, b_1 : R \mapsto R - \frac{R^2C}{T_s}\left(1 - e^{-\frac{T_s}{RC}}\right)$$
$$\text{and } a_{12} : R \mapsto R\left(\frac{RC}{T_s} - e^{-\frac{T_s}{RC}}\left(1 + \frac{RC}{T_s}\right)\right).$$

One needs to verify that the elements are monotonous functions of R. a_{11} clearly is, but some analysis is required for a_{12} and b_1. Differentiating the expressions

$$\frac{\mathrm{d}a_{12}}{\mathrm{d}R} = \frac{2RC}{T_s}\left(1 - e^{-\frac{T_s}{RC}}\right) - e^{-\frac{T_s}{RC}}\left(2 + \frac{T_s}{RC}\right)$$
$$\text{and} \quad \frac{\mathrm{d}b_1}{\mathrm{d}R} = 1 + e^{-\frac{T_s}{RC}} + \frac{2RC}{T_s}\left(e^{-\frac{T_s}{RC}} - 1\right).$$

In practice, $u := T_s/(RC)$ is close to 0. Then, the Taylor series expansion of previous expressions with respect to u gives

$$\frac{\mathrm{d}a_{12}}{\mathrm{d}R} = \frac{u^2}{3} + \mathrm{o}\left(u^2\right) \text{ and } \frac{\mathrm{d}b_1}{\mathrm{d}R} = \frac{u^2}{6} + \mathrm{o}\left(u^2\right)$$

As a result, a_{11}, a_{12} and b_1 are monotonous functions of u if T_s is sufficiently small [6]. Hence polytopes with only three vertices are sufficient to encapsulate those elements. The following principle of polytopes construction is shown on Figure A.17 for a_{11}. Two of the three vertices correspond to

6. Note that, for the experimental setup, u is such that, for all values of $R \in \mathbb{L}$, $\mathrm{d}a_{12}/\mathrm{d}R$ and $\mathrm{d}b_1/\mathrm{d}R$ are greater than 0.

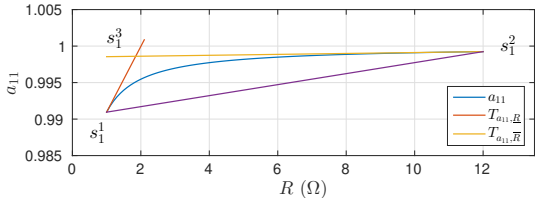

Figure A.17: Polytope construction for a_{11}

the value of $a_{11}(R)$, $a_{12}(R)$ and $b_1(R)$ for the bounds of $\mathbb{L}$, namely R^- and R^+

$$\begin{aligned} s_1^0 &\coloneqq a_{11}(R^-) \quad , \quad s_1^1 \coloneqq a_{11}(R^+), \\ s_2^0 &\coloneqq a_{12}(R^-) \quad , \quad s_2^1 \coloneqq a_{12}(R^+), \\ s_3^0 &\coloneqq b_1(R^-) \quad \text{and} \quad s_3^1 \coloneqq b_1(R^+). \end{aligned}$$

To find the third vertex, take the value of R for which the tangents of a_{11} and a_{12} in R^- and in R^+ intersect. The tangent of a function $f : x \mapsto f(x)$ at point x^* is

$$T_{f,x^*} : x \mapsto f(x^*) + \frac{\mathrm{d}f}{\mathrm{d}x}(x^*)\,(x - x^*)\,.$$

The solutions $\hat{R}_1$, $\hat{R}_2$ and $\hat{R}_3$ of the following relationships

$$\begin{aligned} T_{a_{11},R^-}(\hat{R}_1) &= T_{a_{11},R^+}(\hat{R}_1), \\ T_{a_{12},R^-}(\hat{R}_2) &= T_{a_{12},R^+}(\hat{R}_2), \\ T_{b_1,R^-}(\hat{R}_3) &= T_{b_1,R^+}(\hat{R}_3), \end{aligned}$$

lead to the expression of the third vertex

$$s_1^2 \coloneqq T_{a_{11},R^-}(\hat{R}_1),\ s_2^2 \coloneqq T_{a_{12},R^-}(\hat{R}_2),\ s_3^2 = T_{b_1,R^-}(\hat{R}_3).$$

As a result, every combination of matrix $A(R)$ and $B(R)$ with the vertices leads to the following twenty-seven pairs of matrices

$$[A_i, B_i] \coloneqq \left[\begin{bmatrix} s_1^j & s_2^l & 0 \\ 0 & 0 & 0 \\ -1 & 0 & 1 \end{bmatrix}, \begin{bmatrix} s_3^n \\ 1 \\ 0 \end{bmatrix} \right]$$

where $i = 3\,(3j + l) + n$ with $(j, l, n) \in \{1, 2, 3\}^3$. The convex hull $\mathcal{H}$ becomes

$$\mathcal{H} = \mathrm{co}\left\{ [A_i, B_i]_{i \in \{1,\dots,27\}} \right\}.$$

Appendix B. Proof of Proposition 1

Knowing that the fixed point satisfies $x[k+1] = x[k]$, (14) and (15) imply that

$$v = v_r,\ \sigma = \frac{v_r}{R} \text{ and } \xi = \frac{1 - k_\sigma}{R k_\xi} v_r.$$

If there exists a positive definite matrix $W = W^\intercal \in \mathbb{R}^{3\times3}$ and $Y \in \mathbb{R}^{1\times3}$ such that (17) holds for all $i \in \{1, \dots, n_v\}$, then by Schur complement and a pre/post-multiplication (see [38]), with $P = W^{-1}$ and $K = W^{-1}Y$, one finds that

$$(A_e(R) + B_e(R)K)^\intercal P (A_e(R) + B_e(R)K) - P \prec 0$$

holds. From [39], the corresponding system (14) is then exponentially stable.

References

[1] J. M. Guerrero, J. C. Vasquez, J. Matas, L. G. De Vicuña, and M. Castilla, "Hierarchical control of droop-controlled ac and dc microgrids a general approach toward standardization," *IEEE Transactions on industrial electronics*, vol. 58, no. 1, pp. 158–172, 2010.

[2] M. Baranwal, A. Askarian, S. Salapaka, and M. Salapaka, "A distributed architecture for robust and optimal control of dc microgrids," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 4, pp. 3082–3092, 2018.

[3] H. Hua, Y. Qin, C. Hao, and J. Cao, "Stochastic optimal control for energy internet: A bottom-up energy management approach," *IEEE Transactions on Industrial Informatics*, vol. 15, no. 3, pp. 1788–1797, 2018.

[4] V. J. Thottuvelil and G. C. Verghese, "Analysis and control design of paralleled dc/dc converters with current sharing," in *Proceedings of APEC 97 - Applied Power Electronics Conference*, vol. 2, Feb. 1997, pp. 638–646 vol.2.

[5] Y. Huang and C. K. Tse, "Circuit theoretic classification of parallel connected dc /dc converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 5, pp. 1099–1108, May 2007.

[6] A. Cid-Pastor, R. Giral, J. Calvente, V. I. Utkin, and L. Martinez-Salamero, "Interleaved converters based on sliding-mode control in a ring configuration," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 10, pp. 2566–2577, Oct. 2011.

[7] R. Delpoux, J.-F. Trégouët, J.-Y. Gauthier, and C. Lacombe, "New framework for optimal current sharing of nonidentical parallel buck converters," *IEEE Transactions on Control Systems Technology*, vol. 27, no. 3, pp. 1237–1243, 2018.

[8] S. K. Mazumder, M. Tahir, and K. Acharya, "Master–slave current-sharing control of a parallel dc–dc converter system over an rf communication interface," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, pp. 59–66, 2008.

[9] S. Moayedi and A. Davoudi, "Distributed cooperative load sharing in parallel dc-dc converters," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Mar. 2014, pp. 2907–2912.

[10] M. S. Sadabadi, "A distributed control strategy for parallel dc-dc converters," *IEEE Control Systems Letters*, 2020.

[11] H. Iu and C. Tse, "Bifurcation in parallel-connected buck converters under a democratic current sharing scheme," in *ISIE 2001. 2001 IEEE International Symposium on Industrial Electronics Proceedings (Cat. No. 01TH8570)*, vol. 3. IEEE, 2001, pp. 2118–2123.

[12] J.-F. Trégouët and R. Delpoux, "New framework for parallel interconnection of buck converters: Application to optimal current-sharing with constraints and unknown load," *Control Engineering Practice*, vol. 87, pp. 59–75, 2019.

[13] ——, "Parallel interconnection of buck converters revisited," *IFAC-PapersOnLine*, vol. 50, no. 1, pp. 15 792–15 797, 2017, 20th IFAC World Congress.
[14] J. Kreiss, J. Trégouët, D. Eberard, R. Delpoux, J. Gauthier, and X. Lin-Shi, "Hamiltonian point of view on parallel interconnection of buck converters," *IEEE Transactions on Control Systems Technology*, pp. 1–10, 2020.
[15] T. A. Johansen and T. I. Fossen, "Control allocation-a survey," *Automatica*, vol. 49, no. 5, pp. 1087–1103, 2013.
[16] M. W. Oppenheimer, D. B. Doman, and M. A. Bolender, "Control allocation," *The control handbook, control system applications*, 2010.
[17] A. Bouarfa, M. Bodson, and M. Fadel, "An optimization formulation of converter control and its general solution for the four-leg two-level inverter," *IEEE Transactions on Control Systems Technology*, vol. 26, no. 5, pp. 1901–1908, 2017.
[18] T. A. Johansen, T. I. Fossen, and S. P. Berge, "Constrained nonlinear control allocation with singularity avoidance using sequential quadratic programming," *IEEE Transactions on Control Systems Technology*, vol. 12, no. 1, pp. 211–216, Jan. 2004.
[19] A. Serrani, "Output regulation for over-actuated linear systems via inverse model allocation," in *2012 IEEE 51st IEEE Conference on Decision and Control (CDC)*, Dec. 2012, pp. 4871–4876.
[20] S. Galeani and S. Pettinari, "On dynamic input allocation for fat plants subject to multi-sinusoidal exogenous inputs," in *53rd IEEE Conference on Decision and Control*, Dec. 2014, pp. 2396–2403.
[21] M. Bodson, "Evaluation of optimization methods for control allocation," *Journal of Guidance, Control, and Dynamics*, vol. 25, no. 4, pp. 703–711, Jul. 2002.
[22] Y. Luo, A. Serrani, S. Yurkovich, D. B. Doman, and M. W. Oppenheimer, "Model predictive dynamic control allocation with actuator dynamics," in *Proceedings of the 2004 American control conference*, vol. 2. IEEE, 2004, pp. 1695–1700.
[23] L. Zaccarian, "Dynamic allocation for input redundant control systems," *Automatica*, vol. 45, no. 6, pp. 1431–1438, 2009.
[24] J. Tjønnås and T. A. Johansen, "Adaptive control allocation," *Automatica*, vol. 44, no. 11, pp. 2754–2765, 2008.
[25] J. Kreiss, J.-F. Trégouët, R. Delpoux, J.-Y. Gauthier, and X. Lin-Shi, "A new framework for dealing with input constraints on parallel interconnection of buck converters," in *2019 18th European Control Conference (ECC)*. IEEE, 2019, pp. 429–434.
[26] M. Hanger, T. A. Johansen, G. K. Mykland, and A. Skullestad, "Dynamic model predictive control allocation using cvxgen," in *2011 9th IEEE International Conference on Control and Automation (ICCA)*, Dec. 2011, pp. 417–422.
[27] O. Harkegard, "Backstepping and control allocation with applications to flight control," Ph.D. dissertation, Universitetet i Linkoping, 2003.
[28] ——, "Dynamic control allocation using constrained quadratic programming," *Journal of Guidance, Control, and Dynamics*, vol. 27, no. 6, pp. 1028–1034, 2004.
[29] M. Bodson and S. A. Frost, "Load balancing in control allocation," *Journal of Guidance, Control, and Dynamics*, vol. 34, no. 2, pp. 380–387, Nov. 2011.
[30] O. Harkegard, "Efficient active set algorithms for solving constrained least squares problems in aircraft control allocation," in *Proceedings of the 41st IEEE Conference on Decision and Control, 2002.*, vol. 2, Dec. 2002, pp. 1295–1300 vol.2.
[31] J. Nocedal and S. J. Wright, *Numerical Optimization*, 2nd ed., ser. 1431-8598. Springer-Verlag New York, 2006, vol. XXII, 664.
[32] O. Harkegard, *Quadratic programming control allocation toolbox for Matlab*, Std., 2004. [Online]. Available: http://research.harkegard.se/qcat/
[33] J. M. Gomes da Silva, D. Limon, T. Alamo, and E. F. Camacho, "Dynamic output feedback for discrete-time systems under amplitude and rate actuator constraints," *IEEE Transactions on Automatic Control*, vol. 53, no. 10, pp. 2367–2372, Nov. 2008.
[34] S. Galeani, S. Tarbouriech, M. Turner, and L. Zaccarian, "A tutorial on modern anti-windup design," *European Journal of Control*, vol. 15, no. 3, pp. 418–440, 2009.
[35] J. M. Gomes da Silva and S. Tarbouriech, "Anti-windup design with guaranteed regions of stability for discrete-time linear systems," *Systems & Control Letters*, vol. 55, no. 3, pp. 184–192, 2006.
[36] J. G. Da Silva and S. Tarbouriech, "Antiwindup design with guaranteed regions of stability: an lmi-based approach," *IEEE Transactions on Automatic Control*, vol. 50, no. 1, pp. 106–111, 2005.
[37] H. Wang, M. Han, R. Han, J. M. Guerrero, and J. C. Vasquez, "A decentralized current-sharing controller endows fast transient response to parallel dc–dc converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4362–4372, 2017.
[38] S. Boyd, L. El Ghaoui, E. Feron, and V. Balakrishnan, *Linear Matrix Inequalities in System and Control Theory*. Society for Industrial and Applied Mathematics (SIAM), 1994.
[39] D. Peaucelle, D. Arzelier, O. Bachelier, and J. M. Bernussou, "A new robust d-stability condition for real convex polytopic uncertainty," *Systems & Control Letters*, vol. 40, no. 1, pp. 21–30, 2000.