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A Fully-Digital 0.1-to-27 Mb/s ULV 450 MHz Transmitter with sub-100 μ W Power Consumption for Body-Coupled Communication in 28 nm FD-SOI CMOS

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Abstract— A 0.5 V fully-digital 450 MHz transmitter for surface wave capacitive body-coupled communications is realized in 28 nm FD-SOI CMOS and consumes 17 to 76 μ W for data rates from 0.1 to 27 Mb/s with up to 14 % system efficiency. The heavily duty-cycled transmitter uses a 90 MHz free-running oscillator and edge combiners to generate OOK Gaussian-shaped pulses through a switched-capacitor PA. Body-biasing allows frequency tuning and adaptive efficiency optimization as a function of data rate.

Keywords— Body Area Network, Ultra-Low Power Transmitter, Body-Coupled Communication, 28 nm FD-SOI CMOS

I. INTRODUCTION

Enabling human-centric computing requires an energy efficient network interconnecting multiple sensors and actuators on the human body featuring a diverse and broad range of data rates (Fig. 1). Common RF-based solutions such as ultra-wideband (UWB) or Bluetooth Low Energy (BLE) suffer from data rate and/or energy efficiency limitations. BLE offers a maximum data rate of only 1 to 2 Mb/s [1], [2]. UWB in contrast brings flexibility by enabling both low data rate (hundreds of kb/s) and high data rate (tens of Mb/s) [3]. However, the largest challenge is that free-space RF channels undergo high propagation-loss due to body shadowing effects, requiring increased output power and hence reduced energy efficiency. A promising alternative is Body-Coupled Communication (BCC), where the human body is used as the medium of propagation. Magnetic BCC (m-BCC) [4] offers a low-loss channel but is unstable under

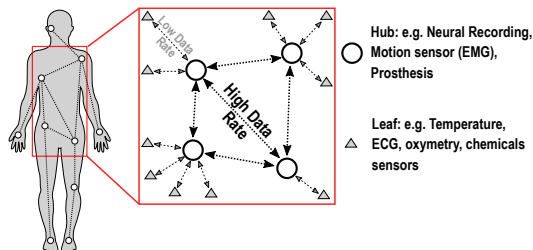


Fig. 1. Human-Centric Computing network topology

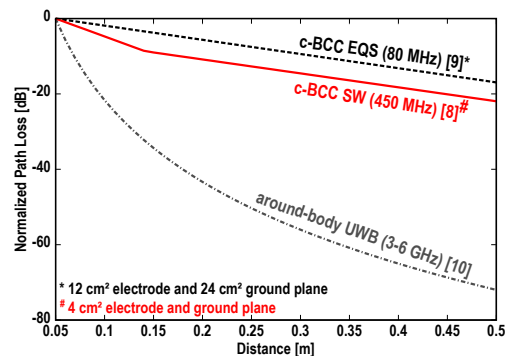


Fig. 2. Channel model of c-BCC SW [8] compared to c-BCC EQS [9] and around-body UWB [10]

motion due to the coil resonance requirements and is not easily wearable because of the form factor of the coils. Capacitive BCC (c-BCC) [5], [6], [7] allows compact solutions for full-coverage on-body communication. However, the state of the art only reports c-BCC operating in the electro quasi-static (EQS) mode (i.e. $f_c < 150$ MHz), which limits the available bandwidth and hence the achievable data rate. Furthermore, it is prone to narrow-band FM-broadcast interference [5], and the channel is highly sensitive to posture, electrode attachment and environment variations.

II. PROPOSED TRANSMITTER

A. Surface Wave Capacitive Body-Coupled Communication

This work proposes a c-BCC transmitter (TX) in the 450 MHz band, where surface wave (SW) propagation is the dominant mechanism. In comparison with EQS, the SW propagates along the surface of the human body and is, by nature, less sensitive to the return path, and hence less sensitive to environment variations, while the higher carrier frequency allows for smaller electrodes [8]. The higher path loss, as compared to EQS [9], is compensated for by the large available bandwidth (> 150 MHz) and the robust channel characteristics (Fig. 2). The path loss models are normalized at 5 cm as the insertion loss depends on the antenna/electrode matching. Exploiting these properties, we have realized a

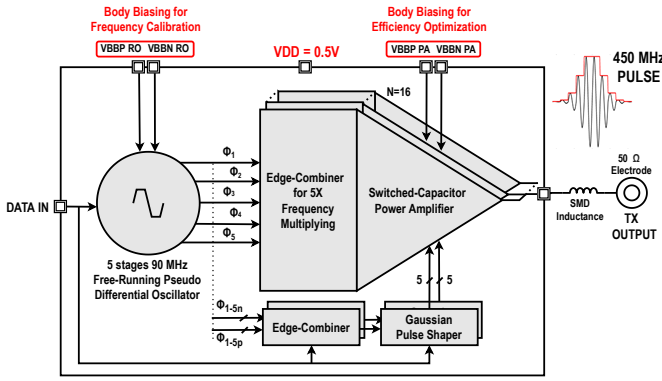


Fig. 3. Proposed architecture of the c-BCC SW TX

sub-100 μW OOK transmitter for pulse-based communication at 450 MHz using wide bandwidth (150 MHz) in a 28 nm FD-SOI CMOS technology. To the authors knowledge, this is the first published c-BCC link employing SW propagation.

B. Transmitter Design

As the required output power is significantly lower than 0 dBm, the PA efficiency is no longer the most crucial part, and frequency synthesis dominates power consumption. This is addressed through an all-digital solution operating at 0.5 V using an unlocked frequency reference, supporting flexible data rates. The pulse-based modulation allows for aggressive duty-cycling reducing the power at low data-rate while taking advantage of the wide available bandwidth.

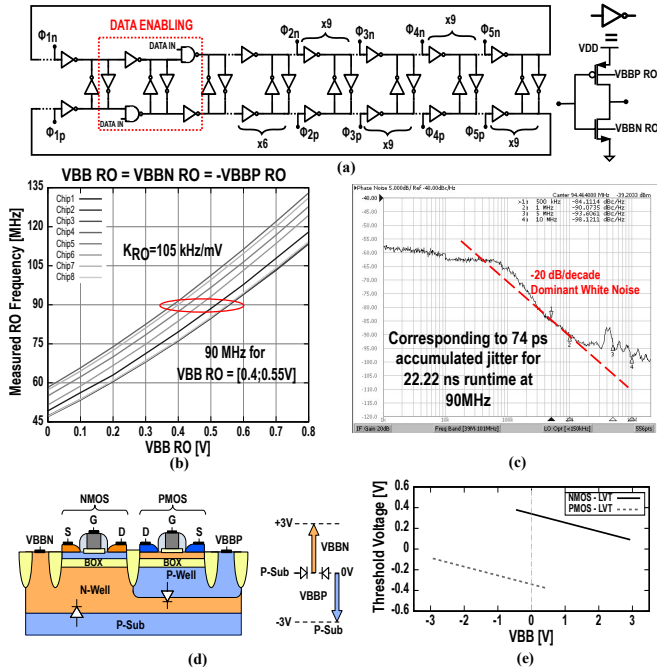


Fig. 4. (a) PD-RO schematic. (b) Measured PD-RO Frequency vs body-bias voltage for 8 devices. (c) PD-RO phase noise measurement (the plateau from 1 kHz to 100 kHz is due to the internal PLL of the measurement equipment locking). (d) FD-SOI cross section and body-bias range. (e) LVT NMOS/PMOS threshold voltage versus body-bias voltage

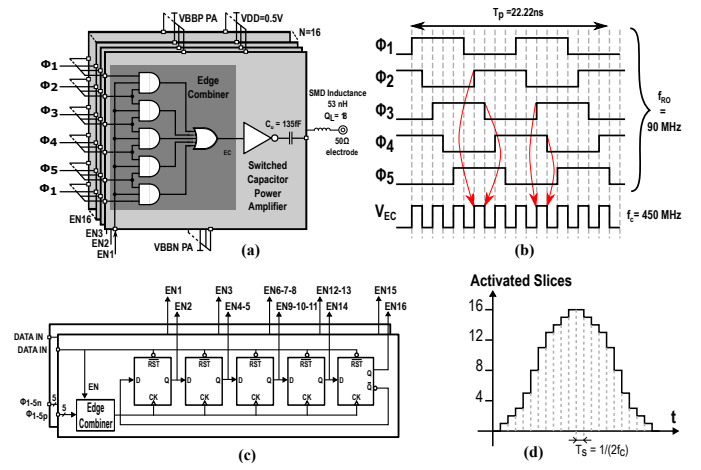


Fig. 5. (a) Schematic of the EC-SCPA. (b) Timing diagram of the EC. (c) Schematic of the digital pulse shaper. (d) Gaussian pulse envelop generated by the pulse shaper

The TX circuit (Fig. 3) is composed of a free-running pseudo-differential ring oscillator (PD-RO) at 90 MHz (Fig. 4.a) and a switched-capacitor power amplifier (SCPA) with embedded edge-combiners (EC). The low-frequency of the PD-RO reduces the power consumption of the frequency reference. The overall TX is data-enabled (OOK modulation), which means it only runs during the pulse duration. Short pulses combined with non-coherent OOK modulation allow for the use of an unlocked frequency reference and enable instant startup time and aggressive duty-cycling. For a short runtime, white noise is the dominant noise source in free-running oscillators, while jitter increases as the square root of the run-time. The PD-RO runs for a 22.22 ns duration (two periods at 90 MHz), and achieves a measured accumulated jitter of 74 ps (Fig. 4.c). It is composed of two single-ended ring oscillator loops mounted in a pseudo-differential topology using inverter-based latch locking between each stage. The positive feedback enables fast current transitions with sharp edges as required for the edge combination [11]. A NAND gate inside each loop duty-cycles the oscillator according to the input data. The oscillator frequency fine-tuning is obtained via body-biasing through one-time calibration (around $VBB_{RO} = 0.5 \text{ V}$) (Fig. 4.b) and allows to compensate PVT variations.

The edge-combiners are performing frequency multiplication by 5 to reach the 450 MHz central emission frequency. In each SCPA slice, an edge combiner multiplies the PD-RO frequency by 5 using simple digital logic (Fig. 5.a.b). In practice, the conceptual ANDs and OR gates shown in Fig. 5.a are implemented in NAND logic. The edge combiner drives an output inverter in series with a 135 fF capacitance. For spectral efficiency, a near-Gaussian pulse shaper activates each slice independently to control the instantaneous output voltage. A dual 5-bit Johnson ring counter driven by complementary clocks provides the enable (EN) signals at a sampling frequency equivalent to twice the carrier frequency (f_c) (Fig. 5.c.d). The complementary 450

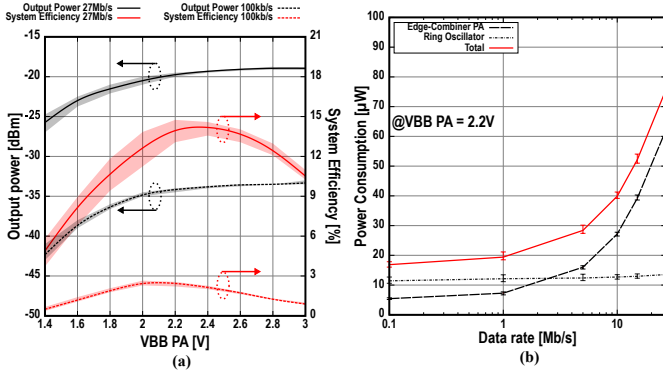


Fig. 6. (a) Output power and System Efficiency versus body-biasing voltage for different data rate (Lines represent the average measured values and the shaded curves represent the boundaries of minimum of maximum measured values on several devices). (b) Power Breakdown of the TX at $VBB_{PA} = \pm 2.2$ V versus data rate (error bars represent the boundaries of minimum of maximum measured values).

MHz clocks are generated by two identical edge combiners from respectively the positive and negative phases of the 90 MHz PD-RO (ϕ_{1-5n}, ϕ_{1-5p}). The increased pulse envelope timing resolution improves the spectral efficiency limiting the spread beyond the targeted band. The energy efficiency of an SCPA strongly depends upon the ON-resistance (R_{ON}) of the switches in the output inverters. The forward body-biasing (FBB) knob, specific to FD-SOI technologies, is used to lower the threshold voltage of the transistors (Fig. 4.d.e), reducing R_{ON} at the low 0.5 V supply voltage, while limiting their size. The pulse shaper and edge combiners are designed using standard cells with a poly-biasing (i.e. gate length extension) of 16 nm. The oscillator's and SCPA's output inverters are custom designed with a gate length increased to $L_{min} + 16$ nm as well. This increased gate length limits the impact of leakage and offers manufacturing robustness when operating at 0.5 V. In a fully practical implementation a body-bias generator could be integrated on-chip to generate the body-biasing voltages.

III. MEASUREMENTS RESULTS

The TX chip has been implemented in a 28 nm FD-SOI CMOS technology and occupies a 0.0418 mm² area (Fig 9.b) For a measured -19.7 dBm output power at the maximum data rate of 27 Mb/s, the SCPA reaches an optimal operating point at $VBB_{PA} = 2.2$ V (Fig. 6.a). The body-biasing voltage can be adapted to reach the best system efficiency for a given data rate or to compensate PVT variations, through one-time calibration. Fig. 7 shows the OOK modulated output signal in the time and frequency domains for the low and high data rates (100 kb/s and 27 Mb/s) and highlights the large signal bandwidth and the effect of the pulse shaping.

A. TX Electrical Performances Measurements

As summarized in Fig. 8, the TX consumes $76 \mu\text{W}$ at 27 Mb/s, which corresponds to 2.8 pJ/b for an overall 14 % system efficiency at -19.7 dBm output power. For the lowest

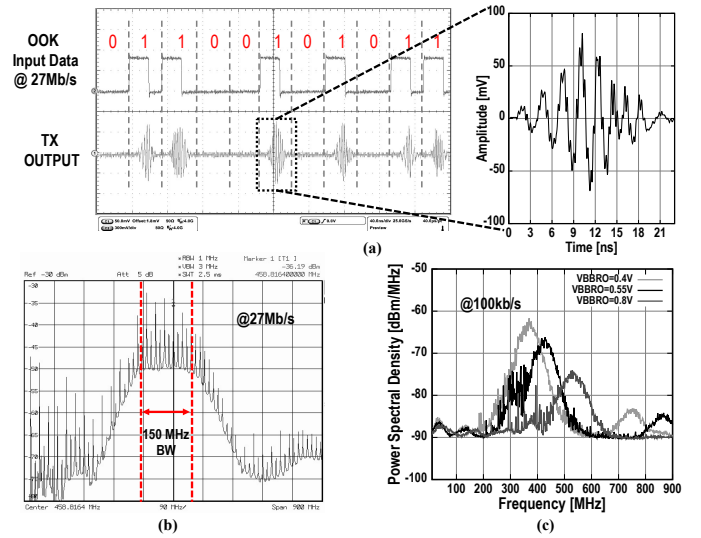
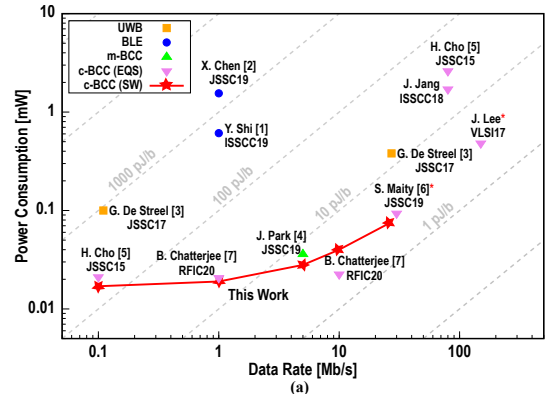


Fig. 7. (a) Timing response of the TX at 27 Mb/s. (b) Spectrum response at 27Mb/s. (c) Frequency response for different body bias voltage on the ring oscillator at 100 kb/s



| | This Work | G. De Streef [3] | J. Park [4] | H. Cho [5] | S. Maity [6] | B. Chatterjee [7] |
|-------------------------|------------|------------------|-------------|-------------|--------------|-------------------|
| Radio Technology | C-BCC (SW) | UWB | M-BCC | C-BCC (EQS) | C-BCC (EQS) | C-BCC (EQS) |
| Process Technology | 28nm FDSOI | 28nm FDSOI | 65nm | 65nm | 65nm | 65nm |
| Carrier Frequency [MHz] | 350 - 550 | 3500-4500 | 40 | 13.56 | 20-60 | 140-180 |
| Supply Voltage [V] | 0.5 | 0.55 | 0.6 | 1.2 | 1 | 1 |
| Data rate [Mb/s] | 0.1 | 27 | 5 | 0.1 | 80 | 30 |
| Modulation | OOK | BPM/BPSK | OOK | OOK | BPSK | NRZ |
| Power Consumption [μW] | 17 | 76 | 100 | 380 | 37 | 21 |
| Energy per bit [pJ/b] | 170 | 2.8 | 950 | 14 | 7.2 | 210 |
| Output Power [dBm] | -33.8 | -19.7 | -20 | -24.8 | N.R. | N.R. |
| System Efficiency [%] | 2.44 | 14 | 2.6 | 17.8 | N.R. | N.R. |
| Area [mm ²] | 0.0418 | 0.095 | 0.0204 | 0.1672 | 0.02 | 0.117 |

* Not including frequency synthesis power consumption
* TX only

Fig. 8. (a) Power consumption versus data rate compared with TX state of the art. (b) Table of comparison with the state of the art

data rate (100 kb/s), the TX consumes $17 \mu\text{W}$ with 2.44 % system efficiency. Here, the PD-RO is the dominating power consumer because of its static power dissipation, translating into an energy efficiency of 170 pJ/b for a -33.8 dBm output power (Fig. 6.b). The power consumption of the SW transmitter is at par or better than the state-of-the-art over the

full range of data rates (Fig. 8.a). When compared to UWB TX, this work shows a 5X improvement in energy efficiency at both high and low data-rates for similar output power [3]. With respect to a c-BCC (EQS) TX [5], this SW solution improves the energy efficiency by 11X and 1.2X, for the high and low data-rates, respectively over the state-of-the-art. In comparison with [7], this work offers a wider range of operating data rate with equivalent energy efficiency order.

B. On-body Demonstration

Finally, as a proof of concept, a demonstration of the signal propagation on the human body is shown (Fig. 9). A 4 cm² electrode (similar to the one used in [8]) is wired to the output of the battery-powered TX and attached to the body. As a receiver, a TRF37D73EVM amplifier from Texas Instruments is attached to an other electrode with the same dimensions. The signal is then observed on a DSO91204A oscilloscope from Keysight, after which a digital band-pass filter is applied. The pulses from the transmitted signal are retrieved and observed on the oscilloscope (Fig. 9.d.e). The signal is observable for a distance up to 50 cm on the full arm (scenario 1) and also for a pectoral to shoulder blade distance (around 30 cm, scenario 2) at the maximum data rate. Furthermore, it is notable that when the electrodes are not attached to the body (air propagation) the signal is merely observable over a few centimeters. This demonstrates that the mechanism of propagation is truly body-coupled and not because of the electrodes acting as antennas with over the air propagation.

IV. CONCLUSION

A 0.5 V 28 nm FD-SOI CMOS ultra-low voltage transmitter with flexible data rate (100 kb/s to 27 Mb/s) and using capacitive body-coupled communication with surface wave propagation is presented. The highly duty-cycled transmitter with pulse-based communication uses a low frequency, body-biased controlled oscillator and a switched-mode power amplifier with embedded frequency multiplier, Gaussian pulse shaping and body-biased efficiency optimization. When compared to body-coupled transmitter state of the art, the proposed TX solution shows a better flexibility as addressing a wider operation data rate, while staying at par or better in terms of energy efficiency. Moreover, the surface wave body-coupled link has been successfully demonstrated on-body using off-the-shelf receiver.

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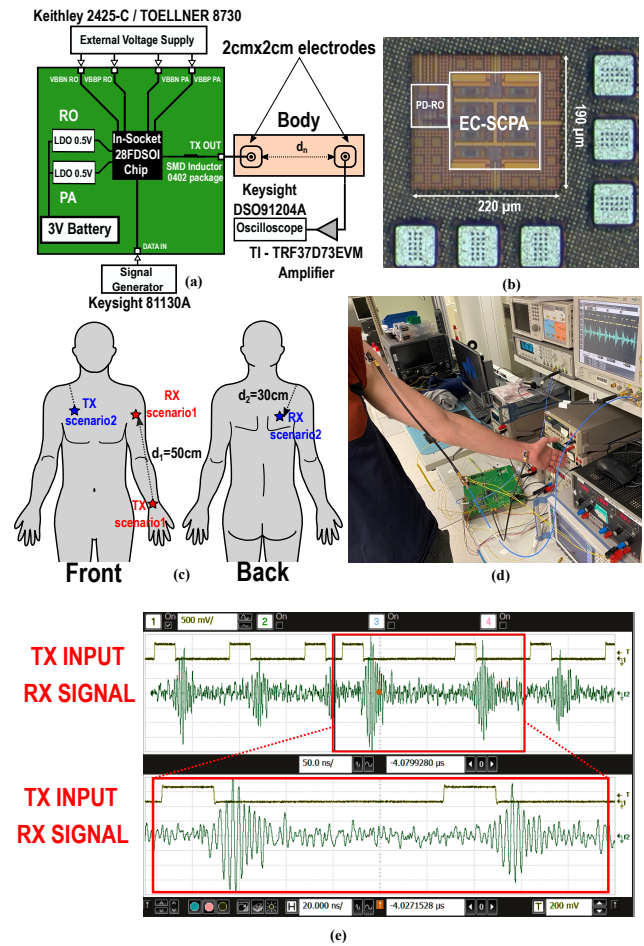


Fig. 9. (a) Set-up for on-body demonstration. (b) Die Photography. (c) Scenarios for on-body demonstration. (d) Picture of the body-coupled demonstration on the arm. (e) Observed signal at the output of the amplifier for torso to back

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