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Guillaume Tochou, Andreia Cathelin, Antoine Frappé, Andreas Kaiser, Jan Rabaey. Impact of forward body-biasing on ultra-low voltage switched-capacitor RF power amplifier in 28 nm FD-SOI. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69 (1), pp.50-54. 10.1109/tcsii.2021.3088996 . hal-03306891

**HAL Id: hal-03306891**

**<https://hal.science/hal-03306891>**

Submitted on 29 Jul 2021

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# Impact of Forward Body-Biasing on Ultra-Low Voltage Switched-Capacitor RF Power Amplifier in 28 nm FD-SOI

Guillaume Tochou, *Student Member, IEEE*, Andreia Cathelin, *Senior Member, IEEE*,  
Antoine Frappé, *Senior Member, IEEE*, Andreas Kaiser, *Senior Member, IEEE*,  
and Jan Rabaey, *Life Fellow, IEEE*

**Abstract**—The Switched-Capacitor Power Amplifier (SCPA) has become a key enabler for modern wireless communication because of its high efficiency, high linearity, and high integrability. This paper discusses the impact of the extended Forward Body-Biasing (FBB) feature in 28 nm FD-SOI technology on Ultra-Low Voltage (ULV) SCPA. A new model of the Drain Efficiency (DE) and System Efficiency (SE) including body-biasing and drivers power consumption is introduced and validated with *SpectreRF* simulations. FBB on the SCPA improves by up to 14 % and 67 % the SE and transistors area, respectively, compared to a nominally body-biased SCPA under 0.5 V supply voltage at 2.4 GHz, while improving linearity and enhancing PVT variations.

**Index Terms**—IoT, SCPA, ULV, Class-D PA, Low-Power, CMOS, RF, 28 nm FD-SOI

## I. INTRODUCTION

INTERNET of Things (IoT) is expected to connect trillions of devices in the coming years, with various kinds of applications in healthcare, urbanism, industry, agriculture, and so forth. However, it is necessary to make those massive networks of nodes sustainable on the environmental and socioeconomic aspects. In [1] four main challenges from the circuit and technology point of view are highlighted to be addressed to make the IoT sustainable:

- 1) Extremely low-power, battery-less sensors with energy harvesting.
- 2) Highly integrated SoC or SiP without external components.
- 3) Agile RF communications.
- 4) Optimized data management.

Manuscript received XXX X, XXXX; revised XXX XX, XXXX; accepted XX XX, XXXX. Date of publication XXX XX, XXXX; date of current version XX X, XXXX.

G. Tochou is with STMicroelectronics, Crolles France ; Univ. Lille, CNRS, Centrale Lille, Junia, Univ. Polytechnique Hauts-de-France, UMR 8520 - IEMN – Institut d’Electronique de Microélectronique et de Nanotechnologie, F-59000 Lille, and Berkeley Wireless Research Center, UC Berkeley, CA, USA (guillaume.tochou@st.com)

A. Cathelin is with STMicroelectronics, Crolles, France (andreia.cathelin@st.com)

A. Frappé and A. Kaiser are with Univ. Lille, CNRS, Centrale Lille, Junia, Univ. Polytechnique Hauts-de-France, UMR 8520 - IEMN – Institut d’Electronique de Microélectronique et de Nanotechnologie, F-59000 Lille (antoine.frappe, andreas.kaiser@junia.fr)

J. Rabaey is with Berkeley Wireless Research Center, UC Berkeley, CA, USA (jan\_rabaey@berkeley.edu)

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Digital Object Identifier XXXXXXXXX

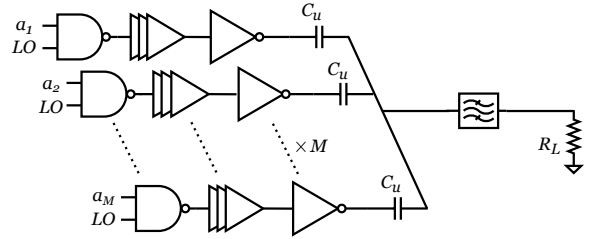


Fig. 1. SCPA Schematic

Reaching these goals will allow reducing battery replacement, end-of-life cycle processes, RF spectrum congestion, and electrical power consumption of the base stations and data centers. It is also shown in [1] that ultra-low voltage (ULV) design and FD-SOI technology can help to meet those goals. Within this scope, Switched-Capacitor Power Amplifiers (SCPA) [2] are an interesting lead as they allow high integrability, high power efficiency, and high configurability. This paper investigates the improvement of an ULV SCPA in 28 nm FD-SOI CMOS technology through optimal body-biasing strategy. Section II presents the principle of operation of an SCPA. Sections III and IV present the proposed model of Drain Efficiency (DE) and System Efficiency (SE), respectively, including body-biasing. Section V presents the simulation results validating the analytical models and discusses these results. Section VI presents the results on the impact on linearity. Finally, Section VII concludes this work.

## II. SWITCHED-CAPACITOR POWER AMPLIFIER

The SCPA is a Class-D PA that has been very popular recently as it allows to design high performances transmitter with high-order complex modulation, watt-level output power, beamforming, among others [3]. As well, it has also been demonstrated to be very well suited for ultra-low power communications [4]–[6].

The SCPA is composed of an array of  $M$  capacitances  $C_u$  and switches (Fig. 1). A switch slice is designed with a CMOS inverter driven by a buffer chain and enabled by a NAND gate. The phase and frequency information is carried through the local oscillator signal (LO). A given number of slices  $m$  of the array is enabled dynamically by a digital code-word  $a = \{a_1, a_2, \dots, a_M\}$  controlling the envelope amplitude of

the output signal. Hence, the ideal output power in continuous wave is given by [2] :

$$P_{out,id} = \frac{2}{\pi^2} \left( \frac{m}{M} \right)^2 \frac{V_{dd}^2}{R_L} \quad (1)$$

Where  $V_{dd}$  is the supply voltage and  $R_L$  is the load. For an ideal SCPA, the only source of loss comes from the dynamic power required to charge and discharge the capacitance array [2]. The Drain Efficiency (DE) is defined as the ratio of the output power to the power drawn from the supply by the switches. The switches are CMOS inverters where the PMOS is connecting the output to  $V_{dd}$ , while the NMOS is in OFF-state, for half a period, and the NMOS is connecting the output to the ground, while the PMOS is in OFF-state, during the other half of the period. The ideal peak DE is 100 % and the ideal DE at power back-off (PBO) (i.e.  $m < M$ ) is defined as [2] :

$$\eta_{id} = \frac{P_{out,id}}{P_{out,id} + \frac{m(M-m)}{M^2} CV_{dd}f_c} = \frac{4m^2}{4m^2 + \frac{\pi m(M-m)}{Q_L}} \quad (2)$$

$$Q_L = \frac{1}{2\pi \cdot f_c \cdot C \cdot R_L} \quad (3)$$

Where  $C$  is equal to the sum of the unit capacitances  $C_u$ ,  $f_c$  is the operating frequency, and  $Q_L$  is the loaded quality factor.

### III. DRAIN EFFICIENCY MODEL

The first source of losses in a SCPA is due to the ON-resistance  $r_{on}$  of the MOSFETs. The common technique to reduce loss is to increase their widths to reduce  $r_{on}$ . However, careful optimization of the MOSFETs' width is required as it linearly increases the parasitic capacitance  $C_p$  making the dynamic losses predominant [7] (Fig. 2). It has been shown [8], that the use of Forward Body-Biasing (FBB) lowers the ON-resistance of the MOSFETs and positions the FD-SOI technology as a great candidate for switched-capacitor circuits. Thus, we propose to introduce the FBB parameter in the DE model to study how its use can help to reduce the ON-resistance while limiting the increase of the parasitic capacitance. However, FBB reduces the transistors' threshold voltage which exponentially increases the leakage of the MOSFETs when they are in OFF-state. Hence, Drain Efficiency can be written as:

$$\eta = \frac{P_{out}}{P_{out} + P_{sc} + P_{diss} + P_{dyn} + P_{leak}} \quad (4)$$

Where  $P_{diss}$  is the dissipated power in  $r_{on}$ ,  $P_{dyn}$  is the dynamic power dissipated due to  $C_p$ , and  $P_{leak}$  is the static dissipated power due to the current leakage.  $P_{sc}$  corresponds to the dynamic power required to charge and discharge the capacitance array at PBO and is equal to [2]:

$$P_{sc} = f_c \cdot V_{dd}^2 \cdot \frac{m(M-m)}{M^2} \cdot C \quad (5)$$

The calculations of these three sources of losses, including the body-bias parameter, are detailed in the following subsections.

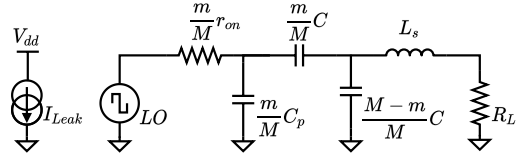


Fig. 2. Equivalent circuit model of the SCPA including ON-resistance, parasitic capacitance, and leakage

#### A. Losses due to ON-resistance

The ON-resistance lowers the output power as it acts as a voltage divider and dissipates power:

$$P_{out} = \frac{2}{R_L} \left( \frac{m}{M} \right)^2 \left( \frac{V_{dd}}{\pi} \frac{R_L}{R_L + r_{on}} \right)^2 \quad (6)$$

$$P_{diss} = \frac{2}{r_{on}} \left( \frac{m}{M} \right)^2 \left( \frac{V_{dd}}{\pi} \frac{r_{on}}{R_L + r_{on}} \right)^2 \quad (7)$$

Where the equivalent  $r_{on}$  model, with body-bias parameter is:

$$r_{on} = \frac{L}{W \cdot K \cdot [V_{dd} - (|V_{T0}| - \gamma|V_{bb}|)] \cdot M} \quad (8)$$

Where  $V_{T0}$ , the nominal threshold voltage,  $\gamma$ , the body factor, and  $K$  (typically equal to  $\mu_{eff}C_{ox}$ ) are all technology parameters.  $L$  and  $W$  are the length and the width of the transistors, respectively, and  $V_{bb}$  is the body-biasing voltage. Thus, to reduce the ON-resistance we can tune the switches' width and the body voltage. In the 28 nm FD-SOI technology, the body factor is  $\sim 85$  mV/V for the thin oxide LVT devices and the body voltage variation can range up to  $\pm 3$  V [9] (Fig. 3) allowing to reduce the threshold voltage and hence the  $r_{on}$ . As a rule of thumb, PMOS width to NMOS width ratio has to be sized such as  $r_{on,p} \approx r_{on,n}$  to minimize the loss [2].

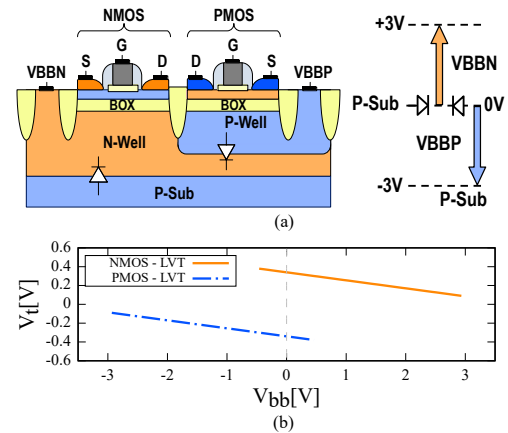


Fig. 3. (a) Cross-section and (b) Threshold voltage variations of LVT transistors in 28 nm FD-SOI [9]

#### B. Dynamic power dissipation in switches

Dynamic dissipated power in the switches is due to the power required to charge and discharge the parasitic capacitance  $C_p$  of the MOSFETs. The dynamic power consumption is expressed by:

$$P_{dyn} = \left( \frac{m}{M} \right) \cdot f_c \cdot C_p \cdot V_{dd}^2 \cdot k_{sc} \quad (9)$$

Where the factor  $k_{sc}$  represents the short-circuit current loss. Typically,  $k_{sc}$  is inferior to 1.1 (ideally equal to 1) for equal rise/fall transition times [10]. The total parasitic capacitance  $C_p$  is linearly proportional to the width of the switches and is equal to  $C_p = b \cdot W \cdot M$  where  $b$  is a technology parameter.

### C. Static power dissipation in switches

Static power dissipation is mainly due to the subthreshold leakage and Drain-Induced Barrier Lowering (DIBL) leakage when the transistors are in OFF-state [11]. The leakage power dissipation is expressed as:

$$P_{leak} = V_{dd} \cdot I_{leak} \quad (10)$$

$$I_{leak} = 2 \cdot n \cdot K \frac{W}{L} U_{th}^2 \exp\left(\frac{-V_{T0} + \gamma V_{bb} + \lambda V_{dd}}{n U_{th}}\right) \cdot M \quad (11)$$

Where  $n$  is the subthreshold slope factor,  $\lambda$  is the DIBL factor and are technology parameter.  $U_{th}$  is the thermal voltage ( $kT/q$ ).

## IV. SYSTEM EFFICIENCY MODEL

A more relevant metric to evaluate the efficiency of a SCPA is the System Efficiency (SE), which takes into account all the power drawn from the supply by *all* the external circuitry required to operate the PA: the digital logic, clock tree distribution and driving buffers [3]. However, we define here the SE as the metric solely taking into account the dissipated power in drivers in addition to the power dissipated in the switches. The buffer chains required to drive the large input capacitance of the switches is the most consuming part in the external circuitry [2]. Furthermore, only the drivers power dissipation is directly dependent on the switch sizing.

$$SE = \frac{P_{out}}{P_{out} + P_{sc} + P_{diss} + P_{dyn} + P_{leak} + P_{dr}} \quad (12)$$

$$P_{dr} = \left(\frac{m}{M}\right) \cdot f_c \cdot C_{dr} \cdot V_{dd}^2 \cdot k_{sc} + I_{leak,dr} \cdot V_{dd} \quad (13)$$

To calculate the power consumption of the drivers we need to estimate the equivalent drivers' capacitance  $C_{dr}$  and their total leakage current. By using the analysis in [12] we can easily calculate the total capacitance in the tapered buffers:

$$C_{dr} = (F^N - 1) \cdot \frac{F C_x + C_y}{F - 1} \cdot M \quad (14)$$

Where  $F$  is the tapering factor of the buffer chain,  $C_x$  is the input capacitance of a minimum size inverter,  $C_y$  is the output capacitance of a minimum size inverter.  $N$  is the number of inverter in the driver chain and is defined as  $N = \ln(C_{sw}/C_x)/\ln(F)$ . Where  $C_{sw}$  is the input capacitance of a switch. By analogy, we can also calculate the total leakage current in the driver chains.

$$I_{leak,dr} = I_0 \cdot \frac{F^N - 1}{F - 1} \quad (15)$$

Where  $I_0$  is the reference current leakage in a minimum size inverter which can be calculated using (11).

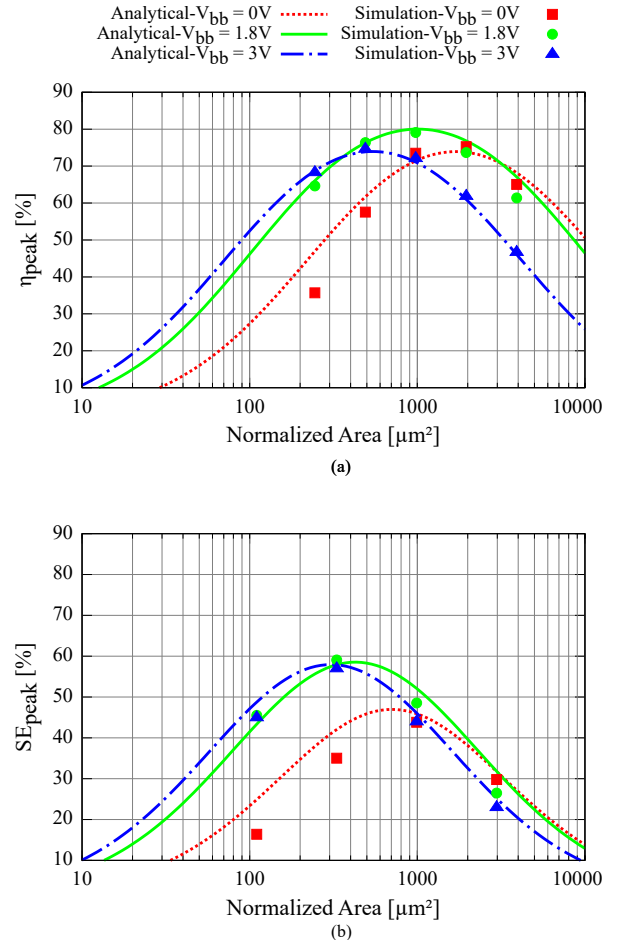


Fig. 4. (a) Peak DE and (b) peak SE versus normalized switch area: simulated results compared to the analytical model for different body-biasing voltage

## V. SIMULATION VALIDATION AND DISCUSSION

To compare and validate the DE and SE analytical models, simulations are performed with *SpectreRF* in the 28 nm FD-SOI technology from *STMicroelectronics*. The simulations and analytical models are compared for a 2.4 GHz frequency, 0.5 V supply voltage. To limit leakage impact, the lengths of the transistors are slightly increased by 15 % through poly-biasing of  $L_{min} + 4 \text{ nm}$  [13]. For the DE simulations, the drivers are considered ideal, consuming zero power and with the same sizing as the switches (i.e. tapering factor of 1). The NMOS transistors are body-biased with voltages spanning from 0 to 3 V, and the PMOS transistors from 0 down to  $-3 \text{ V}$ , respectively (Fig. 3). The body-bias voltages are applied symmetrically (i.e.  $V_{bb} = V_{bb,NMOS} = -V_{bb,PMOS}$ ), and homogeneously in both drivers and switches. As the optimal sizing of the PA depends on the  $R_L$  value (smaller  $R_L$  requires a proportionally larger switches area), and as  $R_L$  is defined by the required output power, we define the normalized area as the switch area for  $R_L = 1 \Omega$ . The scaling of  $R_L$  to  $50 \Omega$  can be achieved with a matching network which is not considered here. Since the scope of this work is to study the efficiency of the active part of a body-biased SCPA, the capacitances  $C_u$  and the inductance  $L_s$  are considered being ideal and defined

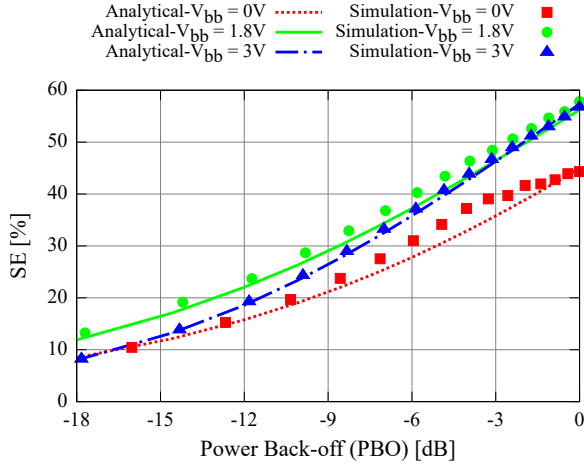


Fig. 5. Simulated SE compared to the analytical model of SE versus Power Back-Off.  $V_{bb} = 0$  V is on Design A,  $V_{bb} = 1.8$  V and  $V_{bb} = 3$  V on Design B

for  $Q_L = 3$ . For the SE simulations, a standard tapering factor of 3 is chosen in the driver chain.

We can observe in Fig. 4 the analytical models proposed in this paper compared to the simulations, with good matching for the peak DE and peak SE (i.e.  $m = M$ ). By sweeping the value of the FBB voltages in the model, we reach the optimal body-biasing at  $\pm 1.8$  V, where we obtain a 5 % improvement in DE with a significant 50 % area reduction. A stronger body-biasing annihilates any efficiency improvement as the leakage power dissipation becomes predominant (Fig. 4.a). The reduction in switch area allows to reduce the number of buffers required in the driver chain and thus shows an improvement of 14 % of the SE with a 67 % improvement of the switch area at an optimal body-biasing of  $\pm 1.8$  V (Fig. 4.b).

We observe on Fig. 5 the SE at Power Back-Off (PBO). Here we consider two different designs: the first one (Design A) is the one sized for an optimized peak SE without body-biasing (normalized area of  $\sim 1000 \mu m^2$  on Fig. 4.b) and

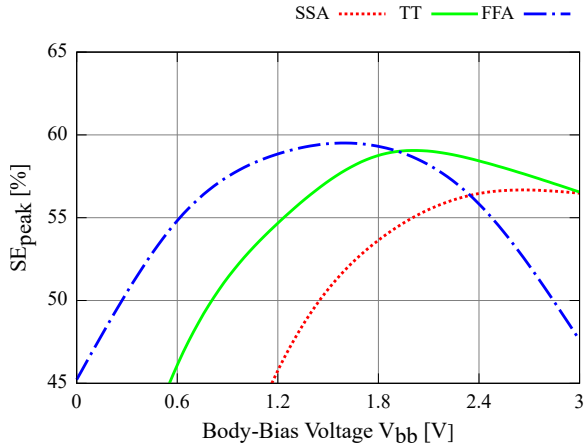


Fig. 6. Simulated Corners peak System Efficiency versus Body-Bias Voltage (on Design B)

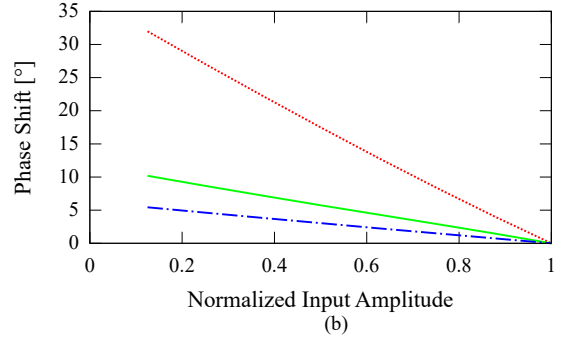
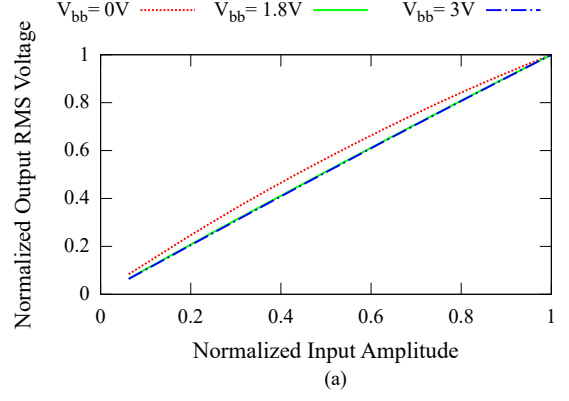


Fig. 7. Simulated (a) AM-AM and (b) AM-PM distortion.  $V_{bb} = 0$  V is on Design A,  $V_{bb} = 1.8$  V and  $V_{bb} = 3$  V on Design B

the second one (Design B) is sized for an optimized peak SE when body-biased at  $V_{bb} = 1.8$  and 3 V (normalized area of  $\sim 330 \mu m^2$  on Fig. 4.b). At  $-6$  dB PBO a body-biased SCPA at  $\pm 1.8$  V still shows a 10 % improvement compared to a non-body-biased SCPA. With a body-biasing of  $\pm 3$  V the SE decreases more rapidly with PBO, caused by a more important leakage power consumption. Furthermore, FBB also allows to compensate process, voltage and temperature (PVT) variations. As observable on Fig. 6 the optimal body bias voltage depends on the process corner. An integrated body-bias generator such as [14] could dynamically tune the body bias voltage for optimal operation under PVT variations, making the design more robust [9].

It is expected to see more impact of the FBB at higher frequencies as it allows to reduce the parasitic capacitance of the switches, reducing the frequency-dependent dynamic power dissipation, and shall benefit from the high transition frequency  $f_T$  of the FD-SOI technologies ( $\sim 300$  GHz [9]) for ultra low-power design up to 30 GHz [3], [15].

## VI. IMPACT ON LINEARITY

In this section we study the impact of Forward Body-Biasing on the linearity by using the simulation results. We consider again the two designs: Design A (sized at normalized area of  $\sim 1000 \mu m^2$  on Fig. 4.b for  $V_{bb} = 0$  V) and Design B (sized at normalized area of  $\sim 330 \mu m^2$  on Fig. 4.b for  $V_{bb} = 1.8$  and 3 V).

Linearity can be studied by simulating the AM-AM and AM-PM distortions. Two other interesting metrics are INL and



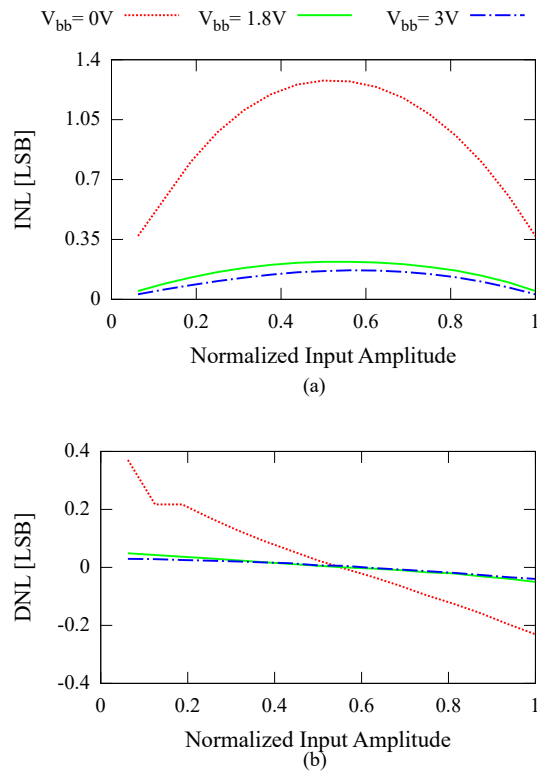


Fig. 8. Simulated (a) INL and (b) DNL.  $V_{bb} = 0$  V is on Design A,  $V_{bb} = 1.8$  V and  $V_{bb} = 3$  V on Design B

DNL as SCPA are basically RF-DACs. Nonlinear distortion is mainly due to two effects in SCPAs: (1) non-zero switching times (2) source impedance variations,  $r_s$ , depending on the input amplitude code and the parasitics ( $r_{on}$ ,  $C_p$ ) [2], [16], [17]. FBB has a positive impact on those two effects. It mainly allows to dramatically increase the switching speed of the inverters [9]. As demonstrated in the previous section, it also allows to obtain compacter design and thus to reduce even more the ON-resistance and  $C_p$  parasitics. Hence, it reduces the AM-AM distortion and divides by 3 to 5 the maximum AM-PM phase shift distortion, for  $V_{bb} = 1.8$  V and  $V_{bb} = 3$  V, respectively (Fig. 7). This is also observable on the INL/DNL metrics (Fig. 8) where FBB permits to drastically reduce the error conversions.

## VII. CONCLUSION

This paper demonstrates that forward body-biasing of low-voltage SCPA in FD-SOI technologies reduces the ON-resistance of the switches, while limiting the increase of the parasitic capacitance. This allows the reduction of the switch area by 67 % and improves by 14 % the SE. It is also shown that forward body-biasing allows for more robust design by selecting the optimal body-bias voltage depending on process corner variations. Ultimately, it is highlighted how forward body-biasing can improve the linearity of SCPAs. Using FBB in FD-SOI technology adds a tuning knob for optimizing the design for energy-efficient, compact, robust and linear ULV SCPA.

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